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# 3.3 kV 4H-SiC DMOSFET with a source-contacted dummy gate for high-frequency applications

**Kyuhyun Cha and Kwangsoo Kim†**

Department of Electronic Engineering, Sogang University, Seoul 04107, Korea

**Abstract:** In this paper, a 4H-SiC DMOSFET with a source-contacted dummy gate (DG-MOSFET) is proposed and analyzed through Sentaurus TCAD and PSIM simulations. The source-contacted MOS structure forms fewer depletion regions than the PN junction. Therefore, the overlapping region between the gate and the drain can be significantly reduced while limiting $R_{ON}$ degradation. As a result, the DG-MOSFET offers an improved high-frequency figure of merit (HF-FOM) over the conventional DMOSFET (C-MOSFET) and central-implant MOSFET (CI-MOSFET). The HF-FOM ($R_{ON}\times Q_{GD}$) of the DG-MOSFET was improved by 59.2% and 22.2% compared with those of the C-MOSFET and CI-MOSFET, respectively. In a double-pulse test, the DG-MOSFET could save total power losses of 53.4% and 5.51%, respectively. Moreover, in a power circuit simulation, the switching power loss was reduced by 61.9% and 12.7% in a buck converter and 61% and 9.6% in a boost converter.

**Key words:** 4H-SiC; MOSFET; dummy-gate; gate-drain charge; switching loss

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## 1. Introduction

4H-SiC is a wide bandgap material with excellent material properties, such as high critical electric field, high thermal conductivity, and high-temperature operation, making it suitable for high-temperature and high-voltage environments[1, 2]. In particular, high-voltage and high-frequency power devices are suitable for applications requiring high-voltage and high power density, such as the solid-state transformers used in next-generation power systems[3]. Therefore, studies on SiC MOSFETs, which have been proven to exhibit low switching losses, are being actively conducted[4].

Among SiC MOSFET structures, the trench MOSFET has a low channel resistance thanks to its high channel density and mobility[5, 6]. However, in a high-voltage SiC MOSFET (a voltage of 3.3 kV or above), the channel resistance does not have a significant effect because of the high drift resistance. In addition, at high voltages, the trench MOSFET causes a gate oxide reliability problem in the off-state operation because the electric field is concentrated in the gate oxide[7].

In previous studies, a central-implant MOSFET (CI-MOSFET) with a $p^+$ region under the gate oxide was proposed to improve the switching characteristics of the conventional DMOSFET (C-MOSFET)[8]. In this structure, the switching characteristics could be improved by reducing the overlapping region between the gate and the drain because of the source-contacted CI structure. However, $R_{ON}$ increases because of the large depletion region formed by the PN junction in the junction gate field-effect transistor (JFET)[9].

Therefore, we propose a 3.3 kV dummy-gate 4H-SiC MOSFET (DG-MOSFET) to alleviate this problem. The static characteristics of the DG-MOSFET were analyzed through a Sentaurus TCAD 2D simulation, and the dynamic characteristics were analyzed through a mixed-mode simulation[10]. The power loss was compared using a PSIM simulation. In the TCAD simulation, Shockley–Read–Hall, AUGER, and Okuto–Crowell models were applied as recombination models. In addition, the doping dependence, high field velocity saturation, and Enormal were used as mobility models. To consider the device process, the trap concentration between the $SiO_2$ and SiC interfaces was set to $3\times10^{12}$ $eV^{-1}$ $cm^{-2}$[11–13].

## 2. Proposed structure and fabrication procedure

### 2.1. Structures of DG-MOSFETs

Fig. 1 shows the cross-sectional schematics of the C-MOSFET, CI-MOSFET, and DG-MOSFET. All of the structures have the same drift thickness (i.e., 30 $\mu$m) and the concentration of the drift region is $1.7\times10^{15}$ $cm^{-3}$. The junction depth of the p base is 1 $\mu$m. In the DG-MOSFET, $C_{GD}$ was reduced using the source-contacted DG structure under an active gate to reduce the overlapping region between the gate and the drain[14]. Since the DG is a MOS structure, it has fewer depletion regions than the PN junction[15]. Therefore, the HF-FOM is improved because $C_{GD}$ can be reduced while limiting the $R_{ON}$ degradation. Additionally, in the DG-MOSFET, a source contact is possible using the same method as when forming the source-contacted $p^+$ shielding in the trench MOSFET[16].

### 2.2. Fabrication procedure for DG-MOSFETs

Fig. 2 shows the proposed process flow to demonstrate the feasibility of the DG-MOSFET. The p base and $n^+$ sources were formed by double diffusion. After forming the nitride hard mask, it was patterned to use the hard mask for dummy etching and then the dummy area was etched. Subsequently, the $SiO_2$ layer is formed in the dummy region by deposition and patterning. Typically, the gate oxide is formed by

Correspondence to: K Kim, kimks@sogang.ac.kr
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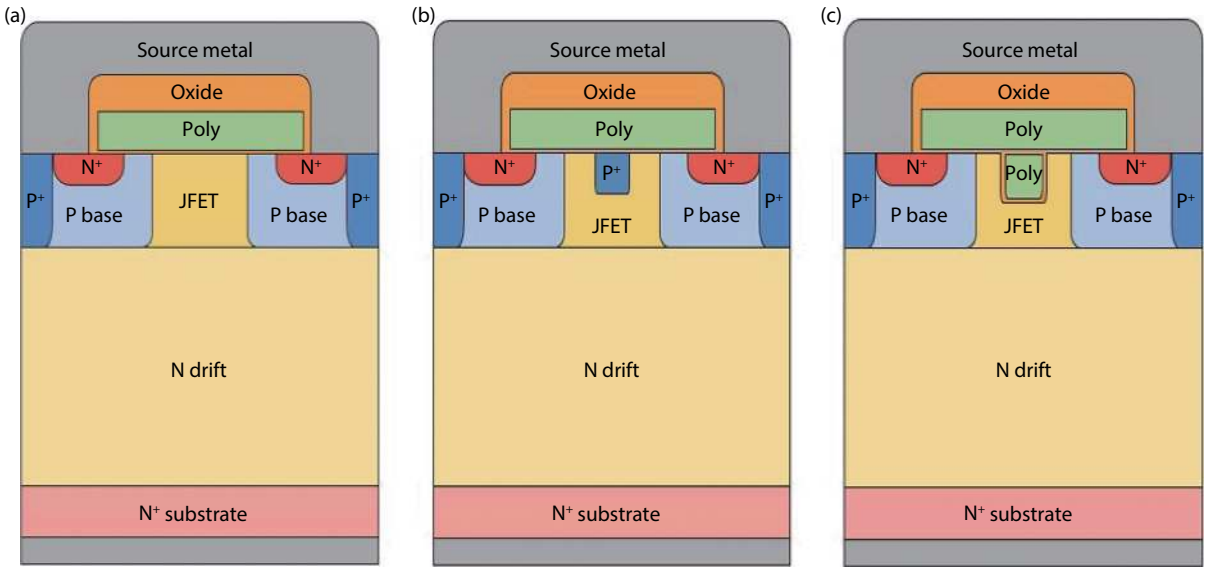


Fig. 1. (Color online) Schematic cross-sectional structure of (a) C-MOSFET, (b) CI-MOSFET, and (c) DG-MOSFET.

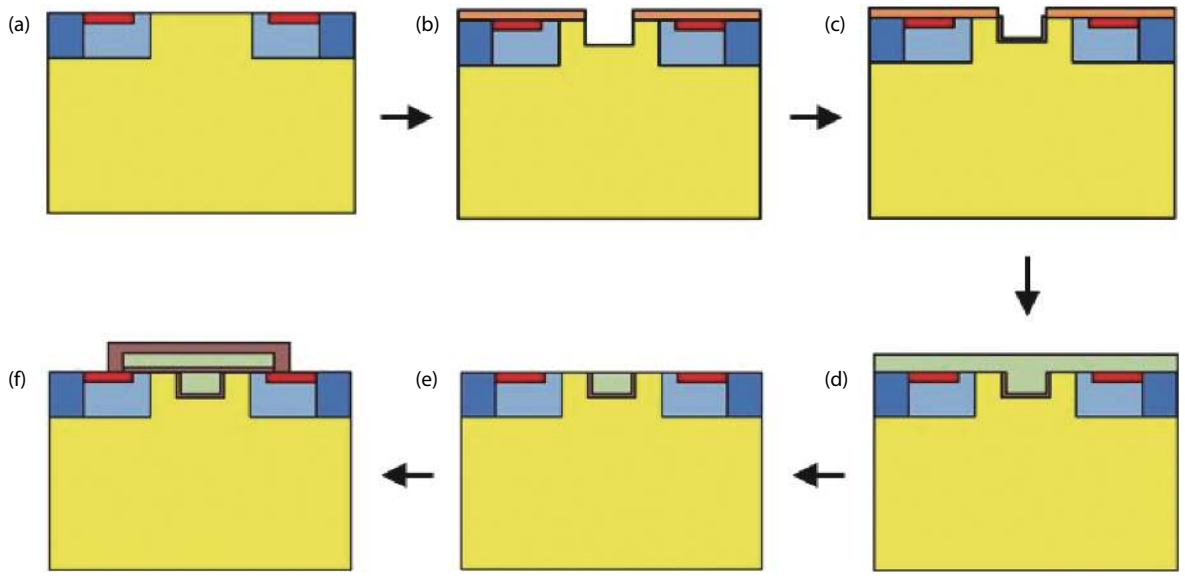


Fig. 2. (Color online) Proposed key fabrication process flow of DG-MOSFET. (a) Ion implantation to form the p-well and $n^+$ source. (b) Dummy etching. (c) Dummy oxide deposition. (d) Nitride mask removal & poly-Si deposition. (e) Poly-Si etchback. (f) Gate oxidation and patterning.

thermal oxidation. However, when $SiO_2$ is grown by thermal oxidation, it is difficult to have the same thickness at the sidewall and bottom of the dummy region because the difference in the growth rate of $SiO_2$ between the sidewall and trench bottom is due to the different crystal orientation[17]. Therefore, in the proposed structure, it was considered that the oxide in the dummy region was formed by the deposition process. After the nitride hard mask was removed, poly-Si was deposited and then etched to form poly-Si in the dummy area. The gate oxide was grown by thermal oxidation and then gate patterning was applied after the deposition of the gate poly-Si.

## 3. Optimizing the structures

To analyze the performance of the proposed device, the compared devices were optimized. The CI-MOSFET and DG-MOSFET were optimized based on the C-MOSFET. The drift thickness and concentration were fixed at 30 $\mu$m and $1.7 \times 10^{17}$ $cm^{-3}$, respectively.

### 3.1. Optimizing the C-MOSFET

Fig. 3 shows the trade-off relationship between $R_{ON}$ and BV based on the changes in the JFET width ($W_{JF}$) and concentration ($N_{JF}$). As shown, $R_{ON}$ and BV decrease at the same time as $W_{JF}$ increases. As $W_{JF}$ increases, the proportion of the depletion region in the JFET decreases. Therefore, the current path increases, thus decreasing $R_{ON}$. Meanwhile, the voltage concentrated in the $p^+$ region increases, which causes BV reduction. Baliga's FOM ($BV^2/R_{ON}$) was compared to optimize the C-MOSFET considering the trade-off between $R_{ON}$ and BV, which is shown in Fig. 4. When $W_{JF}$ is 3.5 $\mu$m, the FOM is highest at all $N_{JF}$. However, $E_{MOX}$ should not exceed 4 MV/cm considering the reliability of the gate oxide[18]. $E_{MOX}$ increases with increasing $N_{JF}$, which is more remarkable with increasing $W_{JF}$. As a result, the C-MOSFET has the highest FOM when $N_{JF}$ and $W_{JF}$ are, respectively, $3 \times 10^{16}$ $cm^{-3}$ and 3.5 $\mu$m. In addition, $E_{MOX}$

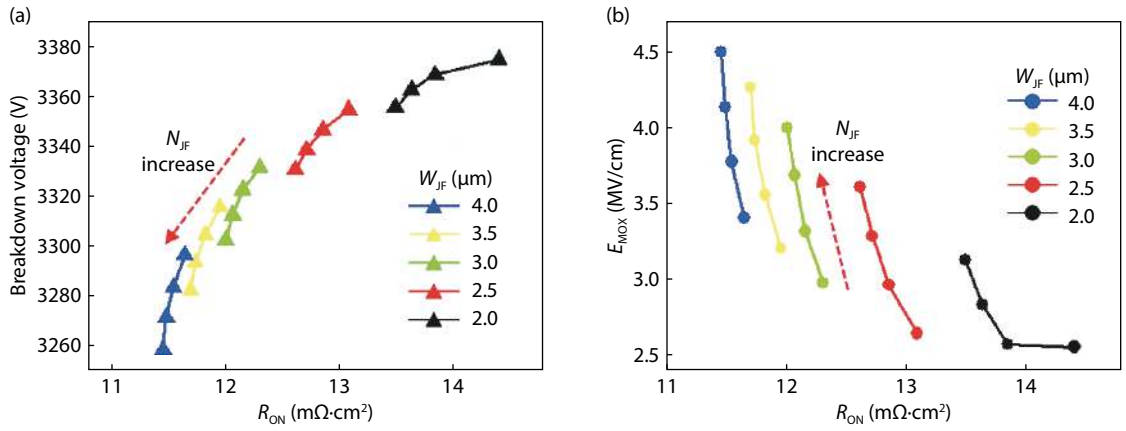


Fig. 3. (Color online) Influences of $W_{JF}$ and $N_{JF}$ of C-MOSFET. (a) The trade-off between $R_{ON}$ and BV and (b) $R_{ON}$ and $E_{MOX}$ ($E_{MOX}$ was measured at $V_{DS}$ = 3300 V.).

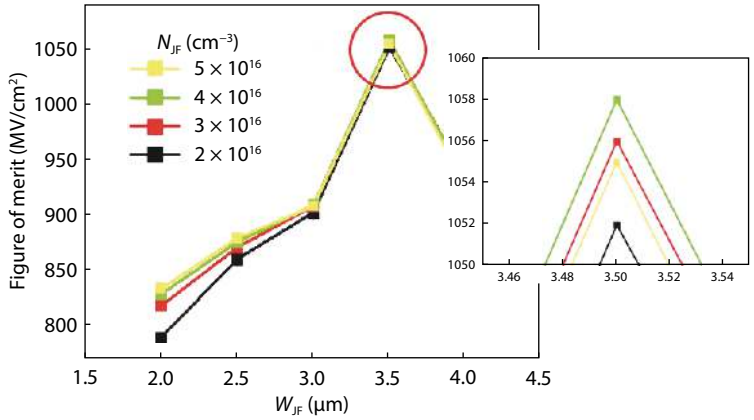


Fig. 4. (Color online) Changes of FOM according to $W_{JF}$ and $N_{JF}$ of C-MOSFET.

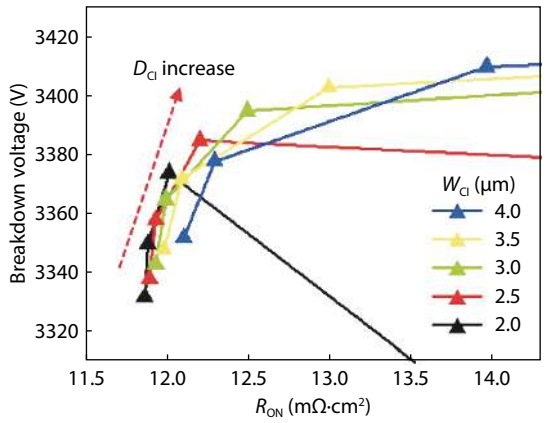


Fig. 5. (Color online) The trade-off between $R_{ON}$ and BV as variation of $W_{CI}$ and $D_{CI}$.

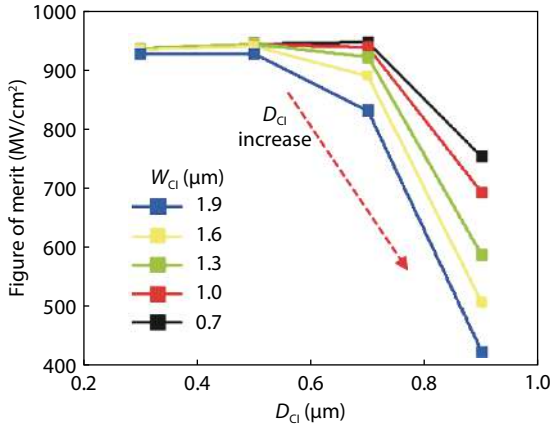


Fig. 6. (Color online) FOM as a variation of $W_{CI}$ and $D_{CI}$.

does not exceed 4 MV/cm, and BV is greater than 3300 V.

### 3.2. Optimizing the CI-MOSFET

The BV, $R_{ON}$, and switching characteristics of the CI-MOSFET and DG-MOSFET are significantly affected by the CI and DG structures, respectively, existing under the gate. Therefore, the CI depth ($D_{CI}$) and width ($W_{CI}$) and the dummy depth ($D_{DG}$) and width ($W_{DG}$) were varied to optimize the two structures. As previously mentioned, both the structures were optimized based on the C-MOSFET. Therefore, $W_{JF}$ and $N_{JF}$ were, respectively, fixed at 10 $\mu$m and 3 × $10^{16}$ $cm^{-3}$, which were optimized for the C-MOSFET.

Fig. 5 shows the trade-off between $R_{ON}$ and BV of the CI-MOSFET when $W_{CI}$ and $D_{CI}$ are simultaneously varied. During the optimization process, $D_{CI}$ and $W_{CI}$ were varied from 0.3 to 0.9 $\mu$m and from 0.7 to 1.9 $\mu$m, respectively. In Fig. 5, at the same $W_{CI}$, $R_{ON}$ increases as $D_{CI}$ increases. Moreover, $R_{ON}$ increases as $W_{CI}$ increases at the same $D_{CI}$. This happens because the current path in the JFET decreases because of an increase in the CI region. In particular, as $W_{CI}$ increases, the accumulation layer under the gate decreases, so $R_{ON}$ increases rapidly. However, the CI structure causes BV to increase by dis-

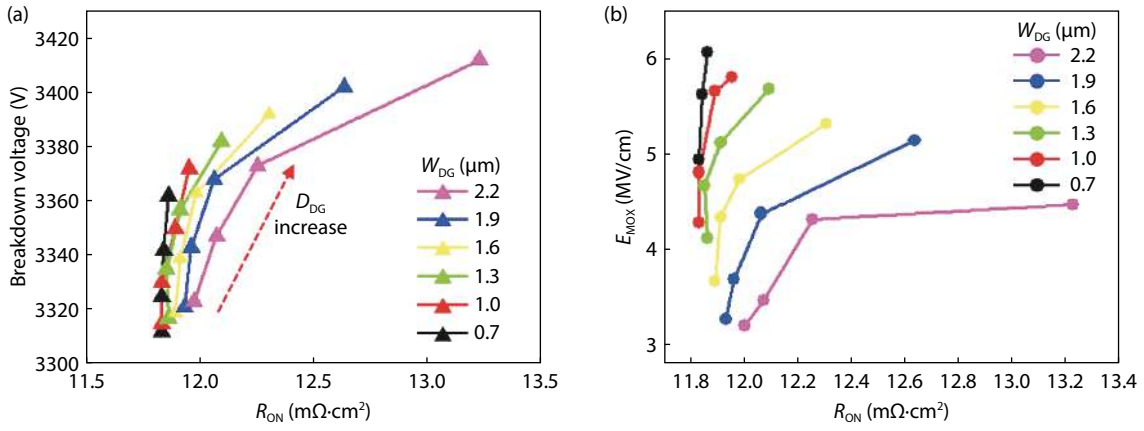


Fig. 7. (Color online) Influences of $W_{DG}$ and $D_{DG}$ of DG-MOSFET. (a) Trade-off between $R_{ON}$ and BV and (b) $R_{ON}$ and $E_{MOX}$ ($E_{MOX}$ was measured at $V_{DS}$ = 3300 V.).

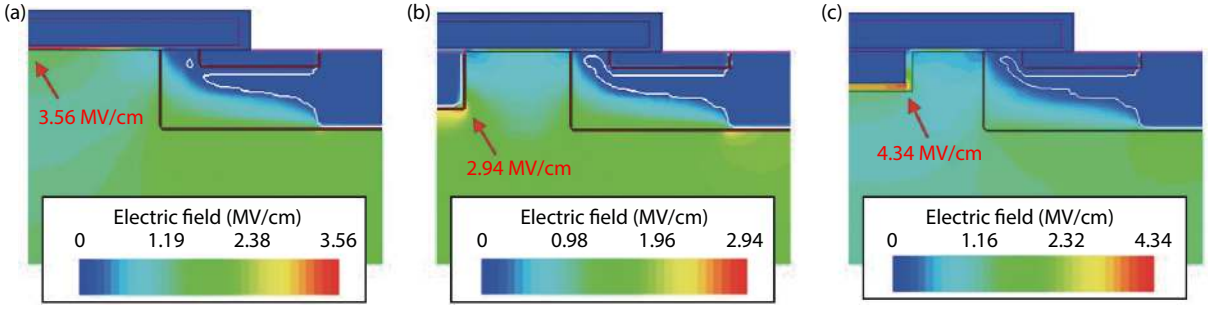


Fig. 8. (Color online) Electric field distribution of three structures at $V_{DS}$ = 3300 V. (a) C-MOSFET. (b) CI-MOSFET. (c) DG-MOSFET.

persing the electric field concentrated in the p base. Therefore, to optimize the CI-MOSFET, it is necessary to compare the variation in the FOM based on the changes in $W_{CI}$ and $D_{CI}$. In Fig. 5, BV decreases rapidly when $D_{CI}$ is 0.9 $\mu$m. This happens because the electric field is concentrated in the CI structure when $D_{CI}$ is too deep. This effect increases at lower $W_{CI}$. Therefore, the CI structure has the highest FOM when $D_{CI}$ = 0.7 $\mu$m and $W_{CI}$ = 0.7 $\mu$m as specified in Fig. 6.

### 3.3. Optimizing the DG-MOSFET

The DG-MOSFET was optimized in the same way as the CI-MOSFET. Fig. 7 shows the result. The oxide thickness of the dummy region was fixed at 100 nm. As mentioned previously, the oxide in the dummy area was formed through a deposition process.

As shown in Fig. 7, $D_{DG}$ and $W_{DG}$ are varied from 0.3 to 0.7 $\mu$m and from 0.7 to 2.2 $\mu$m, respectively. For the same reason as that for the CI-MOSFET, an increase in the dummy area increases both $R_{ON}$ and BV. Fig. 7(b) shows the variations in $E_{MOX}$ and $R_{ON}$ based on the changes in $W_{DG}$ and $D_{DG}$. $E_{MOX}$ increases when $D_{DG}$ increases because of a decrease in the distance between the dummy oxide and the drain. In Fig. 8, the vertex of the dummy has the highest electric field because of the electric crowding effect. This effect is alleviated with increasing $W_{DG}$ because the depletion region between the p base and the n drift protects the dummy oxide[19]. Therefore, $E_{MOX}$ is reduced when $W_{DG}$ increases. However, as previously mentioned, $R_{ON}$ increases significantly because of the reduction in the current path. As a result, $D_{DG}$ and $W_{DG}$ were optimized to 0.5 and 1.6 $\mu$m, respectively.

## 4. Analysis of the electrical characteristics

### 4.1. Static characteristics

Based on the above results, we compared the performance of the three optimized structures. Fig. 9 shows their blocking and output characteristics. The blocking characteristics were measured at $V_{GS}$ = 0 V, and the output characteristics were obtained at $V_{GS}$ = 20 V. Because of the source-contacted region in the JFET, the CI-MOSFET and DG-MOSFET have 16.2% and 15.2% higher $R_{ON}$ than C-MOFET, respectively. The BV values of the two structures are higher than that of the C-MOSFET because of the electric field dispersion effect. Table 1 lists the results of the static characteristics of the three optimized structures. The CI-MOSFET and DG-MOSFET have 10.4% and 11.5% lower static FOM than the C-MOSFET, respectively.

### 4.2. Dynamic characteristics

The static FOM values of the CI-MOSFET and DG-MOSFET deteriorate compared with that of the C-MOSFET. Nevertheless, both structures have improved switching characteristics. The increase in $R_{ON}$ and the decrease in the switching power loss are in a trade-off relationship. Typically, $R_{ON}$ is increased to reduce the switching power loss in high-frequency applications[20].

Fig. 10 shows the input capacitance ($C_{ISS}$ = $C_{GS}$ + $C_{GD}$) and reverse transfer capacitance ($C_{RSS}$ = $C_{GD}$) of the three structures with respect to $V_{DS}$ when $V_{GS}$ = 0 V[1, 21]. To extract the results shown in Fig. 10, a low AC signal was applied at 1 MHz. A comparison of the $C_{ISS}$ values of the three structures

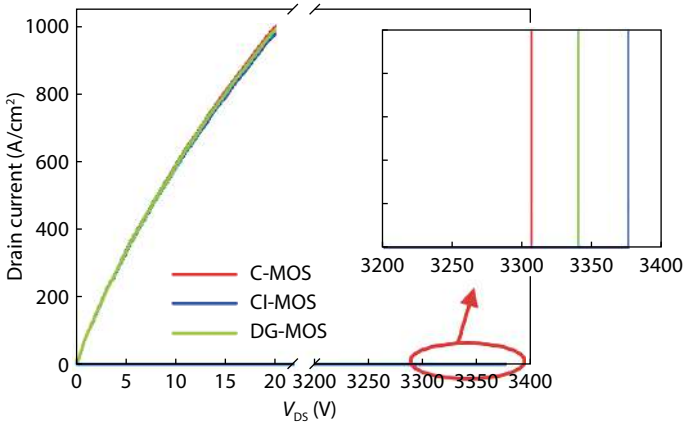


Fig. 9. (Color online) Static characteristics of three structures.

Table 1. Static characteristics of the optimized three structures.

| Parameter | C-MOSFET | CI-MOSFET | DG-MOSFET |
|---|---|---|---|
| $R_{ON}$ (mΩ·cm²) | 10.34 | 12.01 | 11.91 |
| BV (V) | 3305 | 3374 | 3343 |
| FOM (MW/cm²) | 1056 | 947 | 934 |

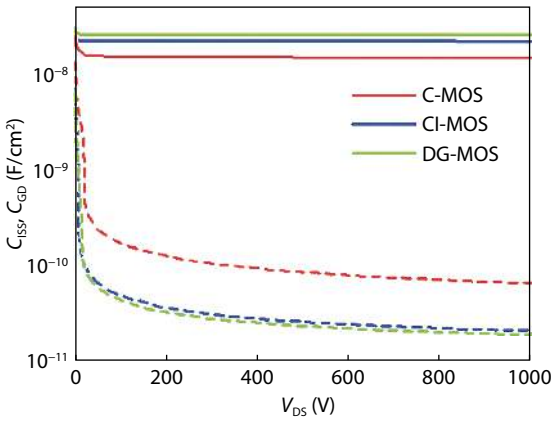


Fig. 10. (Color online) Input and Gate-Drain capacitance of three structures.

shows that the $C_{ISS}$ values of the CI-MOSFET and DG-MOSFET are significantly higher. This can be attributed to the presence of the source-contacted region (CI and DG) under the gate. Meanwhile, the $C_{GD}$ values of the CI-MOSFET and DG-MOSFET significantly decreased. $C_{GD}$ is significantly influenced by the overlapping area between the gate and the drain. The DG-MOSFET can have a wider source-contacted area under the gate when it has a similar static FOM as that of the CI-MOSFET. Therefore, the DG-MOSFET has the lowest $C_{GD}$ because it has the smallest overlapping area between the gate and the drain. Therefore, the DG-MOSFET has 71% and 8.3% lower $C_{GD}$ than the C-MOSFET and CI-MOSFET.

Fig. 11 shows the gate charge curves of the three structures. The test circuit is specified in Fig. 11, and a current of 100 mA was applied to charge the gate. The $Q_{GD}$ value of the C-MOSFET is higher than those of the CI-MOSFET and DG-MOSFET. This happens because $C_{GD}$ is significantly reduced in both the structures. The HF-FOM values of the three structures were calculated and compared in Table 2. For the CI-MOSFET and DG-MOSFET, $R_{ON}$ increased compared with that of C-MOSFET, but $Q_{GD}$ decreased significantly. As a result, the DG-MOSFET has a 59.2% lower HF-FOM than the C-MOSFET

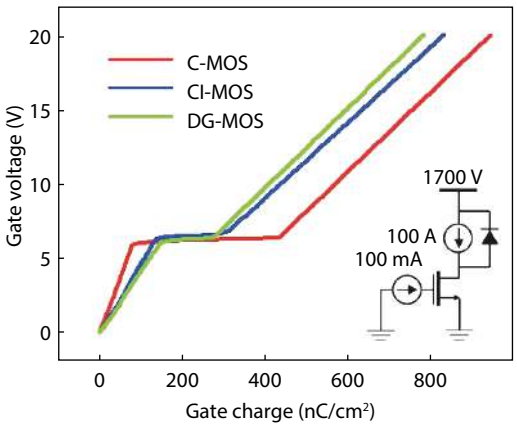


Fig. 11. (Color online) Gate-drain charge curve of three structures.

Table 2. Capacitance and gate charge values of the three structures.

| Parameter | C-MOSFET | CI-MOSFET | DG-MOSFET |
|---|---|---|---|
| $C_{ISS}$ (nF/cm²) | 14.8 | 21.9 | 25.7 |
| $C_{GD}$ (pF/cm²) | 66.67 | 21.12 | 19.36 |
| $Q_{GD}$ (nC/cm²) | 353.1 | 159.5 | 125.3 |
| $R_{ON}$×$Q_{GD}$ (mΩ·nC) | 3651 | 1916 | 1492 |

$C_{RSS}$ and $C_{GD}$ were simulated at $V_{DS}$ = 1000 V and $Q_{GD}$ was simulated at $I_{GS}$ = 100 mA and $V_{DD}$ = 1700 V.

and 22.2% lower than the CI-MOSFET.

Fig. 12 shows a diagram comparing the switching characteristics of the three structures through a double-pulse test simulation. Figs. 12(a) and 12(b) show the turn-off and turn-on transients, respectively. The test circuit is specified in Fig. 12(a), and the load inductance and stray inductance are 400 $\mu$H and 10 nH, respectively.

Consequently, the power losses in the DG-MOSFET and CI-MOSFET are significantly lower than those in the C-MOSFET. Table 3 lists the switching power loss during the double-pulse test. As listed, the DG-MOSFET has 53.4% and 5.5% lower total switching loss ($E_{SW}$) than the C-MOSFET and CI-MOSFET, respectively.

### 4.3. Power loss simulation

The power loss was compared using devices as switches in the power circuit through a PSIM simulation. Fig. 13 shows the buck converter and boost converter circuits used in the power loss simulation. Both circuits comprise an RLC passive device, a diode, and a switch. The L and C components help

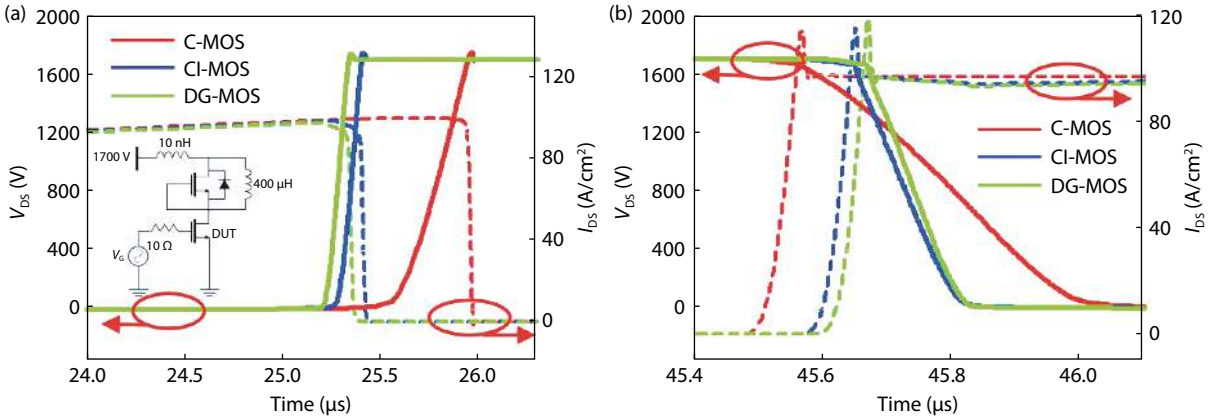


Fig. 12. (Color online) (a) Turn off and (b) turn on transient of the three structures.

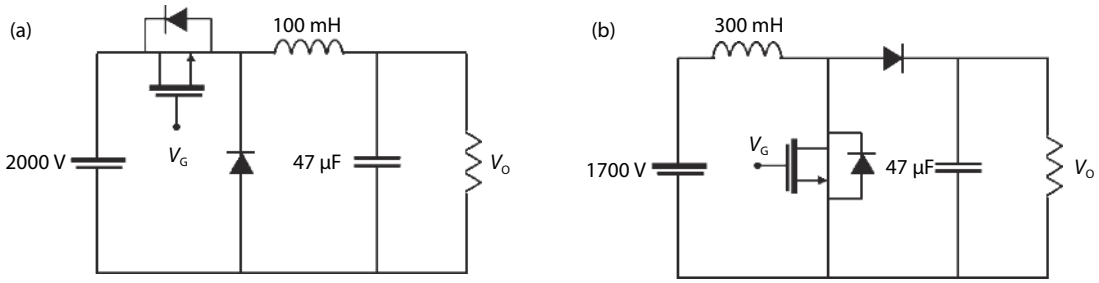


Fig. 13. (a) Buck converter and (b) boost converter circuit used in the power loss simulation.

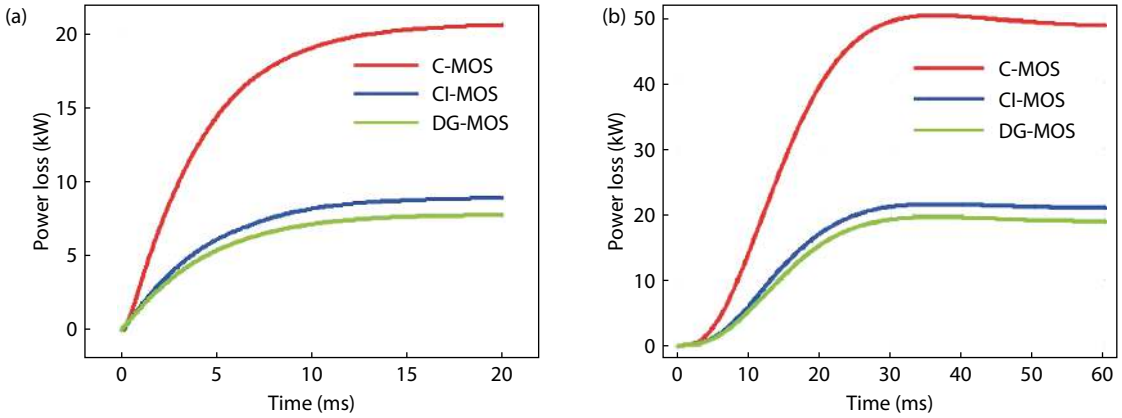


Fig. 14. (Color online) Switching power loss in the power circuit. (a) Buck converter. (b) Boost converter.

Table 3. Double-pulse test simulation results.

| Parameter | C-MOSFET | CI-MOSFET | DG-MOSFET |
|---|---|---|---|
| $E_{ON}$ (mJ/cm$^2$) | 41.9 | 17.27 | 16.03 |
| $E_{OFF}$ (mJ/cm$^2$) | 11.27 | 7.84 | 7.68 |
| $E_{SW}$ (mJ/cm$^2$) | 53.17 | 25.11 | 23.71 |

Table 4. Power simulation results ($f$ = 500 kHz).

| Power circuit | C-MOSFET | CI-MOSFET | DG-MOSFET |
|---|---|---|---|
| Buck converter (kW) | 20.616 | 8.934 | 7.784 |
| Boost converter (kW) | 48.731 | 20.923 | 18.901 |

to remove the unnecessary ripple elements of the output voltage[22]. The C-MOSFET, CI-MOSFET, and DG-MOSFET are used as switches in the power circuit. In consideration of the ideal gating block in the input gate voltage, the duty cycle was set to 0.5 and the frequency was set to 500 kHz. Finally, the output voltage was measured as the voltage of the load resistance.

Fig. 14 shows the power loss simulation results. These results are specified in Table 4. They were recorded after each circuit reached a steady state. As mentioned previously, the DG-MOSFET has the least $P_{SW}$. Consequently, when the DG-MOSFET is used as a switch, $P_{SW}$ is improved by 61.9% and 12.7% compared with those of the C-MOSFET and CI-MOSFET in the buck converter. Likewise, in the boost converter, $P_{SW}$ is improved by 61% and 9.6%, respectively.

## 5. Conclusion

In this study, a 4H-SiC DMOSFET with a source-contacted dummy gate (DG-MOSFET) was developed and compared with the C-MOSFET and CI-MOSFET through TCAD and PSIM simulations. The simulation results confirmed that the pro-

posed DG-MOSFET structure has the least $P_{SW}$. When applied to a power circuit, this structure could save 61% and 12% $P_{SW}$ in the buck converter and 61% and 9.6% $P_{SW}$ in the boost converter. In particular, the DG-MOSFET exhibited a lower $R_{ON}$ than the CI-MOSFET. Consequently, it exhibited a lower HF-FOM and a lower switching loss than the C-MOSFET and CI-MOSFET. Thus, it can be concluded that the proposed DG-MOSFET is more suitable for high-frequency applications.

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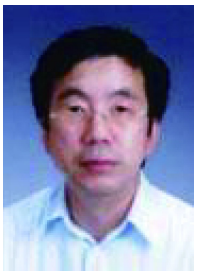
**Kyuhyun Cha** got his BS defree from Dankook University in 2020. Now he is in Master's course at Sogang University under the supervision of Prof. Kim. His research focuses on 4H-SiC semiconductors.



**Kwangsoo Kim** is Professor of the Department of Electronic Engineering at Sogang University. He holds degrees from Sogang University (BSEE, 1881, MSEE, 1983 and PhDEE, 1992). From 1982 to 1998 he was with the Electronics and Telecommunications Research Institute, working on silicon devices (CMOS, Bipolar & BiCMOS). From 1988 to 1992, he carried out his PhD dissertation at Sogang Graduate School on the high speed and high density BiCMOS device. From 1999 to 2005 he was principal research engineer with IITA where he planned new component technology about Information & Communication Technology of Korea. From 2005 to 2008 he was principal research engineer with DGIST where he conducted research on IT convergence technology for intelligent vehicles. He joined Sogang University in 2008. His current research interests focus on the technology, modeling and reliability analysis of SiC power devices for electric vehicles.