REVIEWS

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A review of manufacturing technologies for silicon carbide superjunction devices

Run Tian[1, 2], Chao Ma[3, †], Jingmin Wu[1, 2], Zhiyu Guo[1, 2], Xiang Yang[1], and Zhongchao Fan[1, 4, †]

[1]Engineering Research Center for Semiconductor Integrated Technology, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China

[2]College of Materials Science and Opto-Electronic Technology, University of Chinese Academy of Sciences, Beijing 100049, China

[3]University of Electronic Science and Technology of China, Chengdu 610054, China

[4]School of Electronic, Electrical and Communication Engineering, University of Chinese Academy of Sciences, Beijing 100049, China

Abstract: Superjunction technology is believed to reach the optimal specific on-resistance and breakdown voltage trade-off. It has become a mainstream technology in silicon high-voltage metal oxide semiconductor field effect transistor devices. Numerous efforts have been conducted to employ the same concept in silicon carbide devices. These works are summarized here.

Key words: silicon carbide (SiC); power semiconductor devices; superjunction (SJ); process development

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1. Introduction

Power semiconductor devices play an important role in electric transmission and power conversions[1, 2]. To reduce power consumption and improve energy efficiency, it is necessary to reduce the specific on-resistance ($R_{on,sp}$) of power devices. However, the breakdown voltage (BV) is supported by the drift region in the semiconductor epitaxial layer. The BV increases with the thickness of the epitaxial layer, which leads to a higher $R_{on,sp}$. Based on the typical P–i–N structure shown in Fig. 1(a), the relationship between $R_{on,sp}$ and BV can be derived from Poisson's equation[3]:

$$\frac{\partial E(y)}{\partial y} = -\frac{qN_D}{\varepsilon_s}, \tag{1}$$

where N_D is the donor concentration in the uniformly doped drift region, q is the electron charge, and ε_s is the dielectric constant of the substrate material.

The solution of Eq. (1) indicates a triangular electric profile across the drift region, as shown in Fig. 1(b)[3]. The depletion width of the drift region (L_{PiN}) under breakdown conditions is given by[3]:

$$L_{PiN} = \frac{2BV}{E_C}, \tag{2}$$

where BV is the breakdown voltage and E_C is the critical electric field of the substrate material. The specific on-resistance for the drift region in P–i–N diode ($R_{on,sp\text{-}PiN}$) is given by[3]:

$$R_{on,sp\text{-}PiN} = \frac{4BV^2}{\varepsilon_s \mu_N {E_C}^3}. \tag{3}$$

From Eq. (3), the following relationships can be obtained:

$$R_{on,sp\text{-}PiN} \propto \frac{1}{{E_C}^3}, \tag{4}$$

$$R_{on,sp\text{-}PiN} \propto BV^2. \tag{5}$$

Eq. (4) indicates that power devices made of the substrate material with a higher critical electric field (E_C) will have lower $R_{on,sp}$. The E_C of silicon (Si) and 4H silicon carbide (4H-SiC) are about 0.3 and 3.2 MV/cm, respectively. Thus, at the same BV, the $R_{on,sp}$ of SiC power devices will be much lower than that of Si power devices. Additionally, SiC has more excellent properties, superior to other semiconductor materials used in the power devices, such as high thermal conductivity, high saturation drift velocity, and the ability to form silicon dioxide (SiO_2) as a native oxide[4].

According to Eq. (5), for simple P–i–N structures, the $R_{on,sp\text{-}PiN}$ increases with BV at a quadratic rate. The introduction of superjunction (SJ) structure into the power industry in the late 1990s significantly improved the BV–$R_{on,sp}$ trade-off from quadratic to linear.

A typical SJ structure consists of alternating n- and p-type columns, as shown in Fig. 2(a). In the SJ structure, the voltage blocking capability is enhanced by the two-dimensional extension of the depletion layers. The electric field distribution in two directions is shown in Fig. 2(b). When the charges in the n- and p-columns are fully compensated, the electric field distribution of the drift region along the y-direction is uniform at a value equal to critical electric field (E_C). The depletion width of the SJ structure (L_{SJ}) is given by[3]:

$$L_{SJ} = \frac{BV}{E_C}. \tag{6}$$

The specific on-resistance for the drift region in the typical SJ device ($R_{on,sp\text{-}SJ}$) is given by[3]:

Correspondence to: C Ma, machao@ime.ac.cn; Z C Fan, zcfan@semi.ac.cn
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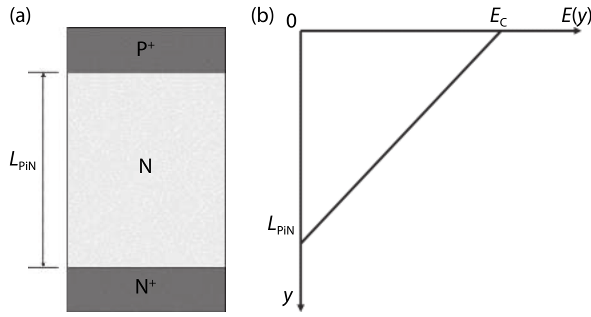

Fig. 1. (a) A typical P–i–N structure. (b) Electric field distribution.

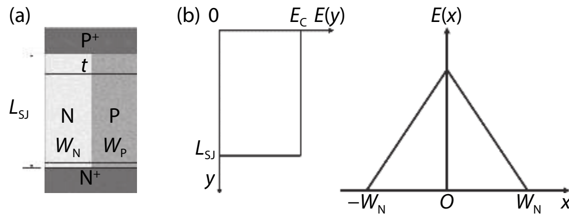

Fig. 2. (a) SJ structure. (b) Electric field distribution in *y*- and *x*-directions.

$$R_{on,sp\text{-}SJ} = \frac{2t\mathrm{BV}}{\mu_N \varepsilon_s {E_C}^2}. \tag{7}$$

Therefore, the relationship between $R_{on,sp\text{-}SJ}$ and BV is:

$$R_{on,sp\text{-}SJ} \propto \mathrm{BV}. \tag{8}$$

The $R_{on,sp}$ for SJ structure devices increases linearly with BV. Compared with Eq. (5), the $R_{on,sp}$ and BV trade-off has been improved in the SJ structure. Thus, since 2000, SJ high voltage Si metal oxide semiconductor field effect transistor (MOSFET) technology has gradually become a dominant technology for applications above 600 V.

Similar to Si, SJ technology could also be introduced in SiC power devices to improve the BV–$R_{on,sp}$ trade-off relationship. For the higher voltage power devices, such as 10 kV, the thickness of the SiC epitaxial layer of a typical P–i–N structure should be more than 60 μm, according to Eq. (2). To make such a thick epitaxial layer, the epitaxial growth rate needs to be increased to improve throughput. However, for such a thick epitaxy, increasing the growth rate while maintaining crystal quality and uniformity is a challenge for existing SiC epitaxy technology[5]. If the SJ structure is introduced to a 10 kV SiC device, according to Eq. (6), the thickness of the epitaxial layer can be reduced significantly. Hence, the $R_{on,sp}$ will be reduced accordingly, and the wafer throughput will be improved as well. Therefore, for higher voltage power devices, the advantages of SiC SJ technology are more obvious.

However, due to the extremely stable chemical and physical characteristics of SiC materials, it is difficult to produce an SJ structure. This paper is to summarize recent efforts to pursue SiC SJ devices.

2. Process development

Currently, multi-epitaxial growth (MEG)[6–8] and trench-filling epitaxial growth (TFE)[9–11] are two mature technologies for Si SJ devices. Following Si technology development roadmap, similar approaches have been employed for SiC SJ devices, which will be discussed in Sections 2.1 and 2.2. Additionally, a combination of the trench and implant technique was proposed as a compromise between MEG and TFE, as discussed in Section 2.3.

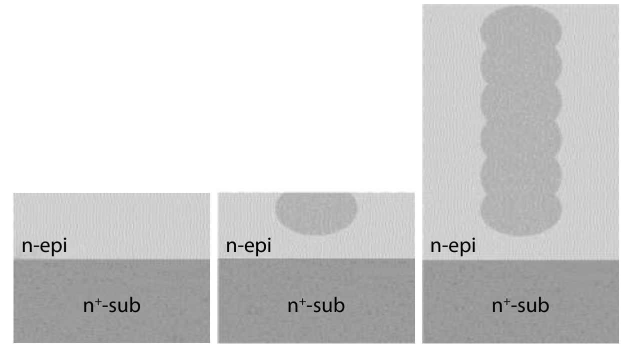

Fig. 3. Process flow diagram of MEG.

2.1. Multi-epitaxial growth (MEG)

A simplified SiC SJ structure process flow (Fig. 3) of multi-epitaxial growth (MEG) is schematically shown here: a) growing n-epitaxy on an n^+ substrate wafer; b) depositing the ion implantation hard mask; c) defining p-type columns by photolithographic and etching processes; d) p-type high energy "box" ion implantation; e) repeating the above cycle of epitaxy and ion implantation process for several times until the desired thickness is achieved; and f) annealing at high temperature to activate the p-type impurities, usually aluminum (Al) ion.

There are two advantages of this technology. One is that the doping concentration of n- and p-columns in each layer can be easily controlled[12]. And the following annealing process can recover the lattice damages, such as vacancy clusters, interstitial clusters, and antisite-vacancy pairs[4], caused by ion implantation.

Most of the MEG approach is to make p-columns on n-type epitaxial layers. The continuous p-columns of Si SJ devices were connected in MEG by diffusion in the thermal budget of the process. However, in SiC, due to the strong chemical bonding, diffusion coefficients of dopants in the high-temperature diffusion are extremely small. For example, the diffusion coefficient of Al atom, a p-type dopant Al^+ commonly used in SiC, is only about 10^{-16} cm^2 s^{-1} at a temperature as high as 1800 °C. Thus, when making SiC SJ structures, it is not practical to connect the implanted p-regions into a continuous p-column by diffusion. Therefore, the diffusion process used in Si technology is not suitable for making SiC SJ structures, and it has to rely on a multiple ion implantation process to produce a "box" doping profile in SiC. In Ref. [13], the research team of the National Institute of Advanced Industrial Science and Technology (AIST) in Japan used seven cycles of epitaxial growth and ion implantation to form an SJ structure of 4.5 μm. In order to make SJ structures with a large depth, the number of cycles is increased accordingly. However, the increase in the number of the cycles brings process challenges, such as the alignment between each step, and the stress between epitaxial layers. These challenges are critical to achieving a deep SJ structure.

Reducing the number of epitaxy-implantation cycles could be achieved by raising ion implantation energy to increase the doping depth of each cycle. In Ref. [14], the AIST research team made a test device with an SJ structure through

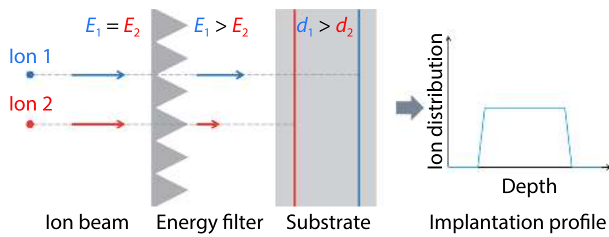

Fig. 4. (Color online) The schematic diagram of energy-filter technology[15].

Table 1. The calculation results of SRIM software.

Depth (μm)		1	3	5	10	20	50
Ion implantation energy (MeV)	N-doping	1.1	5.4	9.6	19.4	35.5	72.5
	Al-doping	1.3	7.5	16.3	38.5	75.0	165.0

two-cycle n-type epitaxial growth and high energy p-type ion implantation. Through two ion implantations with maximum energies of 7 and 5.5 MeV, respectively, Al box profiles were formed with depths of 3 and 2.5 μm. As a result, the total depth of the SJ structure was 5.5 μm.

An energy-filter technology developed by MI2-FACTORY in 2019[15] can achieve a box implantation profile in only one ion implantation shot. The schematic diagram of energy-filter technology is shown in Fig. 4. The accelerated ions lose a certain amount of energy when passing through a micro-patterned silicon membrane, and subsequently they are implanted into a shallower position in the substrate. The longer distance the ion passes through the silicon membrane, the more energy it loses, and the shallower it is implanted into the substrate. In other words, a single high-energy ion beam is converted into an ion beam with various energies after passing through the energy filter. Thus, only one implantation shot rather than multiple implantations at various energies is required to achieve a box dopant profile.

However, the main challenge of the MEG approach is the limited availability of ultra-high energy implanters (with energy in the MeV scale) for SiC wafers. In order to implant impurities as deep as 5.5 μm, an ultra-high energy above 18 MeV is needed, according to the stopping and range of ions in matter (SRIM) simulation. And to make SJ structures with depths of 10, 20, and 50 μm, the required energy is up to about 38.5, 75, and 165 MeV, respectively. SiC devices are expected to be used in ultra-high voltage applications, for instance, above 10 kV applications. The epitaxial layer thickness will exceed 100 μm. It suggests that extremely high-energy implantation tools are needed to reduce the epitaxy-implantation cycles, even with this new implantation filter technology. But the high-energy implantation process will increase unknown defects in the crystal. Thus, not only the high-energy ion implanter, but also a high-quality hard mask technology has to be developed. Due to these issues, MEG is not an efficient process option to commercialize high-voltage SiC SJ devices.

As discussed previously, existing research on SiC SJ structures through MEG mostly perform p-type ion implantation on n-type epitaxial layers, but high-energy p-type ion implantation has some technical challenges. It might be worth studying the process flow to perform n-type ion implantation on the p-type epitaxial layer. According to the SRIM simulation (Table 1), the ion implantation energies to reach the same doping depths required for nitrogen (N) ion are much lower than

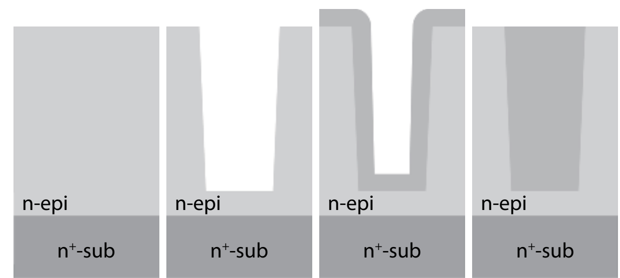

Fig. 5. Process flow diagram of TFE.

those for Al ion in SiC. N ion is an n-type dopant commonly used in SiC ion implantation. However, the epitaxial defects in p-type epitaxial layers is difficult to reduce[16]. Both high-energy p-type ion implantation and p-type epitaxial growth will increase the defects in the crystal, thus, only after the impact of the defects caused by these two process approaches (p-type implantation/n-type epitaxy and n-type implantation/p-type epitaxy) on the performances of the SiC SJ structure has been studied thoroughly, a manufacturable process can be finally decided.

2.2. Trench-filling epitaxial growth (TFE)

The process flow (Fig. 5) of trench-filling epitaxial growth (TFE) is schematically shown here: a) growing n-epitaxy or p-epitaxy on an n^+ substrate wafer; b) etching a deep trench on the epitaxial layer; c) filling the trench with p- or n-epitaxy; and d) surface planarization to facilitate subsequent device manufacturing. Most of the research is to etch trenches on n-type epitaxial layers and then fill them with p-type epitaxial layers.

As discussed in Section 2.1, due to the limitation of high-energy implantation and diffusion depth, it is not practical to make deep SJ structures by MEG, for example, a 10 μm SJ structure. Ref. [14] processed two epitaxy-implantation cycles and the ion implantation energy up to 7 MeV to produce a 5.5 μm deep SJ. At least four epitaxy-implantation cycles are required to make a 10 μm SJ structure. TFE can simplify the process greatly: etching a 10 μm trench, and growing an epitaxial layer to fill the trench. Thus, as the depth of the SJ structure increases, TFE is more practical to make SJ structures than MEG. However, there are also several technical challenges for TFE.

Firstly, the formation of micron trenches at the bottom corners during etching should be prevented. The formation of micron trenches is a common issue in SiC inductively coupled plasma (ICP) etching process. V-shaped micron trenches at the trench corners are produced when the edge of the trench is etched faster than the center of the trench[17]. The enhanced electric field crowding at the micron trenches can trigger a premature breakdown and the irreversible damage of the device[18]. Some works have demonstrated that increasing the temperature of the wafer chuck during the ICP etching process can reduce the risk of micron trenches[19]. Ref. [18] used an improved Bosch etching process and fabricated a mesa structure without micron trenches at the bottom.

Secondly, it is difficult to grow a flawless single-crystal SiC epitaxial layer to fill the trench. The epitaxial layer will grow from the bottom of the trench, as well as the sidewalls of the trench. However, the bottom and sidewalls of the

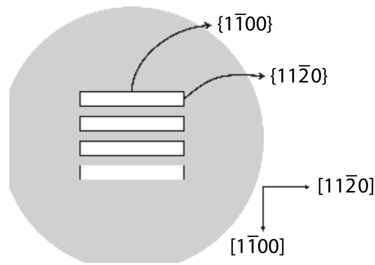

Fig. 6. A schematic diagram of trenches parallel to [11$\bar{2}$0].

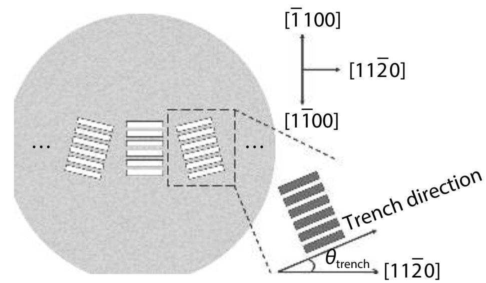

Fig. 7. The schematic diagram of the trench mask pattern.

trench are of different crystal planes. The trench bottom corresponds to (0001) while the crystal planes of the sidewalls are usually {1$\bar{1}$00} and {11$\bar{2}$0}, as shown in Fig. 6. In Ref. [20], the research team in Kyoto University studied epitaxial growth on three planar substrates, (0001) (Sample-1), {11$\bar{2}$0} (Sample-2) and {1$\bar{1}$00} (Sample-3), under the same epitaxial process conditions. The results of the samples are showing here[20]: a) wavy surface structures are observed on the surface of Sample-1 where step-flow growth occurs, and the surface roughness of Sample-1 is 0.26 nm; b) the epitaxial layer of Sample-2 exhibits an excellent surface morphology and the surface roughness of Sample-2 is 0.18 nm; c) the surface of Sample-3 has a high density of "elongated surface defects"; and the surface roughness of Sample-3 is 4.64 nm. In summary, although the process parameters of epitaxial growth are the same, the characteristics of the epitaxial layers grown on the three crystal planes, such as the types of defects and surface roughness, are completely different. Therefore, it is extremely difficult to grow flawless single crystals simultaneously on the three crystal planes in the trench.

Thirdly, a void-free trench filling is a process challenge. There might be two causes to the formation of voids during SiC trench filling. One is that the overgrowth of the epitaxial layer on the mesa top leads to close the trench opening before the trench is completely filled. This can be improved by controlling the epitaxial growth conditions, such as growth temperature, C/Si ratio (ratio of C and Si atoms in supplied source gases), and growth pressure. Due to the large surface diffusion length of reactant species at high temperature (>1600 °C)[21] and low C/Si ratio (< 1)[22], the epitaxial growth at the bottom of the trenches is enhanced compared to the growth on the top of the mesa, which can prevent the closing of the trench opening. Ref. [23] increases the growth pressure from 10 to 38 kPa, which helped reduce the epitaxial growth rate on the top of the mesa, and hence, reduced the risk of trench void formation. Additionally, Ref. [24] reported the introduction of HCl during the SiC trench-filling during chemical vapor deposition (CVD) epitaxial growth. The epitaxial growth is conducted with a minor etch by HCl. HCl could etch more SiC at the mesa than at the trench, so as to prevent the trench neck forming.

The formation of the voids can also be attributed to the tilt of the epitaxial layer on the mesa top. In Ref. [25], the AIST research team slightly misaligned the trench direction from [11$\bar{2}$0] by intention. A simplified trench mask pattern is schematically shown in Fig. 7. θ_{trench} represents the angle that the trench direction deviates from [11$\bar{2}$0] direction. In the experiments, θ_{trench} varied from −2° to 2° with a step of 0.5°. Fig. 8(a) schematically demonstrates the trench filling process. θ_{mesa} represents the tilt angle of the epitaxial layer

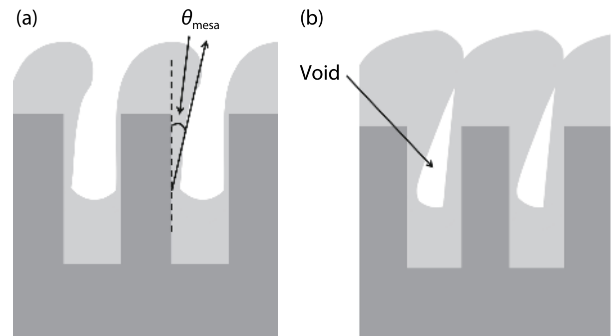

Fig. 8. The schematic diagrams of the cross section of the samples after trench filling.

grown on the mesa top. The experimental results found that θ_{mesa} increased with θ_{trench}. The excessive tilt of the epitaxial layer on the mesa top causes the trench opening to close before the trench is completely filled, and then the voids are formed [Fig. 8(b)]. Therefore, it is necessary to precisely control the trench stripe direction in accordance with the [11$\bar{2}$0] direction.

Fourthly, the doping profile of the filling region is not uniform. Ref. [26] evaluated the doping profile of the p-region by a scanning spreading resistance microscopy (SSRM). The SSRM result showed a lower concentration at the trench sidewalls. Ref. [27] found that the doping profile in the filling region of trenches without micron trenches is relatively uniform. Thus, it seems that the lower concentration at the trench sidewall might be attributed to the formation of the micron trenches at the trench corners. However, the mechanism of forming such a doping profile is still under research.

Furthermore, even a p-type epitaxial layer grown on a planar substrate still has a problem of high density of epitaxial defects[16], therefore it could be expected that p-type epitaxial growth in trenches will be more difficult. Hence, following the same logic of the previous discussion on the MEG approach, it is reasonable to infer that the approach to etch trenches on the p-type epitaxial layer, and then fill them with n-type epitaxial layers, might also be feasible. However, in addition to the challenges in reducing epitaxial defects, obtaining a uniformly grown p-type epitaxial layer on a large diameter substrate also limits the application of p-type epitaxial layers[16]. As TFE approach on n-type epitaxial materials, the formation of micron trenches at the trench corners when etching deep trenches on the p-type epitaxial layer also needs to be prevented. Moreover, the growth of an n-type epitaxial layer to fill the trench with a void-free high-quality single crystal of uniform doping profile is also a technical challenge, al-

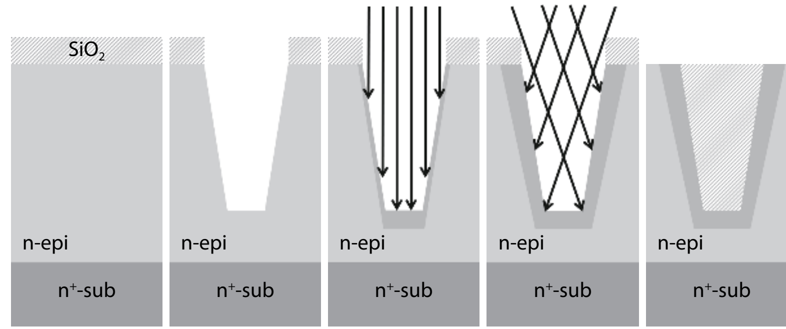

Fig. 9. Process flow of the trench and implantation technique.

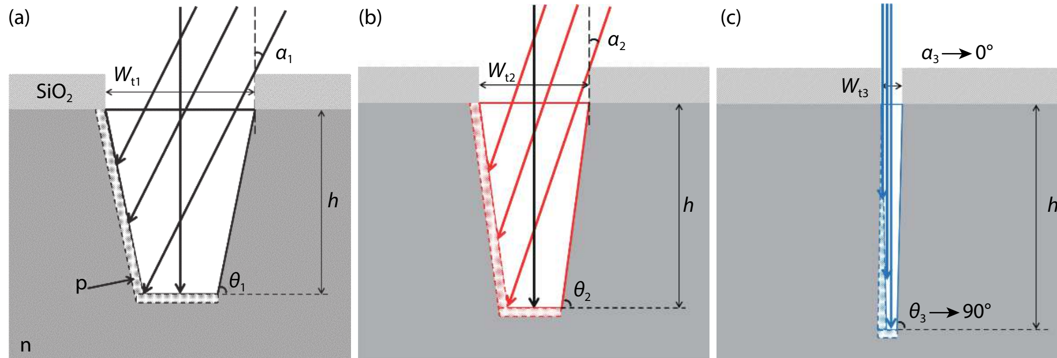

Fig. 10. (Color online) The schematic diagram of the trenches with inclined sidewall.

though it might be easier than growing p-type epitaxial layers to fill the trenches. Therefore, which approach is more feasible for mass production requires more thorough studies to evaluate and compare these two technologies.

2.3. Trench and implantation technique

As discussed previously, both MEG and TFE approaches have to overcome some technical challenges to make a functional SJ device. The research team in Zhejiang University proposed a compromise process: a combination of the trench etching and implantation technique to realize a SiC SJ structure[28].

The process flow (Fig. 9) is schematically shown here: a) growing n-epitaxy on an n^+ substrate wafer; b) etching trench with a taper angle intentionally; c) implanting straightly and then at an angle to form a p-region surrounding the trench; d) annealing at high temperature to activate the p-type dopants; e) refilling the trench by SiO_2. The p-type region surrounding the trench is performing as the p-columns in the standard SJ structures.

It is worth noting that the trench sidewall has a certain inclination. The tapered trenches favor the tilted ion implantation. However, it does not help to form a uniform implantation profile on the sidewall as the depth of the trench increasing. The schematic diagram of the trenches with an inclined sidewall is shown in Fig. 10. The three trenches shown in Fig. 10 have different depths. As the trench depth increases, the trench opening should be narrowed accordingly to reduce the cell pitch of the SJ structure, and then the slope of the sidewall would become more vertical ($\theta \rightarrow 90^{\circ}$). Moreover, in order to perform ion implantation to the bottom of the sidewall, the angle of the incident ion beam (α) is reduced. Thus, as the trench depth increases, the tilted ion implantation is not feasible to implant the trench sidewall. In this case, as shown in Fig. 10(c), the implantation to the trench sidewall could not be realized from the bottom to the top. In other words, the implantation profile on the sidewall of the deep trench is not uniform. Hence, there is a limitation in the depth of SJ structures made by this technique.

As discussed previously, SiC SJ structures are expected to be used in ultra-high voltage applications, which require a large SJ structure depth. Due to the limitation in the depth of SJ structures made by the combination of trench etching and implantation, this technology is not a feasible approach for producing SiC SJ structures in the industry.

3. Conclusion

The application of SiC SJ structure can improve the trade-off relationship between $R_{on,sp}$ and BV of SiC power devices. This paper summarized the process development to realize SiC SJ structures and the corresponding technical challenges. The works on MEG and TFE, the two main manufacturing technologies to make SiC SJ structures, were analyzed and compared. From the process simplicity point of view, the TFE approach is a more promising technology for future mass production.

Most MEG and TFE approaches perform p-type ion implantation or p-type epitaxy on an n-type epitaxial layer, though many technical challenges need to be solved in the future. Because the technical challenge of n-type ion implantation or epitaxy of SiC is less than that of p-type, it is worth studying to make SiC SJ structure by performing n-type ion implantation or epitaxial trench-filling on the p-type epitaxial layer. Therefore, it is expected to find out the works on the either p-epitaxy based MEG and TFE efforts on SiC SJ process studies in the future.

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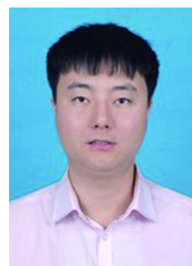
Run Tian received her B.S. degree from the Northwest University, Shaanxi, China, in 2018. She is currently working toward the M.S. degree in microelectronics and solid-state electronics at the Institute of Semiconductors, Chinese Academy of Sciences (CAS), and in the University of Chinese Academy of Sciences. Her research interests include SiC materials, SiC power devices and semiconductor manufacturing processes.



Chao Ma received the M.S. degree in integrated circuit engineering from University of Chinese Academy of Sciences, Beijing, China. He works in the Institute of Microelectronics, Chinese Academy of Sciences (CAS). His research interests include integrated circuit design, integrated circuit technology innovation and industrial development planning.

Zhongchao Fan is a professor of the Institute of Semiconductors, Chinese Academy of Science (CAS). He received his Ph.D. degree from the Institute of Semiconductors, CAS in 2004. His current research interests include wide bandgap power devices, optoelectronic devices and integration technology.