REVIEWS

Hybrid material integration in silicon photonic integrated circuits

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Abstract: Hybrid integration of III–V and ferroelectric materials is being broadly adopted to enhance functionalities in silicon photonic integrated circuits (PICs). Bonding and transfer printing have been the popular approaches for integration of III–V gain media with silicon PICs. Similar approaches are also being considered for ferroelectrics to enable larger RF modulation bandwidths, higher linearity, lower optical loss integrated optical modulators on chip. In this paper, we review existing integration strategies of III–V materials and present a route towards hybrid integration of both III–V and ferroelectrics on the same chip. We show that adiabatic transformation of the optical mode between hybrid ferroelectric and silicon sections enables efficient transfer of optical modal energies for maximum overlap of the optical mode with the ferroelectric media, similar to approaches adopted to maximize optical overlap with the gain section, thereby reducing lasing thresholds for hybrid III–V integration with silicon PICs. Preliminary designs are presented to enable a foundry compatible hybrid integration route of diverse functionalities on silicon PICs.

Key words: CMOS technology; photonic integrated circuits; hybrid integration; ferroelectric modulator

1. Introduction

During the past several decades, silicon photonics has gradually matured into an attractive platform to meet the ever-increasing demands of optical communications[1], optical sensing[2], microwave photonics[3], and classical and quantum computing to name a few[4]. As silicon foundries continuously augment their mature complementary metal–oxide–semiconductor (CMOS) capabilities with ultra-low-loss single-mode waveguides with high index contrast enabling high density, ultra-compact integration, together with integration of light sources and detectors on-chip, benchtop free-space optical measurements with arduous and fragile alignment requirements are gradually transitioning to pre-aligned component integration on chip. Photonic components such as multimode interference (MMI) devices, directional couplers, microring modulators (MRMs) and Mach–Zehnder interferometers (MZIs) enable low-cost, low-power, compact optical beam-splitting and interferometry on chip. An electronic-photonic integrated system on a CMOS platform will thus enable a low c-SWaP (cost, size, weight and power) packaged system with advanced functionality, performance and scalability.

In this context, silicon and silicon nitride waveguides have experimentally demonstrated low propagation losses, ~0.3 and ~0.06 dB/cm respectively on 300 mm foundry platforms; however other functional challenges remain. Silicon is an indirect bandgap semiconductor and hence does not emit light efficiently at room temperature. Silicon nitride has a very large bandgap and does not emit light either. In contrast, quantum well (QW), quantum-dot (QD) and quantum-

dash emitters in direct bandgap III–V semiconductors such as InP and GaAs efficiently emit light at visible, near-infrared and mid-infrared wavelengths. III–V materials can also function as efficient detectors when integrated with ultra-low-loss (ULL) silicon nitride at visible wavelengths. Silicon modulators need to be doped for operation in injection, depletion or accumulation modes that rely on changes in carrier concentration in the waveguiding region with applied bias[5–7]. Doped waveguides have higher propagation loss than passive waveguides. In contrast, materials such as lithium niobate (LN), barium titanate (BTO) and electro-optic (EO) polymers have intrinsic electro-optic coefficients much larger than values in silicon and have experimentally demonstrated large in-device EO-coefficients in low-loss waveguides on silicon substrates[8–10]. Over the past two decades, hybrid material integration strategies with silicon and silicon nitride waveguides have thus been effectively pursued to enhance photonic functionalities on the CMOS platform. In this paper, we review some of the hybrid photonic integration methods pursued in the literature that are gradually transitioning to foundry adoption. We specifically review the concept of adiabatic mode energy transfer[11] for efficient coupling of the optical modes between heterogeneous material waveguiding elements.

2. Light source integration

Hybrid integration of light sources on chip have been achieved with flip-chip bonding[12], direct growth[13] and die-to-wafer bonding[14]. Some bonding approaches have used BCB bonding[15], metal-assisted bonding[16, 17] and direct wafer bonding[18]. In recent years, fully processed lasers have been transfer printed onto silicon and silicon nitride waveguides[19, 20]. While alignment to sub-micron precision is a requirement for the above methods, an alternative method

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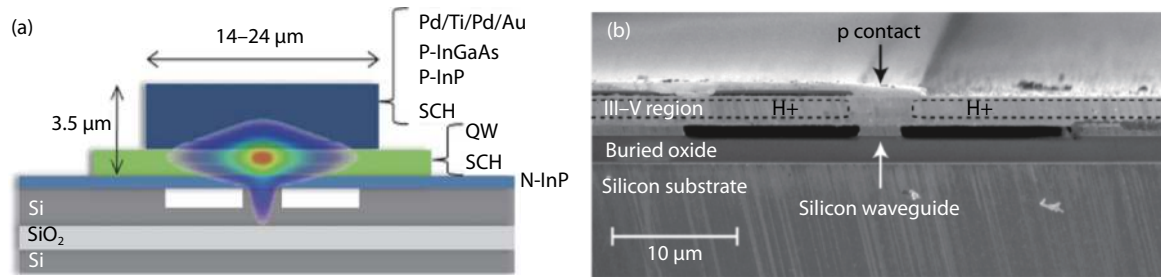Fig. 1. (Color online) (a) Schematic of the hybrid laser with the superimposed optical mode. (b) SEM of cross-section of the hybrid laser[21, 22].
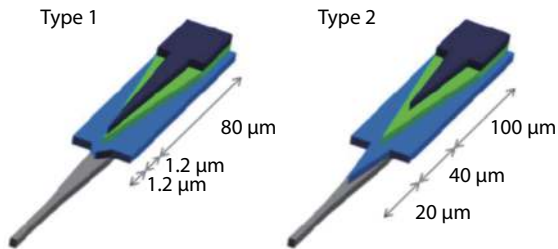

Fig. 2. (Color online) Schematic of mode conversion tapers for coupling light into the silicon waveguide. The silicon waveguide is in gray while different sections of the top III–V layer with different taper lengths are shown in other colors[22].

that eliminates the stringent alignment tolerance needs to have the laser cavity defined by a prefabricated silicon ridge.

Fig. 1 shows the schematic and scanning electron micrograph (SEM) cross section image of a hybrid III–V laser integrated on a silicon waveguide. The lasing mode is superimposed on the structure in Fig. 1(a). Electrical current flows from the p-contact, through the center of the mesa defined by proton implantation, to the n-contact, while achieving a large overlap with the optical mode. Light generated in the hybrid III–V/Si section is coupled completely into the underlying silicon waveguide via adiabatic multi-level tapering of the III–V epi, as shown in Fig. 2. In Ref. [22], the authors investigated two types of multilevel tapers as shown in Fig. 2. In Fig. 2, the top InP cladding layer of the III–V laser is indicated in blue, the active region of the III–V material is indicated in green, the bottom cladding of the III–V laser and bonding layers are drawn in cyan while the bottom silicon layer is drawn in grey. The chosen designs were made to reduce loss and reflection, and also support fewer higher order modes for efficient light confinement in the fundamental mode. The taper architecture in Fig. 2(a) transferred the power from III–V to silicon more abruptly than the taper design in Fig. 2(b), which was manifested in a higher taper loss in the design in Fig. 2(a) (~0.5 dB).

Another method popularly adopted in the literature for the hybrid integration of III–V lasers, semiconductor optical amplifiers (SOAs) and III–V photodetectors is micro-transfer printing. Micro-transfer printing (μTP) is a revolutionary heterogeneous integration technology with a high degree of modularity and flexibility[19, 20, 23]. μTP not only enables the fabrication of photonic heterogeneously integrated systems that are orders-of-magnitude smaller and more dense, but are also not limited to the number of different types of functionalities (i.e., μChiplet functions, materials, shapes, and sizes) that can be incorporated in an intermingled circuit design on a single substrate. The ability of a custom stamp to simultan-

eously transfer devices of varying sizes ensures that gain blocks of varying sizes can all be incorporated into a single PIC. Overall, μTP has been shown to be an efficient, flexible, high-yield, and high-quality process for placement of optical devices on photonic integrated circuits.

The principle of micro-transfer printing of III–V gain material onto a silicon passive platform on >8-inch wafer-scale in this program is illustrated in Fig. 3. A poly-dimethyl siloxane (PDMS) stamp with a post array (or a single post) whose size and pitch match those of the device array arranged on the source III–V wafer, is used to pick up and transfer these devices onto a target wafer. The stamp is fabricated through casting PDMS on a Si master mold and after releasing, laminating it on a glass carrier wafer. Over 300 000 printing cycles[19, 20] have been demonstrated with such stamps. Details of the fabrication steps and experimental data from prototype devices are presented in Ref. [19]. However, similar to the bonding method, a properly designed adiabatic taper is critical to the efficient coupling of power from the active III–V section to the passive silicon region.

The principle of coupling light from the III–V to the silicon section is governed by the supermode theory of the coupled III–V and silicon waveguides presented by Yariv *et al.* in Ref. [11]. According to this theory and as shown schematically in Fig. 2, it is possible to couple light from the top III–V waveguide to the bottom Si waveguide section simply by tapering the widths of the individual waveguides. As shown in Fig. 4, the upper III–V core-cladding combination and the lower silicon waveguide core with SiO_2 cladding form a system of two coupled vertically offset waveguides that are separated by the bonding interface. Such a coupled system of waveguides support two modes with propagation constants β_1 and β_2 respectively and designated by subscripts odd (o) or even (e) based on their modal symmetry when $\delta = \beta_1 - \beta_2 = 0$.

As observed in Fig. 4, by changing the δ parameter by controlling the widths of the individual waveguides as schematically illustrated in Fig. 2, the particular waveguide whether III–V or silicon in which the odd or even mode field is concentrated is determined. For the even supermode, in one roundtrip, light starts in the III–V waveguide where it is amplified, enters the adiabatic transformer section where δ changes from $\delta < 0$ to $\delta > 0$ by increasing the Si waveguide width and simultaneously decreasing the III–V width thereby transferring the mode energy to the bottom Si waveguide where it is partially reflected towards the left high reflection coating facet on the left of the III–V waveguide, thereby completing one roundtrip. The odd mode E_0 being primarily confined in the lower silicon waveguide in the lasing section on
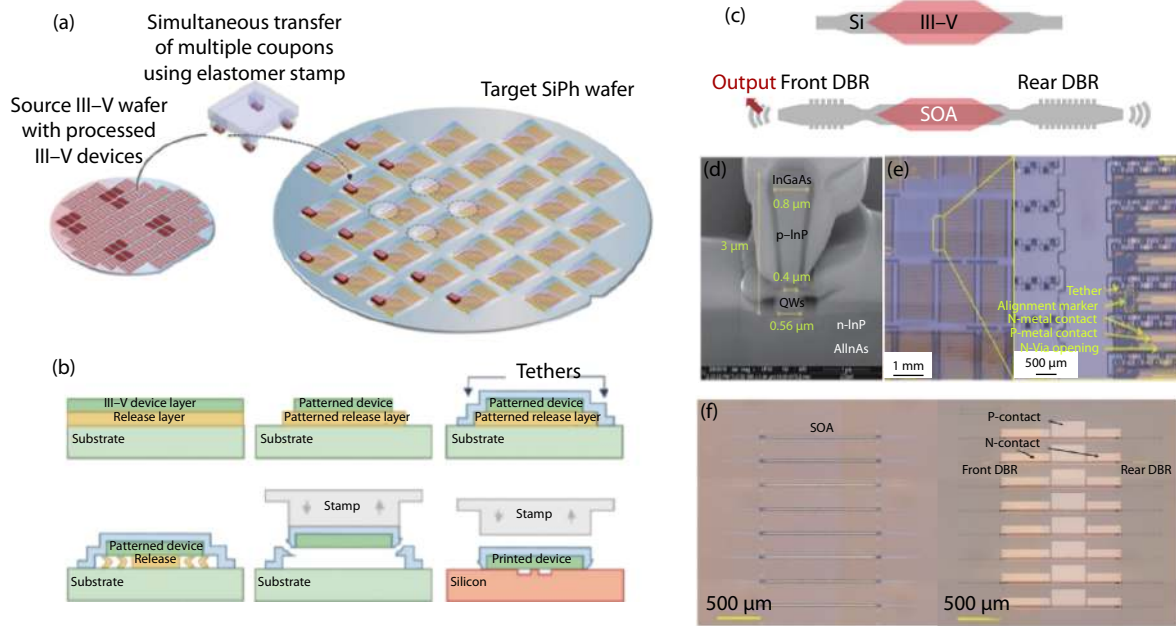
Fig. 3. (Color online) (a, b) Schematic Illustration of micro-transfer printing of III–V gain material on silicon wafers[19]. (c) Schematic integration and (d) SEM image of the III–V coupon with a silicon photonic waveguide. Top view microscope images of (e) large scale transfer printed coupons on a silicon photonic circuit, and (f) a semiconductor optical amplifier (SOA)[15].
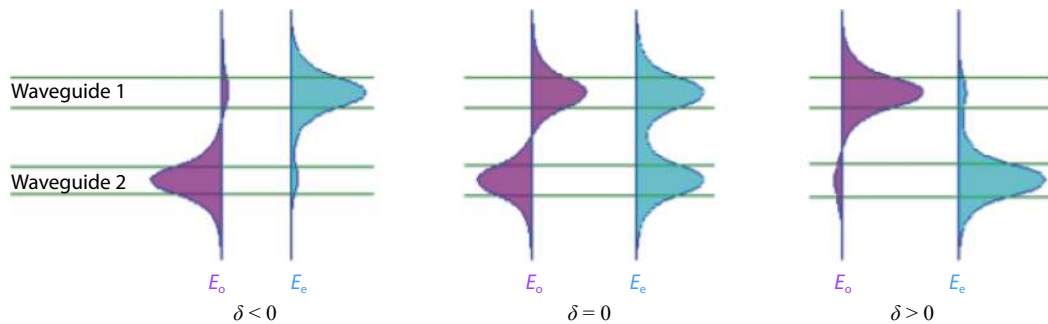

Fig. 4. (Color online) Schematic representation of the two supermodes, designated by E_o and E_e in the (left) lasing section (middle) coupling section and (right) passive waveguiding section[11].

the left image in Fig. 4, has a high lasing threshold and is thus prevented from lasing.

IMEC's iSiPP50G platform has silicon ridge waveguides of thickness 220 nm with demonstrated propagation loss ~0.3 dB/cm. For efficient coupling from III–V to silicon via the adiabatic tapering concept illustrated in Fig. 4, it is necessary to have an intermediate poly-Si interface of thickness 160 nm, which is also available in the iSiPP50G process, as shown in Figs. 5(a) and (b). The lower waveguide in Fig. 5 is essentially 160 nm of poly-Si (in green) on 220 nm device silicon (in purple) in a SOI wafer. Figs. 5(A)–5(H) shows the evolution of the optical mode from a typical laser epi stack in the O-band to the underlying poly-Si/Si waveguide, with the corresponding cross-sections at which the mode profiles are obtained being shown in Fig. 5(b). The III–V epi section can be patterned into a ridge laser with air cladding or a buried heterostructure laser with Fe:InP cladding when high power is desired. As noted in Figs. 6(a) and 6(b), in both configurations, Eigen-Mode Expansion (EME) simulations in the Lumerical MODE indicate that the coupling taper length increases with increasing thickness of the III–V cladding region separating the III–V core region from the poly-silicon surface. Simulations were

also performed for various ridge widths in the buried heterostructure configuration, as shown in Fig. 6(c). Once light is coupled into the passive poly-Si/silicon region, as shown in Fig. 7(a), the poly-Si layer is tapered to couple the even mode to the fundamental transverse electric (TE) mode in the silicon passive waveguide, as shown in Fig. 7(b). IMEC's iSiPP50G platform also enables co-integration of silicon and silicon nitride waveguides. Fig. 7(c) shows that by suitably designing the taper in both silicon and silicon nitride in opposite directions, the fundamental TE mode can be coupled entirely from the silicon with 220 nm thickness to 400 nm silicon nitride thickness, separated by an oxide thickness ~200 nm.

The hybrid integration scheme of the III–V gain section to silicon passives offers a significant device processing advantage compared to III–V lasers. As shown schematically in Fig. 3(c), front and rear distributed Bragg reflector (DBR) gratings can be defined in the silicon in standard CMOS processing to define Bragg reflectors with any desired reflectivity. Figs. 8(a) and 8(b) shows a typical reflectivity spectra for a different number of grating periods and tooth depths. In addition, hybrid integration allows the Bragg grating tunable sections in III–V lasers from the gain region. Fig. 8(c) shows typic-
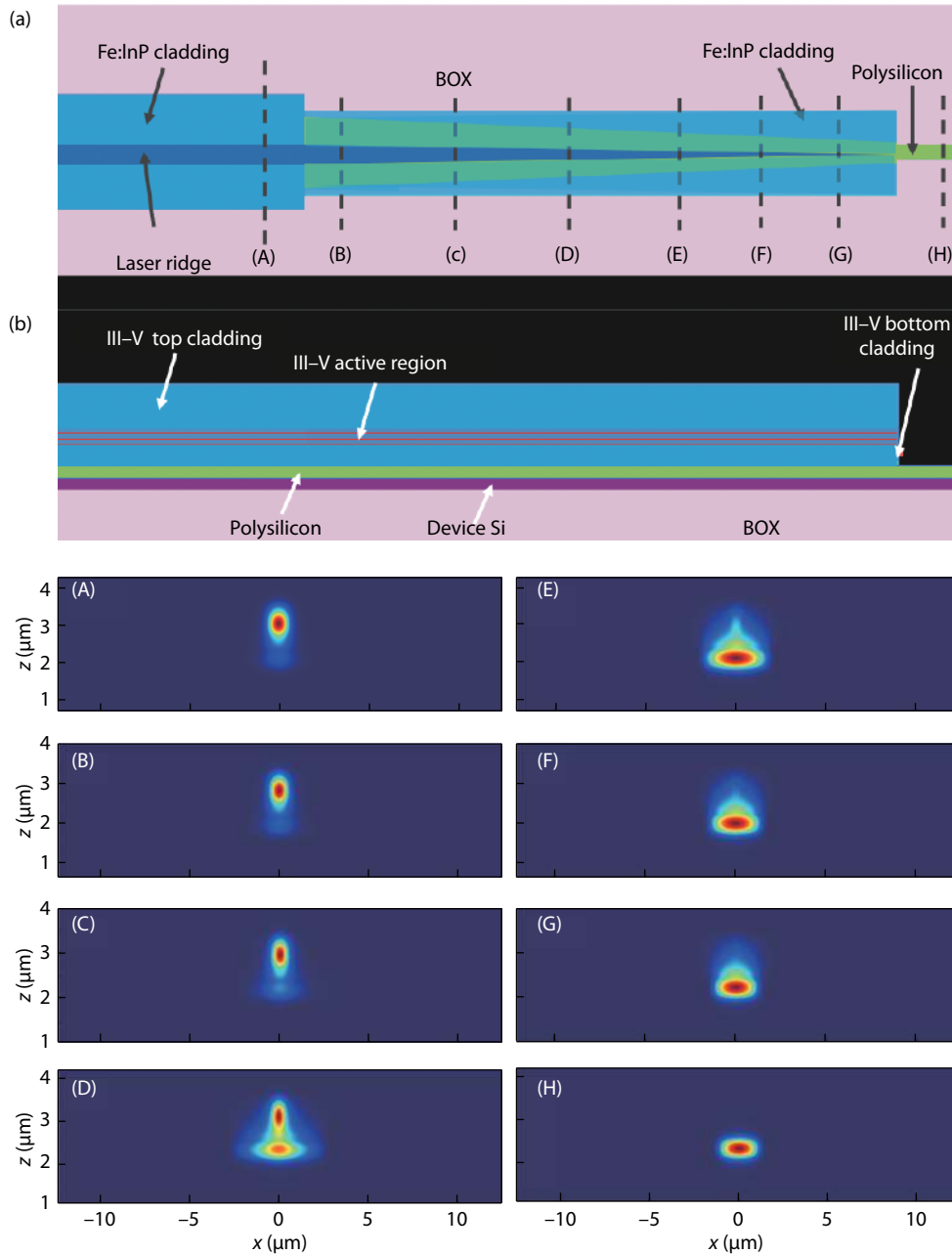
Fig. 5. (Color online) Schematic (a) top view and (b) side view of the III–V light emitting heterostructure with Fe:InP cladding in the buried hetero-structure configuration integrated on a SOI wafer with an intermediate polysilicon layer (in green). A dual taper configuration is shown in the adiabatic mode transformation region where the laser ridge as well as the underlying polysilicon layers are tapered. The mode evolution of the fundamental TE mode from the gain region to the underlying silicon-poly-Si waveguide is shown in (A)–(H) with the corresponding cross-sections demarcated in (b).
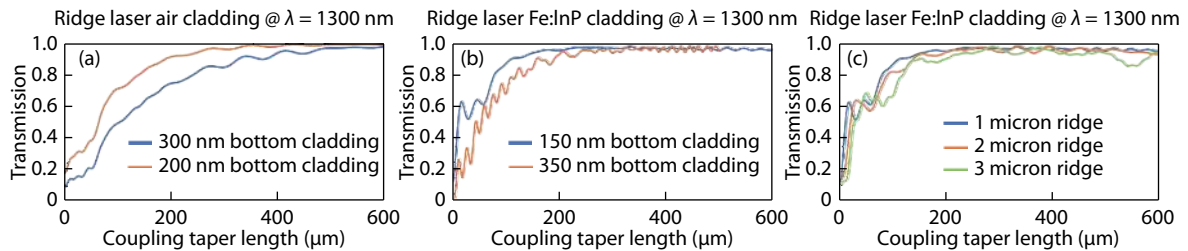

Fig. 6. (Color online) Coupling efficiency vs taper length as function of bottom cladding thickness for (a) air clad ridge laser and (b) buried heterostructure laser and (c) as a function of buried ridge width.

al tunable spectra from a system of two coupled Vernier ring resonators in the O-Band. Individual ring resonances can be thermo-optically tuned to tune the lasing wavelength of the hybrid laser. Similar demonstrations have been done in the
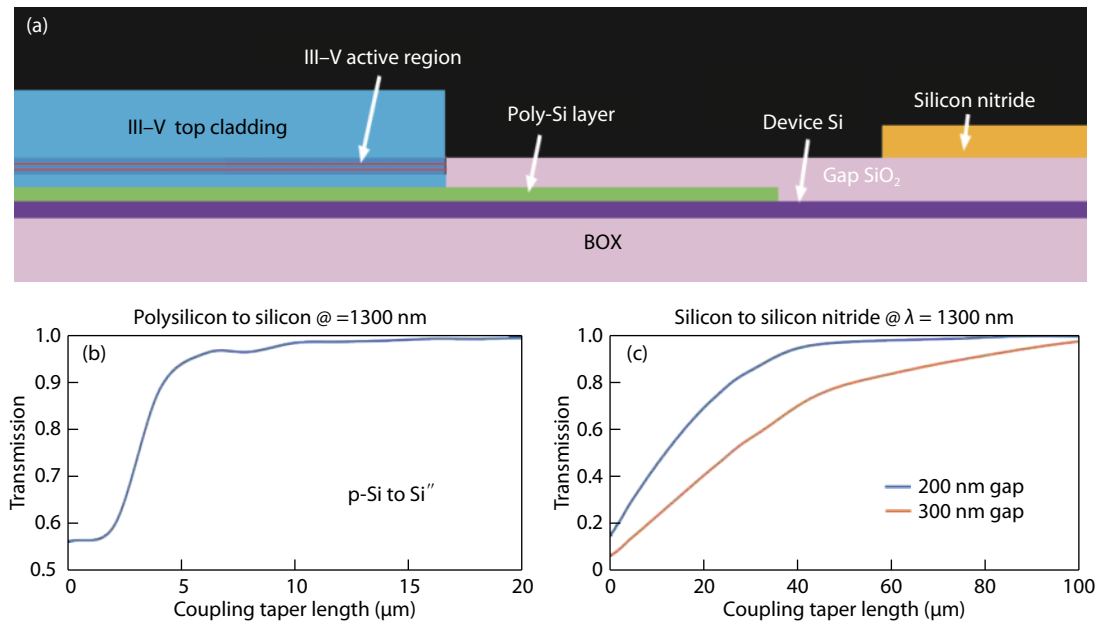
Fig. 7. (Color online) (a) Schematic cross-section of the hybrid laser/light emitter bonded to polysilicon (in green) on device silicon (in purple). Coupling efficiency versus taper length for coupling from (b) poly-Si to 220 nm silicon, and (c) from 220 nm silicon to 400 nm silicon nitride for various oxide gaps between silicon and silicon nitride as indicated in (a).
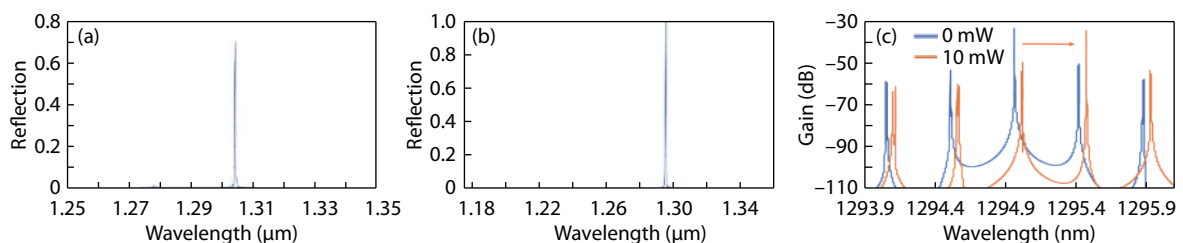

Fig. 8. (Color online) Reflectivity spectra of DBR reflectors for gratings with (a) etch depth of 100nm and 3600 periods with period $\Lambda = 207$ nm, (b) etch depth of 30nm and 7200 periods with $\Lambda = 207$ nm. (c) Vernier coupled ring spectra showing thermo-optic tuning around $\lambda = 1295$ nm.

C-band in Ref. [14].

3. Ferroelectric modulator integration with silicon PICs

Heterogeneous integration techniques have led to the emergence of ultra-compact thin-film lithium niobate (TFLN) electro-optic (EO) modulators on silicon substrates. Several high performance TFLN EO modulators with 3 dB bandwidths up to ~100 GHz have been demonstrated[24]. Simulations showing feasibility of achieving 3 dB bandwidths up to 400 GHz have been reported. In contrast, the modulation bandwidth of silicon modulators is inherently limited by carrier mobility in silicon. The best reported 3 dB bandwidths in Ge–Si electro-absorption modulators (EAMs) is ~74 GHz[25]. To achieve data rates ~1.6 Tb/s with DP-16QAM, a 3 dB RF bandwidth ~115 GHz is needed which is very much feasible with ferroelectric integrated modulators on Si PICs. Furthermore, nonlinear modulation and high loss due to free carrier absorption and two-photon absorption limit the power handling capability of doped and undoped silicon waveguides. Hybrid integration of TFLN with silicon or silicon nitride overcomes the inherent drawbacks of plasma dispersive silicon modulators.

Various TFLN hybrid integration strategies have been reported in the literature. While etched LN on lithium-niobate-on-insulator (LNOI) wafers are being demonstrated elsewhere, Figs. 9(a) and 9(b) show schematics of two architectures for integration of unetched slab TFLN with embedded and un-embedded electrodes respectively.

The steps in the fabrication/hybrid integration of TFLN with silicon waveguides and embedded electrodes have been reported in Ref. [27]. In Fig. 10, we show the steps in the hybrid integration with electrodes not embedded in the silicon PIC.

The silicon or silicon nitride waveguides in Mach–Zehnder interferometer configurations, with grating couplers and other passive waveguide components, are patterned in a full wafer or multi-project wafer (MPW) which runs in a standard 200 or 300 mm foundry using 193 nm lithography. The patterned die/wafer is planarized with silicon dioxide (SiO_2) to have a surface roughness compatible with high yield bonding as shown in Fig. 1(d). Thin film lithium niobate on insulator (LNOI) wafers are cut into dies of sizes compatible with modulator lengths (~5 mm to 2 cm) followed by deposition of SiO_2 and polishing for a die–die bonding compatible surface as shown in Fig. 1(e). Since LN is not a foundry compatible material, subsequent post-processing is done in a custom semiconductor microfabrication facility with steps involving the removal of the silicon handle and SiO_2 from the LNOI die [Figs. 1(h) and 1(i)] and traveling wave modulator (TWM) elec-
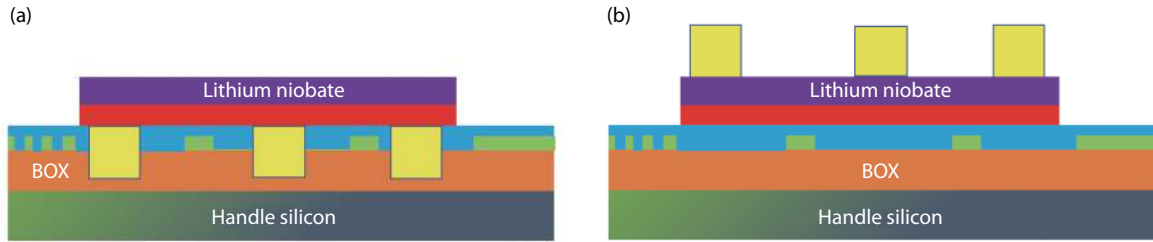
Fig. 9. (Color online) Schematic of hybrid TFLN integrated with silicon PICs with (a) embedded electrodes[26] and (b) un-embedded electrodes. Legend: (yellow) electrodes/metal contacts; (green) silicon or silicon nitride waveguides; (blue) silicon dioxide; (purple) thin film lithium niobate; (red) bonding interface with silicon dioxide between lithium niobate and top of silicon/silicon nitride waveguide.
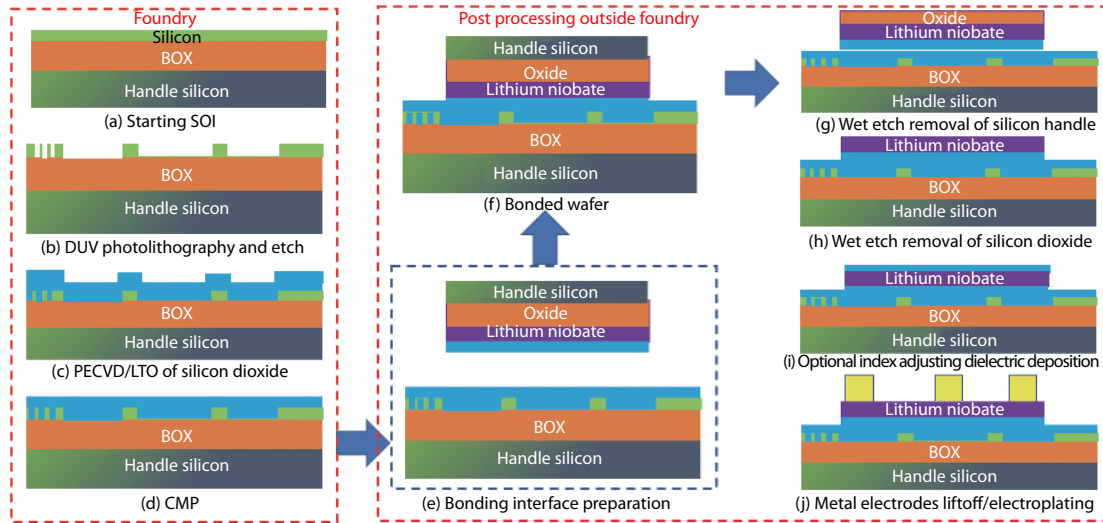

Fig. 10. (Color online) Steps in the hybrid integration of TFLN on silicon or silicon nitride PICs.
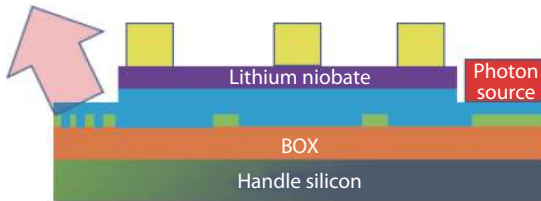

Fig. 11. (Color online) Steps in the hybrid integration of a III–V laser with silicon in a hybrid TFLN on silicon or silicon nitride PIC.

trode definition by metal-lift-off [Fig. 1(j)].

A III–V gain medium can be bonded or transfer printed either before or after the metal lift-off step, as shown in Fig. 11, wherein the silicon or silicon nitride waveguides in those sections are adiabatically tapered as described in Sec. 2 to achieve full integration. One may note that the grating coupler output in Fig. 11 can be substituted by integrated photodetectors that receive light guided by the silicon/silicon nitride waveguides via adiabatically tapered waveguides.

For EO modulators, a few significant parameters of interest are the 3 dB RF bandwidth, the $V\pi$-L, the RF propagation loss and the optical waveguide propagation loss along with other metrics such as insertion loss, ripple, temperature dependence etc. In both structures with embedded and un-embedded electrodes shown in Fig. 9, the bonding interface is shown in red and is a significant determining factor for the $V\pi$-L parameter. Fig. 12 shows a typical refractive index profile and mode profile for a 400 nm thin LN slab on a 220 ×

200 nm² silicon nitride waveguide, separated by an oxide bonding interface ~50 nm.

As observed in Fig. 12, the optical mode profile in the modulator section spreads in the slab lithium niobate. While alternate designs with etched LN strongly confines the mode, as will be shown later in Fig. 14, we observe from Tables 1 and 2 in Fig. 13 that the optical overlap integral with the adjacent electrodes and the consequent proximity induced optical loss sets a lower limit to the minimum distance between the ground and signal electrodes in the traveling wave modulator. By setting this lower limit as 1 dB/cm, we observe that the thickness of the gap interface oxide, indicated in red in Fig. 9, plays a significant role such hybrid integration.

From a fabrication standpoint, an oxide interface gap of dimensions shown in Fig. 13 imposes stringent bonding interface requirements. With an oxide interface gap of 50 nm between the top of the silicon and the bottom of the TFLN, a minimum spacing of 10 μm is required between the ground and signal electrodes, so that the optical propagation loss (excluding the material loss, surface roughness loss) simply due to the overlap of the optical mode with the electrodes is less than 1 dB/cm. Simulations indicate that the $V\pi$-L increases to 3.28 and 3.92 V·cm respectively for embedded and unembedded electrodes case, versus ~2 V·cm which would have been possible if the electrodes were 5 μm apart. While details will be covered elsewhere, it may be noted that the RF loss is higher and RF bandwidths significantly lower in the case with embedded electrodes versus unembedded electrodes.
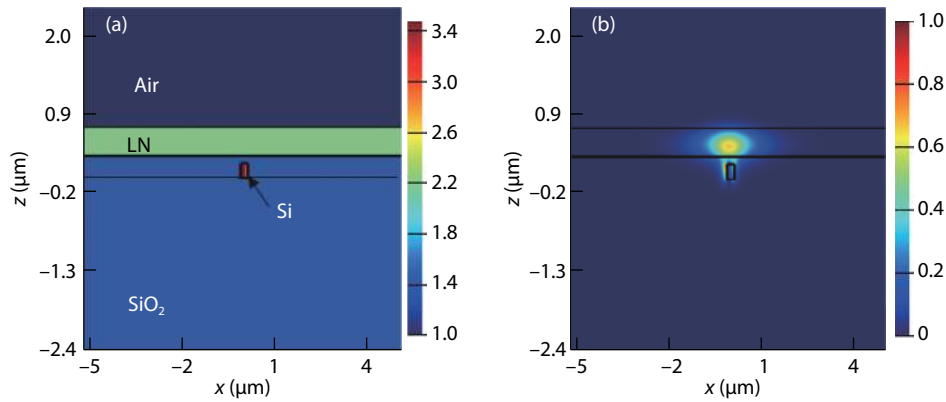
Fig. 12. (Color online) (a) Refractive index profile and (b) optical mode profile of the fundamental TE mode in a thin film ~400 nm LN bonded to a silicon waveguide 240 × 220 nm² separated by 100 nm SiO₂ interface. The top cladding is air.

(a)

dB/cm	Optical loss metal Cu for different electrode gaps					
Gap	4 µm	5 µm	6 µm	8 µm	10 µm	12 µm
0 nm	2.427	0.198	0.018	1.5×10^{-4}	1.3×10^{-6}	1.07×10^{-8}
25 nm	1138	203	35	1.125	0.035	0.001
50 nm	2692	637	149	8.47	0.47	0.027

(b)

dB/cm	Optical loss metal Cu for different electrode gaps					
Gap	4 µm	5 µm	6 µm	8 µm	10 µm	12 µm
0 nm	1.42	0.12	0.015	8.8×10^{-5}	7.5×10^{-7}	6.3×10^{-9}
25 nm	802	142	24	0.787	0.025	7.9×10^{-4}
50 nm	2548	602	141	8.01	0.45	0.025

Fig. 13. (Color online) Tables indicating optical propagation loss contribution from the overlap of the propagating optical mode with the ground and signal electrodes as a function of interface oxide thickness (vertical axis) and spacing between ground and signal electrode (horizontal axis) for hybrid traveling wave modulator configuration with (a) an embedded electrode and (b) an un-embedded electrode.

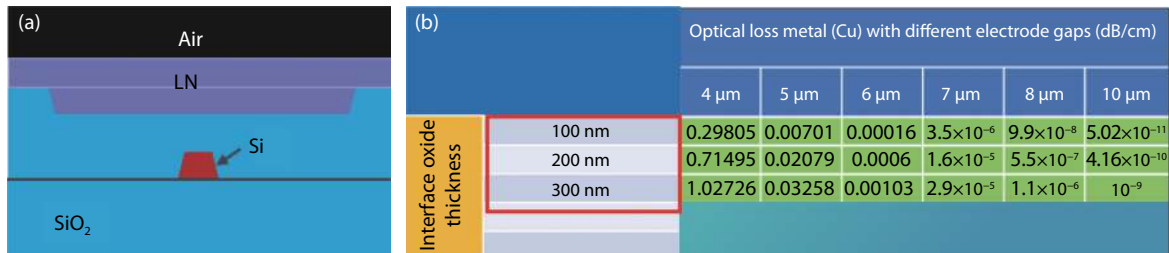| Interface oxide thickness	Optical loss metal (Cu) with different electrode gaps (dB/cm)					
	4 µm	5 µm	6 µm	7 µm	8 µm	10 µm
100 nm	0.29805	0.00701	0.00016	3.5×10^{-6}	9.9×10^{-8}	5.02×10^{-11}
200 nm	0.71495	0.02079	0.0006	1.6×10^{-5}	5.5×10^{-7}	4.16×10^{-10}
300 nm	1.02726	0.03258	0.00103	2.9×10^{-5}	1.1×10^{-6}	10^{-9}

Fig. 14. (Color online) (a) Cross-section schematic of etched LN integrated with silicon PIC. (b) Optical propagation loss contribution from the overlap of the propagating optical mode with the ground and signal electrodes as a function of interface oxide thickness (vertical axis) and spacing between ground and signal electrode (horizontal axis) for hybrid traveling wave modulator configuration.

It is possible to overcome the stringent oxide thickness limitations with TFLN slab structures presented previously, however, that will be the subject of a different paper. Another option to overcome such stringent limitations is to bond an etched LN film in Fig. 10(e) in which case, the cross-section profile of the bonded etched LN film in the modulator section is as shown in Fig. 14.

As observed in Fig. 14, the interface oxide thickness stringency is significantly relaxed whilst also enabling ground-signal electrode spacing ~4 µm thereby enabling low Vπ-L.

In such hybrid architectures, light initially coupled into a silicon or silicon nitride waveguide via grating couplers (as shown in Fig. 12) is coupled to the etched LN film by adiabatic tapering of both the silicon waveguide and the TFLN so that nearly 100% light is coupled for propagation in the rib etched LN over a coupling length ~100 µm. In Fig. 15, a fraction of the propagating mode in the modulator section is still in the silicon; however one can taper the silicon waveguide width to zero in which case the mode would reside entirely in the rib etched LN.

The adiabatic tapering architecture is also robust to misalignment. As demonstrated elsewhere with respect to the transfer printed alignment of III–V lasers to a passive silicon waveguide, we observe in Fig. 16 the simulated optical mode profile for ~500 nm misalignment while bonding the etched LN to the silicon PIC. We observe in Fig. 16 that nearly 100% of the propagating optical mode initially in silicon can be coupled to the etched TFLN film bonded above, the misalignment offset being accounted for during fabrication by a slightly longer taper length ~500 µm.

4. Conclusion

In summary, in this paper, we have reviewed the basic principles of hybrid integration of different materials with silicon PICs, to attribute functionalities unachievable in silicon or Group IV semiconductors alone. III–V materials have been efficiently integrated with silicon by various methods including bonding and transfer printing to function as gain media for
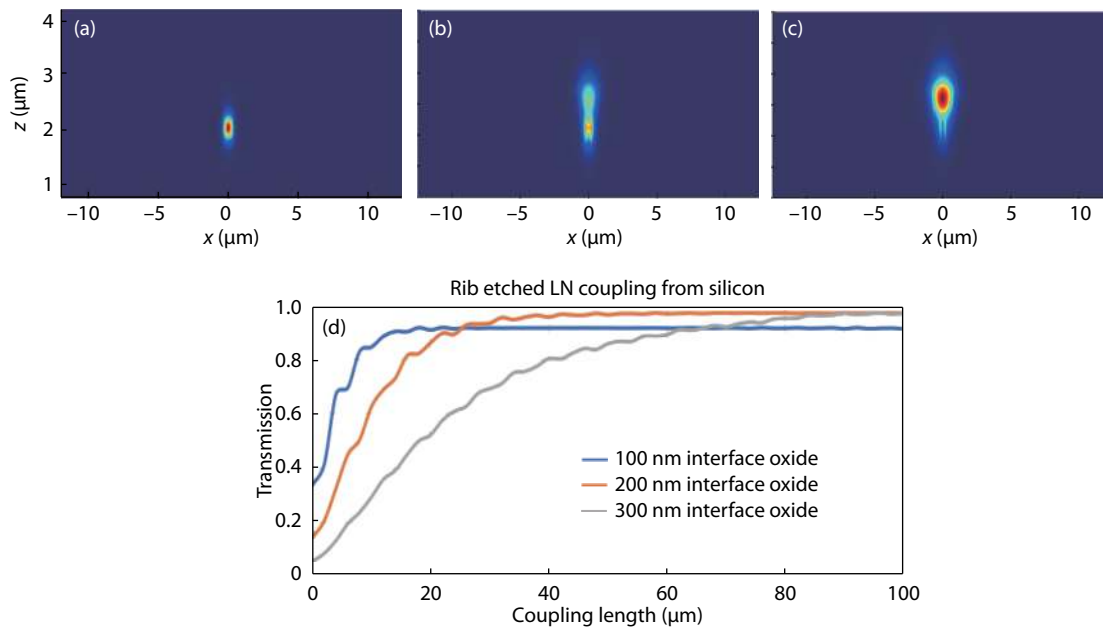
Fig. 15. (Color online) Evolution of the optical mode as it couples from the silicon to the etched TFLN in Fig. 14(a) in (a) initially in silicon (b) adiabatic coupling section and (c) mode primarily in the TFLN in the modulator section. (d) Coupling efficiency as a function of adiabatic taper length for different thicknesses of the interface oxide.
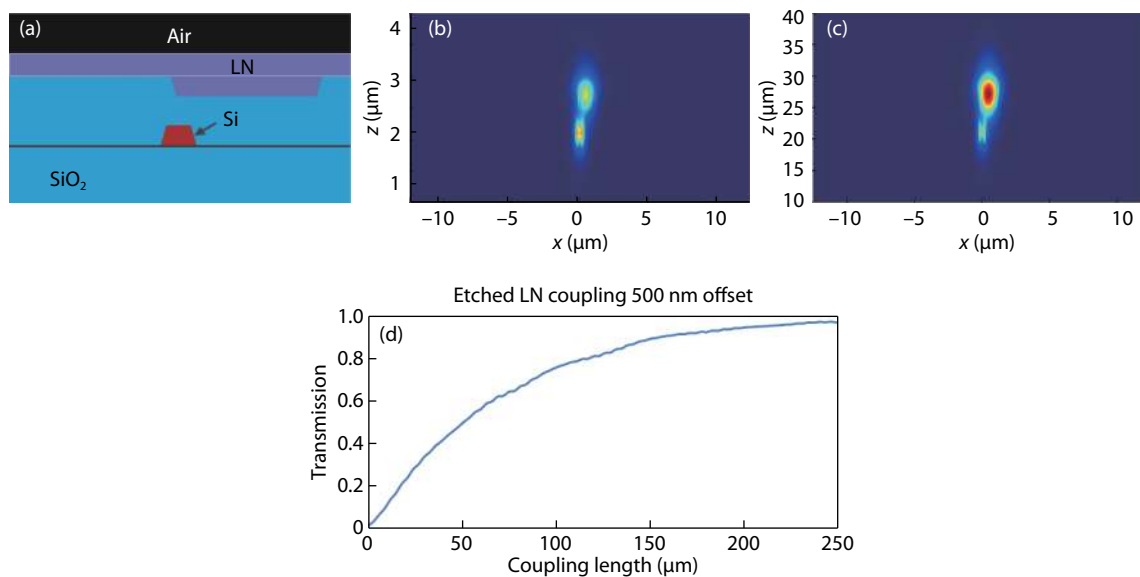

Fig. 16. (Color online) (a) Schematic cross-section assuming the TFLN slab has a misalignment offset of 500 nm perpendicular to the waveguide, when bonding. Mode profiles in the (b) adiabatic coupling section and (c) TFLN in the modulator section. (d) Coupling efficiency as a function of adiabatic taper length when waveguides are misaligned.

lasers and SOAs, and as efficient photodetectors. While III–V materials are also promising candidates as modulators by virtue of their linear and non-linear electro-optic characteristics, low-loss ferroelectric modulator integration with silicon PICs is also reaching advanced maturity. In addition to thin film lithium niobate (TFLN) referenced here, similar efforts are ongoing at IMEC and elsewhere towards integration of barium titanate (BTO) that have demonstrated superior EO-coefficients[9], comparable to in-device EO coefficients demonstrated with EO polymers[10]. It is worthwhile to note that EO polymers have shown superior RF performance recently in plasmonic waveguide architectures[28, 29]. While EO polymers are potentially strong candidates as standalone modulators once ques-

tions surrounding polymer shelf life and reliability are addressed[10, 28, 29], integration challenges and the large propagation loss associated inherently with plasmonic waveguides precludes integration in large circuits needed for computing and transceiver applications. Adiabatic transformation of modal energies between the hybrid materials provides a generalized strategy for efficient coupling of light between different integrated hybrid materials on chip.

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