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Integration of GaN analog building blocks on p-GaN wafers for GaN ICs

Xiangdong Li[1, 2, †], Karen Geens[1], Nooshin Amirifar[1], Ming Zhao[1], Shuzhen You[1], Niels Posthuma[1], Hu Liang[1], Guido Groeseneken[1, 2], and Stefaan Decoutere[1]

[1]imec, Leuven 3001, Belgium

[2]Department of Electrical Engineering, KU Leuven, Leuven 3001, Belgium

Abstract: We demonstrate the key module of comparators in GaN ICs, based on resistor-transistor logic (RTL) on E-mode wafers in this work. The fundamental inverters in the comparator consist of a p-GaN gate HEMT and a 2DEG resistor as the load. The function of the RTL comparators is finally verified by a undervoltage lockout (UVLO) circuit. The compatibility of this circuit with the current p-GaN technology paves the way for integrating logic ICs together with the power devices.

Key words: p-GaN; resistor-transistor logic (RTL); comparator; undervoltage lockout (UVLO); GaN ICs

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1. Introduction

GaN power ICs bear significant advantages over the discrete solution, namely reduced chip size, suppressed parasitic inductance, and simplified circuit designing[1]. A lot of effort has been made to realize all-GaN power ICs. In 2009, Panasonic Corporation first demonstrated a GaN monolithic motor-drive inverter IC on a Si substrate, consisting of three integrated half-bridges[2]. Specific gate driver designs have also been investigated to provide a high driving capability and a low power dissipation[3, 4]. Previously, at imec we have successfully eliminated back-gating effect by trench isolation on engineered substrates, based on which the 200 V half-bridge with on-chip drivers have been integrated[5–11].

Moreover, analog building blocks such as protection and diagnostic circuits are also obligatory. A comparator, the core block of analog ICs, is of paramount importance and has been demonstrated on D-mode epitaxy wafers[12]. However, the mainstream p-GaN technology requires the co-integration on E-mode epitaxy wafers. The lack of a pFET also imposes challenges to the circuit design. In this work, a comparator based on resistor-transistor logic (RTL) gates will be demonstrated on E-mode wafers and the function verified by a undervoltage lockout (UVLO) circuit.

2. Epitaxy and fabrication

This work commenced with device stack epitaxy using a MOCVD reactor on 200 mm SOI substrates, as shown in Fig. 1. The schematic cross-section is illustrated in Fig. 2(a). The epi stack consists of a 200 nm AlN nucleation layer, a 2.15 μm (Al)GaN buffer layer, a 400 nm GaN channel layer, a 12.5 nm $Al_{0.235}GaN$ barrier layer, and an 80 nm Mg-doped p-GaN layer. An in-situ annealing of the p-GaN layer was conducted in N_2 ambient after the epitaxy to activate the Mg dopants. Delicate strain engineering was carried out in order to control the stress during the epitaxy and to avoid excessive wafer warp. The optimized epi stack showed a high structural quality with wafer warpage well below 50 μm and a smooth surface.

The devices were processed using imec's 200 mm CMOS compatible process modules and the processing flow is sequentially detailed in Fig. 2(b)[13]. A TiN/p-GaN stack was used for the gate[14]. Nitrogen implantation was used for horizontal isolation. After the device fabrication, the trench isolation was processed by etching through the (Al)GaN/Si(111) to the SiO_2 buried layer. Afterwards, the trench was filled by SiO_2, followed by chemical mechanical polishing (CMP). The substrate contact was then processed by etching through the (Al)GaN to the Si(111) device layer, followed by Ti/Al sputtering for the power metal to connect the Si(111) with the source. Finally, a back-end passivation layer was deposited.

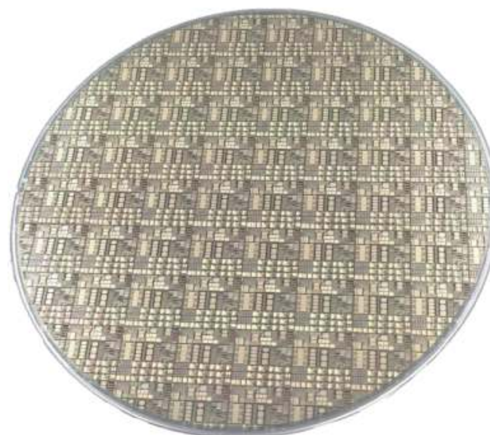

Fig. 1. (Color online) Fabricated 200 mm GaN-on-SOI wafer with CMOS-compatible processing.

Correspondence to: X D Li, lixiangdong28@126.com
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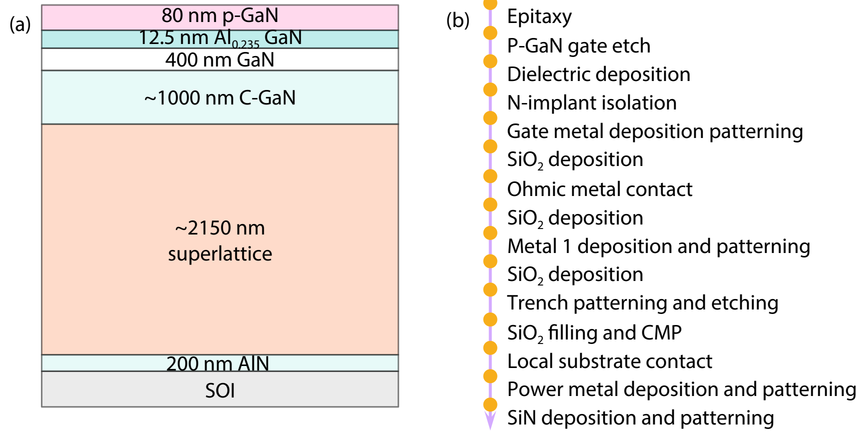

Fig. 2. (Color online) (a) Schematic cross-section of the epitaxial layer stack and (b) processing flow.

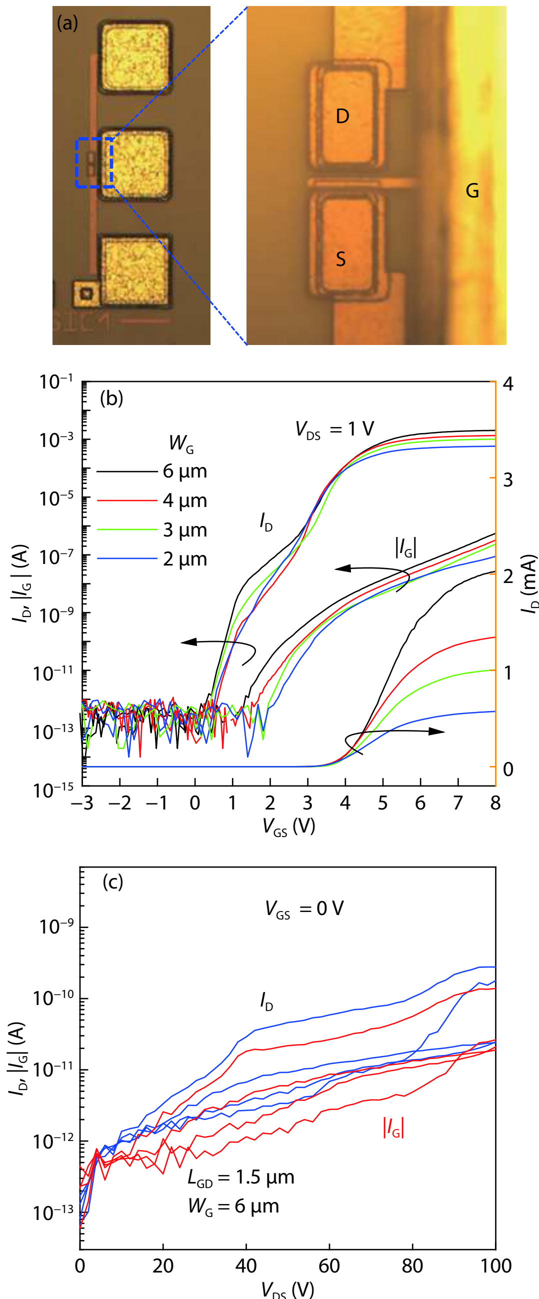

Fig. 3. (Color online) (a) Microscope images, (b) transfer characteristics, and (c) OFF-state leakage characteristics of the logic HEMTs with L_{GD} of 1.5 μm and W_G scaling from 6 μm to 2 μm.

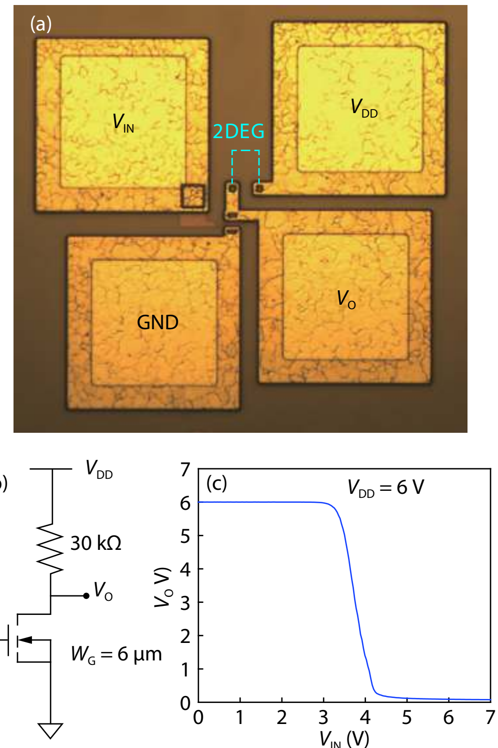

Fig. 4. (Color online) (a) Microscope image, (b) schematic, and (c) measured voltage transfer characteristic (VTC) of the integrated RTL inverter.

Currently, p-GaN gate HEMT technology cannot fabricate complementary devices. Therefore, our integration falls back to the RTL that uses a 2DEG resistor to replace the pFET. The 2DEG resistor was fabricated together with the HEMTs. The p-GaN layer was first removed, followed by dielectric deposition. Then the two terminals of a 2DEG resistor were contacted by ohmic contacts. The fabricated HEMTs feature a small W_G scaling down from 6 to 2 μm and a L_{GD} of 1.5 μm as shown in Fig. 3. The 2-μm-wide meander 2DEG resistor works as a load resistor in the ICs. The RTL-based comparator and UVLO circuits were designed using the PDK of Ref. [15].

3. Results and discussion

The processed logic HEMTs show a V_{TH} of ~ 3.6 V and I_{DS} scaling with W_G till 2 μm (Fig. 3(b)). The current bump on the I_D–V_{GS} curve at 1 V in Fig. 3(b) is stemming from the trapping

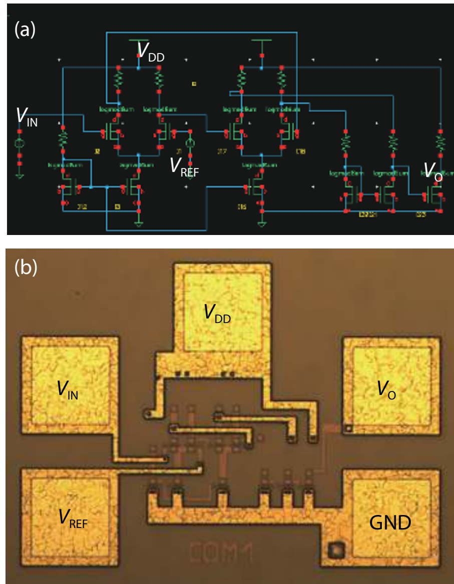

Fig. 5. (Color online) (a) Comparator designed by RTL and (b) the microscope image of the processed comparator.

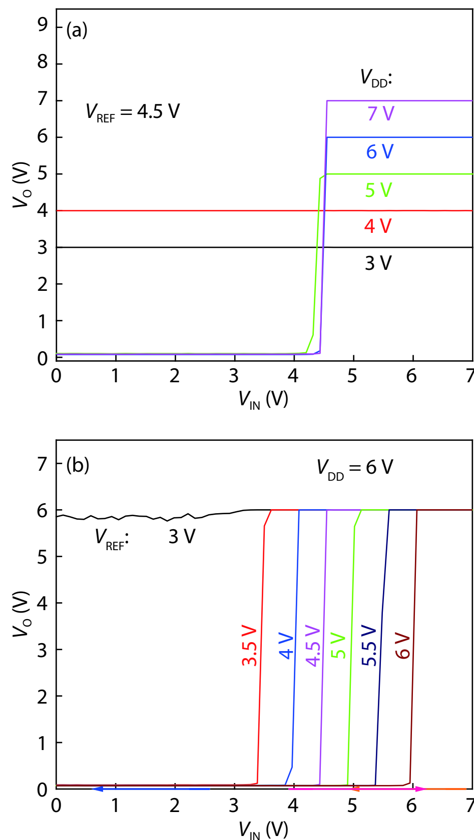

Fig. 6. (Color online) (a) Voltage transfer characteristics of the comparator with (a) various V_{DD} and (b) various reference voltage V_{REF}.

effect of the p-GaN layer. In detail, when the gate is positively biased, the traps get charged so that the V_{GS} will drop on the p-GaN layer instead of the channel, which induce the current bump. This phenomenon has been elaborated in our previous work[16]. The OFF-state breakdown voltage exceeds 100 V (Fig. 3(c)) with the pinch-off leakage below 1 nA. Fig. 4 demonstrates the processed RTL inverter including a 6-μm logic HEMT and a 30-kΩ 2DEG resistor, whose voltage transfer characteristic (VTC) is shown in Fig. 4(c). The output voltage V_{OL} reaches a very low value of 88 mV at V_{IN} = 6 V.

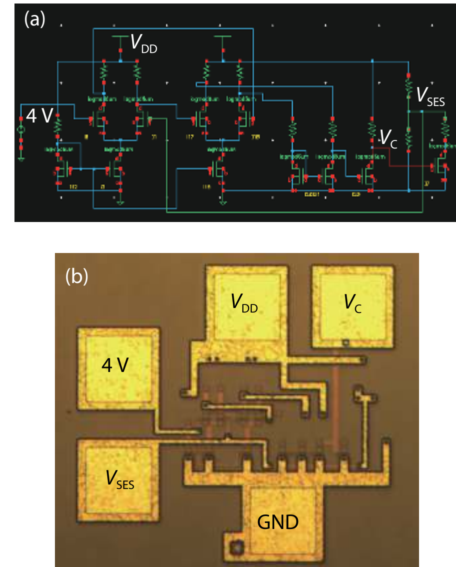

Fig. 7. (Color online) (a) Undervoltage lockout GaN circuit, (b) layout, and (c) voltage transfer characteristics show the IC shuts down when V_{DD} < 5 V and restarts when V_{DD} > 5.7 V.

Fig. 5 shows the comparator circuit and microscope image based on RTL inverters. Due to the lack of pFET, the gain, namely dV_O/dV_{IN}, of the RTL inverter is lower than that of the CMOS inverter, which is demonstrated by the smooth flipping curve in Fig. 4(c). To overcome this weakness, three-stage comparators are designed. In Fig. 6(a), a supply voltage V_{DD} ranging from 3 to 7 V was sequentially applied to the comparator and the input signal V_{IN} swept from 0 to 7 V. As can be seen, the comparator cannot work until the V_{DD} reaches 5 V, suggesting the supply voltage V_{DD} should be kept within 5 to 6 V, considering both the function and power dissipation. The basic function of this comparator is realized as shown in Fig. 6(b) where the V_O flips at the corresponding V_{REF}.

A UVLO circuit based on this comparator was further designed (Fig. 7(a)) and processed (Fig. 7(b)). UVLO is an electronic circuit used to turn off the power of an electronic device in the event of the voltage, battery charge for instance, dropping below the minimum operational value. Without this, logic functions may generate wrong control signals. Fig. 7(c) shows that when the V_{DD} gradually ramps down to 5 V, the protection circuit gives a shutdown signal; when the V_{DD} ramps up from 3 V, the IC restarts as V_{DD} reaches 5.7 V. This hysteresis design ensures the safe operation of the

power system.

4. Conclusion

In summary, the RTL analog building blocks on the p-GaN technology platform have been successfully processed. Logic p-GaN gate HEMTs compatible with the power ones demonstrated a scalable W_G down to 2 μm. The logic devices showed an excellent robustness with OFF-state breakdown voltage exceeding 100 V, with L_{GD} of only 1.5 μm. The elementary building block of comparators for analog circuits were successfully integrated, whose function was finally verified by the undervoltage lockout design. Integrating the analog circuits together with power devices can not only reduce system cost, but also can suppress the parasitic inductance of the interconnect between components so that it suppresses oscillation and boosts reliability. This work promises to pave the way for all-GaN smart power IC integration.

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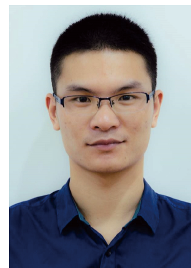

Xiangdong Li received the B.S and M.S. degrees in microelectronics from Xidian University, Xi'an, China, in 2013 and 2016, respectively, and the Ph.D degree with the Department of Electrical Engineering, Katholieke Universiteit Leuven, Leuven, Belgium, in 2020. From 2016 to 2020, he was also with the GaN Group, IMEC, Leuven, Belgium, as a Ph.D researcher. He focuses on GaN materials, devices, reliabilities, and circuits.