REVIEWS

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A review of silicon-based wafer bonding processes, an approach to realize the monolithic integration of Si-CMOS and III–V-on-Si wafers

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Abstract: The heterogeneous integration of III–V devices with Si-CMOS on a common Si platform has shown great promise in the new generations of electrical and optical systems for novel applications, such as HEMT or LED with integrated control circuitry. For heterogeneous integration, direct wafer bonding (DWB) techniques can overcome the materials and thermal mismatch issues by directly bonding dissimilar materials systems and device structures together. In addition, DWB can perform at wafer-level, which eases the requirements for integration alignment and increases the scalability for volume production. In this paper, a brief review of the different bonding technologies is discussed. After that, three main DWB techniques of single-, double- and multi-bonding are presented with the demonstrations of various heterogeneous integration applications. Meanwhile, the integration challenges, such as micro-defects, surface roughness and bonding yield are discussed in detail.

Key words: material; thin film; integrated circuit

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1. Introduction

The silicon (Si) complementary metal–oxide–semiconductor (CMOS) is the most dominant component in the semiconductor industry and the miniaturization of Si-CMOS is the main trend to further improve its speed, power consumption and production cost[1]. However, as the Si-CMOS is scaled to smaller devices, the issues of device reliability, such as short channel effects and random fluctuations, become more severe, and the lithography and etching processes are more complex and costly[2, 3]. As the benefits of scaling subside, the device's performance will be more and more materials-driven. Thus, the development of new materials systems, which are compatible with the Si-CMOS platform, can be the next generation of semiconductor technologies to break the bottleneck of Si-CMOS scaling.

The performance improvement of a transistor is driven by the carrier mobility enhancement in the channel. The Group IV materials, such as SiGe and Ge, and the Group III–V compound materials, such as GaAs and InP, are well-known for their unique electrical properties and superior high mobility transistors[4, 5]. In addition, most of the III–V materials have direct bandgaps and are commonly used as lighting materials for LEDs and lasers. Compared to III–V materials, Si is an indirect bandgap material and it is difficult to fabricate an efficient lighting device using Si. Therefore, III–V materials-based light sources are used as a hybrid solution in a silicon photonics platform for data transmission[6–10]. Meanwhile, this hybrid technology opens up numerous possibilities to develop new integrated circuit designs and applications in the fields of high-speed computation and sensing.

Epitaxial integration of growing III–V materials directly on Si substrates is the most desirable approach to integrate the III–V transistor with the Si platform. However, this method experiences many issues due to the large lattice mismatch and the difference in coefficient of thermal expansion (CTE) between the III–V compound semiconductor and Si. Thus, it remains a challenge to form thin III–V layers on Si while retaining excellent crystal quality. In addition, the growth of III–V materials requires a high temperature condition (650–1350 °C, depending on the materials systems).

Compared to the epitaxial integration method, direct wafer bonding (DWB) is a more straightforward and practical approach to achieve the heterogeneous integration between III–V and the Si substrate without the exposure of Si-CMOS to

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high temperature[11–13]. One of the most prominent applications of DWB is to make silicon-on-insulator (SOI) substrates, of which the technique can be extended to X-on-insulator substrates, such as Ge-OI, GeSn-OI, SiC-OI or other III–V-OI[14–18]. In addition, the wafer bonding technique enables separate wafer processing of III–V materials and CMOS in their respective foundries and then to be integrated at final stages. This separate processing method can avoid the cross-contamination between III–V materials and Si-CMOS in wafer processing tools in the Si foundries.

In Section 2 of this paper, several mainstream bonding techniques, including their applications and challenges, will be reviewed. In Section 3, our recent progress of single-, double- and multi-DWB bonding techniques will be discussed in detail. After that, various applications enabled by these techniques, such as CMOS-driven HEMT, LED, and other novel applications will be shown at the end of this paper.

2. Wafer bonding techniques

In this section, various mainstream approaches in wafer-scale bonding will be reviewed, including DWB, surface-activated bonding, thermocompression bonding, eutectic bonding, glass frit bonding, adhesive bonding and anodic bonding. Among these bonding techniques, the DWB is the most promising approach for wafer-scale III–V on Si integration and Si-CMOS integrated devices due to its strong bonding strength, reliable bonding interface and low temperature processing conditions. This section will present these bonding techniques in more details.

2.1. Direct wafer bonding

Heterogeneous integration technologies show great potential in the applications of novel materials, MEMS devices and 3D packaging. In the past, wire bonding, flip-chip and epitaxial integration were commonly used for heterogeneous integrations. However, due to the concerns of process complexity, scalability and materials quality, these integration applications were ruled out by the traditional materials science and semiconductor processing technology[19]. DWB has shown great potential for heterogeneous integration by directly bonding two similar or dissimilar materials and devices at the wafer-level. As a result, DWB has enabled numerous new applications, such as SOI, silicon-based sensors and actuators, and III–V optical and electrical devices[20]. Direct wafer bonding is also known as "wafer bonding" or "direct bonding", which was first proposed in 1985 by Lasky *et al.*[21]. It is known that when two materials with clean and flat surfaces are brought into intimate contact, the two materials will adhere and form bonds across the interface without the need of an intermediate layer[22]. The adhesion between two mating surfaces is through van der Waals interactions or hydrogen bridge bonds[19]. A similar phenomenon was also observed when two mirror-polished wafers were brought into close proximity, so that the wafers are directly bonded. As the strength of such adhesion is much weaker than covalent bond, annealing at high temperature is commonly applied after the room temperature pre-bond step to strengthen the wafer bonding. In the silicon-to-silicon direct hydrophilic bonding, good bond strength is only obtained with a high temperature anneal at above 800 °C. Such high temperatures are undesirable for many applications, especially for metallization and compound semiconductors. Fortunately, the anneal temperature can be significantly reduced with plasma-activated or other special wafer surface treatments. Meanwhile, the thermal stress is significantly reduced when lowering the annealing temperature, and the low temperature process also makes it compatible with back-end CMOS processing.

Besides annealing and plasma treatment, there are some stringent requirements in the process flow to ensure a successful wafer bonding, such as bonding energy, surface cleanliness, roughness and flatness. Firstly, the bonding is initiated by applying a physical force at one point on the wafer, allowing the bond front to propagate. The propagation of the bond front to a sealed interface is dependent on the balance between the surface energy dissipation to form the bond and the strain energy to deform the wafers[23]. Secondly, a clean surface is essential in wafer bonding processes[20]. The presence of organic and metallic contaminations and particles can affect the structural and electrical properties of the bonding interface. Therefore, the pre-steps of proper surface cleaning must be applied. Additionally, it is essential to ensure that the cleaning method will not cause severe surface roughening. The bonding surface cleaning method, named Radio Corporation of America (RCA) cleaning, is commonly used in the semiconductor industry. There are two hydrogen peroxide based steps: RCA1 or SC1 ($NH_4OH : H_2O_2 : H_2O = 1 : 1 : 5$) and RCA2 or SC2 ($HCl : H_2O_2 : H_2O = 1 : 1 : 6$). RCA1 is designed to remove the organic contaminants, especially hydrocarbon, by oxidizing action from H_2O_2 and solvating action of NH_4OH. Apart from RCA1, strong oxidizer periodic acid (H_5IO_6) can also be used to remove hydrocarbon residual at the wafer surface. RCA2 is aimed at removing metallic (ionic) contaminants. It is suggested to have a low ratio of NH_4OH for surface cleaning to avoid the surface roughening caused by the ammonia from RCA1. Due to this concern, UV/ozone cleaning and plasma treatments are also employed to treat the surface before bonding without degrading the surface[22]. Besides organic and metallic contaminations, particles can act as spacers, preventing intimate wafer contact and creating intrinsic voids. Since the presence of a small particle can result in a large void, ultraclean environment is preferred during wafer bonding. Thirdly, wafer surface roughness is another crucial parameter for DWB. It is suggested that if the root mean square (RMS) roughness is less than 1 nm, it poses no obstacles in DWB at room temperature via hydrogen bonds[20]. Fortunately, the current semiconductor technology is able to produce prime Si wafers with roughness less than 0.1 nm. The post-process surface roughening can also be reduced by a technique, named chemical-mechanical polishing (CMP). CMP polishes the surface at wafer-level to achieve the bonding required roughness level. Lastly, surface flatness is another important factor in DWB. By assuming the back surface is flat, the flatness is the deviation of the front surface to a reference plane, which can be quantified by the total thickness variation (TTV)[20]. TTV is defined as the height difference between the highest and lowest sites on the top wafer surface. If two wafers with different TTVs need to be bonded, they will be deformed into a common shape during the bonding processes[23]. If the TTV is small, the bonding can be successful by simply bringing two polished wafers into intimate contact at room temperature. When TTV is large, the gap

prevents the wafers from bonding, resulting in large unbounded areas. Though the deposition of nitride or metal layers on the wafer backside can introduce external stress to reduce the TTV, there is no established method to fully resolve this issue as it changes significantly with wafer materials, dimensions, layer structures and fabrication conditions.

When the wafers are bonded, bonding defects may exist, causing the failures of device fabrication in the later processing steps. Therefore, it is important to detect these bonding defects at early stages. One of the most commonly used methods is the IR imaging. As silicon is transparent at IR wavelength range (> 1.1 μm), the bonding defects, such as dark spots, interferential lines and voids, are visible under IR imaging. IR imaging is a fast and cheap method to detect bonding defects, but its resolution is limited. For small bonding defects, c-mode scanning acoustic microscopy (C-SAM) is a more efficient method compared to IR imaging. Acoustic wave propagates across the bonding structure and is reflected when meeting voids and bubbles. The reflections amplify the beam energy locally, and an acoustic image of the bonding defect is formed. In addition, the acoustic spectroscopy can also be used for bonding quality detection in metallic bonding, while metals are opaque to infrared radiation. Apart from these two non-destructive defect detection methods, wafer thinning is another approach to detect the defects. The bonded wafers are thinned down by etching until the bonding defects can be observed. This method provides an extra dimension in depth to visualize the bonding defects, compared to IR imaging and C-SAM.

2.2. Surface activated bonding (SAB)

In SAB, the bonding reaction is driven by the cohesive and adhesive energy of solids. Wafer surfaces are sputter-cleaned and activated with argon fast atom beam (FAB) before being brought into close contact in an ultrahigh vacuum (~10^{-5}–10^{-6} Pa) chamber. Then, large bonding pressure of a few tens of mega-pascal is applied to the close-contacted wafer pair. The bonding strength achievable at room temperature is close to the bulk fracture energy of the materials[24]. Hence, further heat treatment is not necessary in the surface activated bonding. Wafer-level room temperature bonding is applicable to dissimilar semiconductors, metals and insulators[24–28], and III–V optical and electronic device bonding have also been demonstrated without using the high temperature annealing process[27, 29]. Therefore, the potential damages by the annealing process, such as doping profile change, thermal stress induction, and new defect generation, can be eliminated. Additionally, experimental results from TEM and electrical conductivity measurements show that SAB enables oxide-free semiconductors and metal bonding interfaces[26, 29, 30]. This is very beneficial for stacked solar-cell and 3D integrations. However, some ionic materials, like glass to SiO_2 and SiO_2–SiO_2 show a polarized surface after FAB bombardment, which inhibits the bonding[31]. Another disadvantage of SAB is its restricted requirement of surface conditions, in terms of smoothness and flatness, which strongly affect the bonding results.

2.3. Thermocompression bonding

Thermocompression bonding, also known as diffusion bonding, is a metal-based bonding technique that brings two surfaces into atomic contact under heat and pressure. A smooth surface with high surface flatness is desirable as it promotes the interatomic attractions. Metals with a high diffusion rate are used in this bonding technique. The most commonly used metals are Au, Al and Cu[32–36]. They can be deposited through evaporation, sputtering or electroplating. A thin adhesion layer is deposited first, not only improving the adhesion strength, but also reducing the bonding temperature and pressure. Three mains steps in thermocompression bonding are metal film deposition, surface pre-treatment for organic and oxide removal, and bonding under heat and pressure. In Au–Au thermocompression bonding, a thin oxide diffusion barrier layer and Ti adhesion layer are deposited prior to Au layer deposition, in which the oxide layer is to block Si from diffusion into the Au surface. A successful wafer-level Au–Au bonding has been obtained at the bonding temperature of 300 °C and the compressive pressure of 7 MPa[33]. In Al–Al and Cu–Cu bondings, a slightly higher bonding temperature is required. The bonding temperature is in the range of 400–500 °C for Al–Al thermocompression bonding[32] and 250–400 °C for Cu–Cu bonding[35]. An increase in bonding pressure is necessary when reducing the bonding temperature is needed. Thermocompression bonding is a well-established wafer-level hermetical sealing method of MEMS devices with small form factor. It is also very attractive in 3D integrations as it can provide electrical contacts. However, the main disadvantages are the relatively high bonding temperature and bonding pressure. A large bonding force is required when increasing the wafer size, which can cause wafer fracture during bonding.

2.4. Eutectic bonding

Eutectic wafer bonding is a widespread method in MEMS systems for hermetically sealed packaging and 3D integrations. Compared to thermocompression bonding between two metals, eutectic bonding is based on a eutectic system of alloys used as the intermediate bonding layer to bond two wafers together via diffusion mechanism. In the eutectic system, their mixture can melt or solidify at a lower temperature than the melting point of the individual component materials. There is a wide range of material combinations for eutectic wafer bonding, such as Au–In, Au–Ge, Au–Sn, Au–Si, Al–Ge and Cu–Sn[37–40]. Among these combinations, Au–Si system is the most commonly used one. Before the Au–Si eutectic bonding process begins, a surface pre-treatment process is required. It is an essential step as the native oxides of metals can prevent the bonding. After the pre-treatment, a silicon-cap wafer and a wafer deposited with Au layer are placed face-to-face and loaded into the bonding chamber. The bonding starts to occur at the temperatures higher than their eutectic temperature of 363 °C. The typical bonding condition is to use 410–450 °C chamber temperature and 0.2–0.5 MPa bonding pressure[41]. Bonding uniformity continues to increase with the increasing chamber pressure. However, the bonding strength and bonding yield can decrease when the contact pressure is too high. This is caused by the metal squeezing-out at the bonding interface[42]. Benefiting from the lithography process to define the bonding sites, small device packaging with a relatively small seal ring pattern is possible. Eutectic bonding, similar to thermocompression bonding, has electrically conductive bonds, compatible with electronic components integration. However, it also has disad-

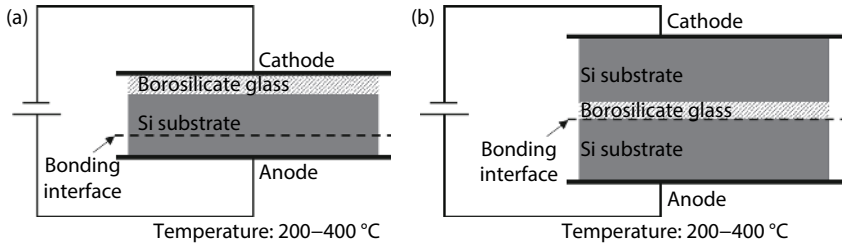

Fig. 1. Schematic views of (a) silicon–glass anodic bonding and (b) silicon–silicon anodic bonding mediated with a borosilicate glass layer.

vantages, such as non-uniform bonding, complicated bonding process, and high bonding temperature. In addition, as eutectic bonding occurs at elevated temperatures, the large thermal budget is detrimental to the electronic and MEMS devices. Localized heating with focused laser beam heating at the contact sites is a viable approach[43]. The exposed area to high temperature is significantly reduced.

2.5. Glass frit bonding

Glass frit bonding is a wafer-level encapsulation and packaging technology. It allows strong hermetic wafer bonds with a high process yield, especially designed for MEMS resonators and micosensors[44, 45]. Recent research shows laser-assisted glass frit bonding is a suitable encapsulation technology for inorganic quantum dot light-emitting devices (QLED)[46]. In glass frit bonding, there are three major steps: i) the deposition of glass paste on the wafer surface by spaying, screen-printing, or spin coating, ii) the conditioning or pre-sintering of the paste to remove the organic binders, and iii) the bonding step allowing hermetic bonds to form between the wafers. Low melting glass (lead or lead silicate) as an intermediate material in the bonding is milled into fine powder. Then the powder is mixed with an organic binder, which promotes the deposition of the glass on wafer surface. The thermal expansion coefficient can be modified by adding inorganic fillers into the glass paste, making it compatible with silicon-based MEMS devices. During the bonding steps, heat is applied to enable glass paste reflowing and wetting over the bonding frames. A strong and stable bond is formed after cooling down. The main advantage of the glass frit bonding is its applicability to nearly all surfaces regardless of the surface materials and roughness. No wafer surface activation or special preparation process is necessary. Other advantages include high bond strength, good process stability, particle compensation, selective area bonding and hermetical sealing. However, the large sealing ring and relatively low sealing frame precision make glass frit bonding less superior than eutectic bonding. Additionally, uncontrolled flowing of glass paste into the undesired region is a main problem using glass frit bonding. A special design to block reflowing and optimization in glass paste deposition can help to solve this problem in the future.

2.6. Adhesive bonding

Adhesive bonding utilizes polymer adhesives such as benzocyclobutene (BCB), spin-on glass (SOG), resists and polyimides as the intermediate layer for bonding[47–50]. Wafer-scale bonding with the substrate diameter up to 200 mm has been successfully demonstrated using BCB as the adhesive material[48]. In adhesive bonding process, a thin layer of the polymer adhesive is applied on one of the two mating wafers followed by the steps of polymer heat or ultraviolet light pre-curing, room temperature pre-bonding and low temperature annealing. The polymer adhesives are normally in a liquid, semi-liquid or viscoelastic phase during the bonding, then transformed into a low viscous phase, and finally into the solid phase to achieve strong and stable bonds[50]. In order to improve the bonding strength and quality, the bonding processes, such as film deposition methods, pre-curing conditions, bonding and chamber pressures, need to be carefully chosen. One of the advantages using the adhesive bonding technique is its low temperature conditions (typically not exceeding 250 °C), making it suitable for 3D MEMS, nano-electromechanical systems (NEMS), photonic circuits integration and CMOS integrated devices. Another major advantage is the soft and deformable features of poly adhesives. On one hand, the intermediate adhesive layer can flow easily to avoid the microvoids formation by compensating the extrinsic interface particles (particles with the diameter smaller than the layer thickness) and the CMP caused imperfections. On the other hand, the intermediate layer thickness can also be varied in a wide range from nm to μm. A sufficiently thick intermediate layer can be used to planarize the surface and even encapsulate the high topography structures. Thus, adhesive bonding applications are also applied in wafer-to-wafer alignment. However, the wafer alignment accuracy is significantly reduced due to the unavoidable sheer force during the bonding process. When two mating wafers are brought into close contact and stacked, the deforming intermediate layer is not strong enough to counteract the sheer force at the bonding interface and the bonding process causes alignment shifts. To reduce the shift, surface structures are introduced at the wafer edge to increase the friction[51]. The use of partially cross-linked polymer adhesives can also help to improve the alignment accuracy as they do not reflow during the bonding process. It has been demonstrated that the shift can be attained as low as 1 μm by using the partially cured BCB[52].

2.7. Anodic bonding

Anodic bonding, also referred to as field assisted bonding or electrostatic bonding, joins ion conductive materials to metal or silicon through a sufficiently strong electrical field[53, 54]. It is a well-established technology used in the semiconductor industry for microsensors fabrication and MEMS packaging. Alkali ion containing borosilicate glass (traded as Pyrex® 7740) is often used in metal-glass and silicon-glass bonding. Silicon–silicon bonding is also possible with anodic bonding when mediated with a thin layer of the sputter-deposited borosilicate glass[55]. The schematic process of silicon–silicon anodic bonding is shown in Fig. 1(b). The bonding temperature used ranges from 200 to 400 °C[56], which needs to be sufficiently high to render the non-conductive material electric-

ally conducting. The electrostatic voltage in the range of 200–1000 V is applied[57]. In silicon–glass anodic bonding pair, the silicon side and the glass side are biased as the anode and the cathode, respectively. When the sandwiched anode–silicon–glass–cathode structure is subjected to a strong electrostatic field, the mobile alkali ions in the glass are drifted away from the bonding interface, leaving a few-micron-thick depletion region. The charges left in the glass create a large electric field. The wafer surfaces are pulled into contact by the large electric field[57]. Therefore, anodic bonding is not strongly relying on the surface smoothness and ultraclean environment thanks to the large pulling forces. In addition, anodic bonding has the advantages of low process temperature and high bond strength of 10–25 MPa. However, anodic bonding is limited to joining ion conductive materials with metals or semiconductors. A sufficient amount of mobile charge carriers are required, which makes it incompatible with some MEMS devices. Thermal mismatch between the ion conductive material and the anode material is another major concern. Even a small thermal mismatch can induce a noticeable distortion in devices. Contamination from mobile charge ions is also a challenge using anodic bonding.

3. Wafer bonding technique and applications

Our group has successfully demonstrated the monolithic integration of Si-CMOS on SOI and III–V device layers on Si using wafer bonding and layer transfer techniques. In this section, we will discuss various DWB techniques, such as single-, double- and multiple-bonding techniques, and their possible applications. Since the high temperature growth of III–V wafers can be completed without the presence of Si-CMOS layers, DWB provides more temperature tolerance to pre-bonding processes. In addition, a plasma activation step is used to increase the surface hydrophilicity of bonding dielectric layers, and it can be performed at room temperature and atmosphere pressure. Therefore, DWB also avoids the thermal damage to Si-CMOS devices during the bonding processes.

3.1. Direct wafer bonding using various types of bonding dielectrics

3.1.1. SiO_2 to SiO_2 bonding

Silicon oxide (SiO_2) is a widely used dielectric material in the semiconductor industry, deposited by plasma-enhanced chemical vapor deposition (PECVD). In this experiment, two Si wafers were pre-cleaned using standard RCA to remove organic and metallic contaminants, followed by the deposition of SiO_2 by PECVD. Then additional densification was applied to remove the gas molecules or by-product residuals. After densification, the oxide surface was polished by CMP to smoothen the oxide surface to obtain a nearly atomically flat surface. After an RCA-based post-CMP cleaning step, a particle-free hydrophilic surface was obtained. By bringing two wafers into intimate contact at room temperature, the wafers were bonded. Fig. 2(a) shows the schematic of this bonding process, and Fig. 2(b) shows the IR image of the bonded wafers. An annealing step at 300 °C was applied after bonding to enhance the bonding strength[11, 12].

However, as shown in Fig. 3, there are many voids after post-bond annealing. These voids are caused by the increased incorporation of hydroxyl groups (–OH) during annealing, which can be explained by the silanol polymerization reaction. During this reaction, Si–OH groups react with each other and form Si–O–Si groups and H_2O, as expressed by the following formula[58]:

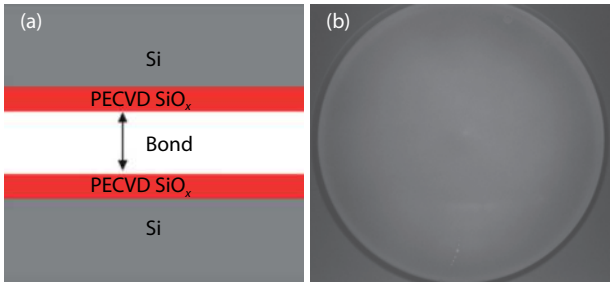

Fig. 2. (Color online) (a) Schematic of the DWB process via SiO_2 dielectric layers, and (b) shows the IR image of the bonded wafer.

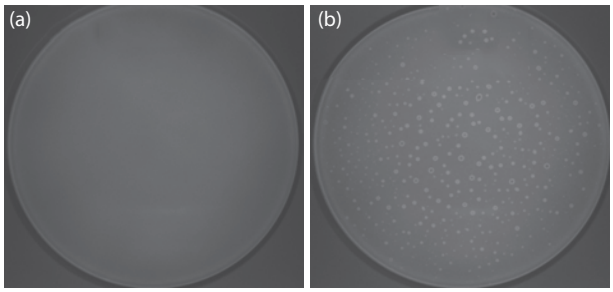

Fig. 3. IR images of a bonded wafer with SiO_2 dielectric layers (a) as bonded, and (b) after post-bond annealing.

$$\mathrm{Si{-}OH + HO{-}Si \rightarrow Si{-}O{-}Si + H_2O.} \quad (1)$$

The H_2O and absorbed moisture can be trapped and accumulated at the bonding interface to form voids.

3.1.2. Si_3N_4 to Si_3N_4 bonding

To address the void formation issue after post-bond annealing, an additional thin Si_xN_y layer a capping layer was added to SiO_2 layers by PECVD, as shown in Fig. 4(a)[59]. The Si-NH groups from Si_xN_y layers react to reduce the incorporation of –OH groups and the moisture absorption, as expressed as the following[58]:

$$\mathrm{Si{-}NH + HN{-}Si \rightarrow Si{-}N{-}Si + H_2.} \quad (2)$$

The IR images of the as-bonded and post-bond annealing wafers pairs with Si_xN_y intermediate layers are shown Figs. 4(b) and 4(c).

To verify the function of the additional nitride layer, Fourier transform infrared (FTIR) spectra were used. From Fig. 5, the vibration mode at 3750 cm^{-1} for the wafers with nitride films stays almost flat after four days of storage compared to the wafer with SiO_2 film only, indicating the capping nitride layer was acting as a moisture barrier.

The film stress can be determined by using a stress measurement system, it shows that the compressive stress in Si_xN_y layers becomes tensile stress, and the tensile stress is very stable after 10 days of storage, as shown in Fig. 6. This also indicates that the Si_xN_y layers block the moisture absorption after annealing. This can be explained by the higher density and mechanical strength, compared to SiO_2.

3.1.3. AlN to AlN bonding

AlN can also be used as the bonding dielectric, due to its excellent properties, such as good temperature stability

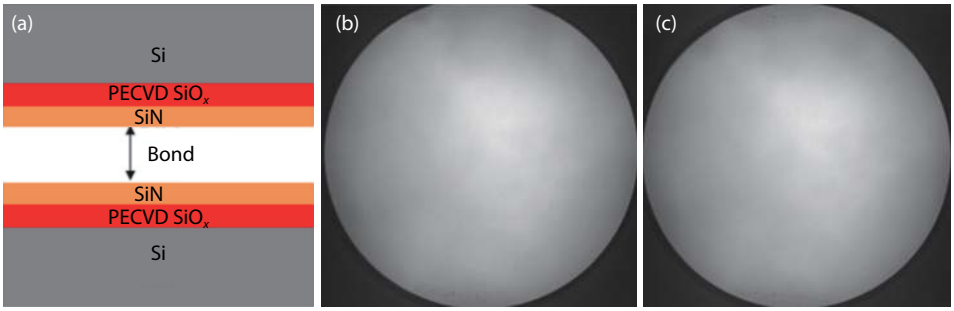

Fig. 4. (Color online) (a) Schematic of the bonding process with an additional thin deposited Si_xN_y layer, and the IR images of (b) as-bonded wafers and (c) after post-bond annealing.

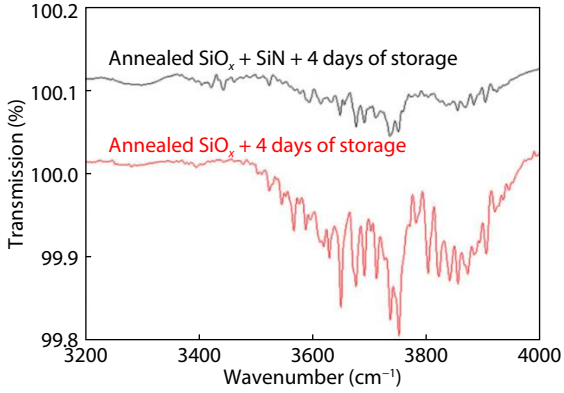

Fig. 5. (Color online) The comparison of FTIR spectral changes at the vibration mode at 3750 cm^{-1} between the $SiO_x + Si_xN_y$ and SiO_2 films after annealing and four-day storage under cleanroom environments.

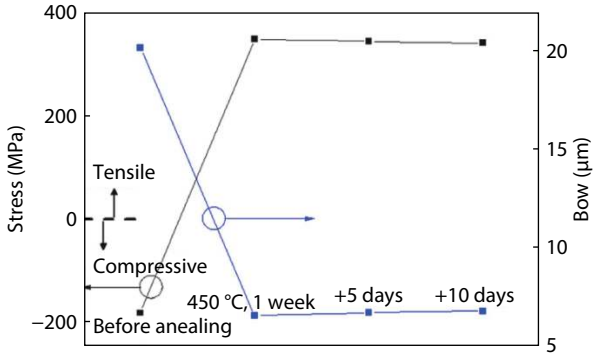

Fig. 6. Change in the Si_xN_y layers stress profile. Compressive stress turns into tensile stress in Si_xN_y layers after annealing, and its stress and bow stay stable after 10 days of storage, indicating that the moisture absorption is blocked.

and high thermal conductivity (AlN: 134 $Wm^{-1}K^{-1}$ and SiO_2: 1.4 $Wm^{-1}K^{-1}$). Similar to SiO_2 to SiO_2 bonding, two Si wafers were pre-cleaned, followed by the deposition of 20 nm AlN films by sputtering aluminium in N_2 atmosphere at 75 °C using atomic layer deposition (ALD)[60]. After the deposition, a pre-annealing step at 450 °C for 1 h in N_2 environment was carried out. This annealing step densifies the AlN film to suppress the void formation. Then 15 s Ar plasma activation was applied to enhance the surface hydrophilicity, followed by de-ionized (DI) water cleaning and spin rinse drying (SRD). As mentioned previously, the plasma activation of AlN to AlN bonding was initiated at room temperature and atmospheric pressure. Then, a relatively low post-bond annealing temperature at 300 °C in N_2 ambient for 3 h was used to further increase the bonding strength. The schematic process and the IR images are shown in Fig. 7. In Fig. 7, the unbonded areas appeared after bonding due to the presence of particles. After post-bond annealing, there was no new formation of voids. Although the performance of AlN to AlN bonding is excellent, its bonding mechanism is not well established. We suspect that the bonding reaction is a polymerization process of Al–NH groups after the surface is passivated by H in DI water rinse.

During the pre-annealing step for outgassing in a furnace, the AlN thin film was prone to oxidation when exposed to ambient, and the high temperature at 450 °C also accelerated the oxidation. With this concern, the composition of AlN thin films was verified by XPS measurement. Fig. 8 shows the atomic concentration against the sputtering depth. The atomic ratio of Al and N are close to 1 : 1, indicating the expected composition of AlN. The surface region shows a slight stoichiometry mismatch, which is possibly caused by the partial oxidation by H_2O or O_2 in the air.

3.1.4. Al_2O_3 to Al_2O_3 bonding

We also investigated Al_2O_3 as the bonding dielectric[61–64]. Al_2O_3 was chosen due to its higher thermal conductivity than that of SiO_2 (Al_2O_3: 30 $Wm^{-1}K^{-1}$ and SiO_2: 1.4 $Wm^{-1}K^{-1}$). In this experiment, two wafers are prepared: (i) Ge/Si wafer fabricated by Ge directly epitaxial grown on Si (001) substrate, and (ii) Si (001) wafer. A 10 nm Al_2O_3 film was deposited on both Ge/Si and Si (001) wafers by ALD, as shown in Fig. 9. A 15 s O_2 plasma activation treatment was applied, followed by DI water cleaning and drying on the prepared wafers. The cleaning step covered the wafer surfaces with –OH groups to initiate the Al–O–Al bond formation, of which the reaction is expressed as the following:

$$\text{Al–OH} + \text{HO–Al} \rightarrow \text{Al–O–Al} + H_2O. \quad (3)$$

After bonding, the post-bond annealing at 300 °C in an atmospheric N_2 ambient for 3 h was performed for bond enhancement.

Fig. 10 shows a cross-section transmission electron microscope (TEM) image of the bonded wafer pair to verify the bonding quality at the Al_2O_3 bonding interface. As shown in the TEM images, the Al_2O_3 bonding interface is uniform and seamless with no sign of micro-voids. In addition, the O_2 plasma activation modified the stoichiometry of the Al_2O_3, causing contrast differences in the Al_2O_3 layers.

3.1.5. Applications ('X'-OI)

Silicon-on-insulator (SOI) has many advantages over Si,

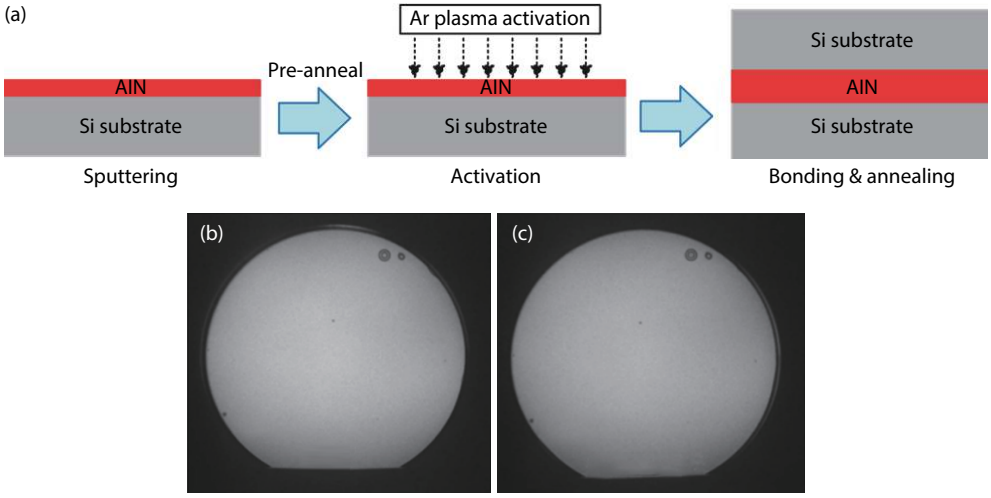

Fig. 7. (Color online) (a) Schematic of AlN to AlN bonding process and the IR images of (b) as-bonded wafers, and (c) after post-bond annealing.

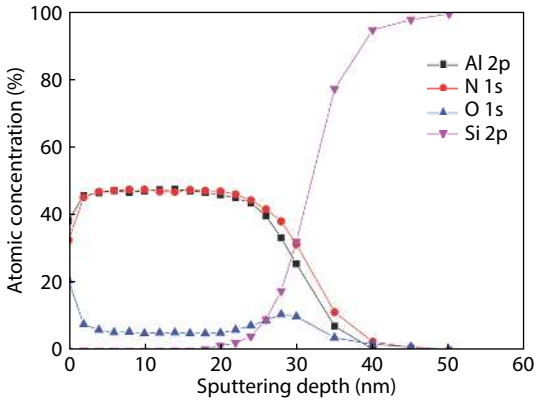

Fig. 8. (Color online) XPS Atomic concentration profiles of pre-annealed AlN.

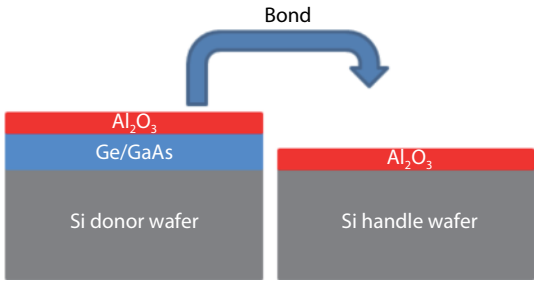

Fig. 9. (Color online) Schematic of Al_2O_3 to Al_2O_3 bonding process.

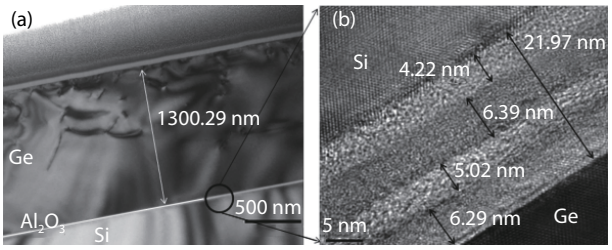

Fig. 10. Cross-sectional TEM images of (a) the bonded wafer pair, and (b) the bonding interface.

such as reduced parasitic capacitances and short channel effects. Similar to SOI, the germanium-on-insulator (Ge-OI) and other III–V materials-on-insulator ('X'-OI) are not only used as the substrates, but also as active layers, such as the light source in a silicon photonic system. In addition, since Si is the handle wafer, some of the CMOS tools and processes can be shared with these new insulators.

In this section, we present a scalable method to fabricate high-quality Ge-OI wafers[61–64]. The fabrication involves the processes of direct Ge epitaxial growth on Si, fusion bonding, and layer transfer. The fabrication of GaAs-OI and GaN-OI wafers will also be discussed.

In the Ge-OI fabrication experiment, two sets of wafers were prepared: (i) Ge films epitaxially grown on 200 mm Si donor wafer using a metal organic vapor deposition (MOCVD), and (ii) Si (001) handle wafer. A 10 nm thin Al_2O_3 layer was deposited on each prepared wafer by ALD.

The bonding process was similar to Al_2O_3 to Al_2O_3 bonding as described previously. SiO_2 can be used as the bonding dielectric as well. After bonding and post-bond annealing, the donor Si substrate was removed through mechanical grinding and selective wet etching in 80 °C tetramethylammonium hydroxide (TMAH) solution, which etch-stopped at the Ge layer. The backside of the handle wafer was protected with spin-coated ProTEK® B3-25 films during TMAH etching. Then the O_2 plasma with the power of 800 W was applied to remove the protective coating. The schematic of the Ge-OI fabrication process flow is shown in Fig. 11.

The Ge-OI substrate was annealed at 850 °C in O_2 environment for 4 h, followed by CMP process, to reduce the misfit dislocation by oxidation, and the threading dislocation densities (TDDs) by annihilation. After that, HF etching (49% HF : H_2O = 1 : 20, by volume) for 30 s to remove the oxidized Ge layer, a Ge film with a low TDD of mid-10^6 cm^{-2} was achieved. This TDD level of the Ge is good enough for the Ge film is good enough for most electronic and optoelectronic device applications.

TEM and etch-pit density (EPD) methods were used to characterize the Ge film quality. Plan view TEM shows the Ge-OI surface before and after O_2 annealing, as shown in Fig. 12. It shows that the TDD was reduced by 1 order of magnitude after annealing. As EPD is a fast and cheap method, it was used to quantify the TDD of the Ge film after annealing and CMP by etching the sample in iodine solution for 1 s. As shown in Fig. 13, the EPD counted TDD was reduced by two orders of magnitudes from $(5.2 \pm 0.45) \times 10^8$ to $(2.5 \pm 0.4) \times$

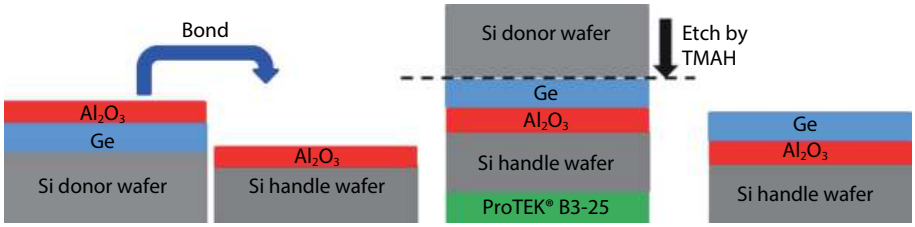

Fig. 11. (Color online) Schematics of Ge-OI fabrication process.

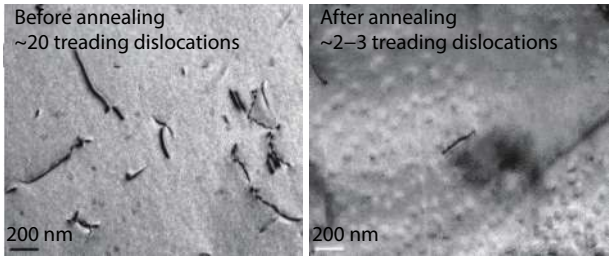

Fig. 12. Plan view TEM images of the Ge surface of Ge-OI before and after O_2 annealing.

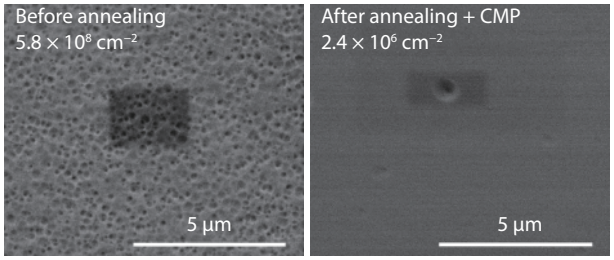

Fig. 13. The EPD determined TDD of the Ge of Ge-OI before annealing and after annealing + CMP.

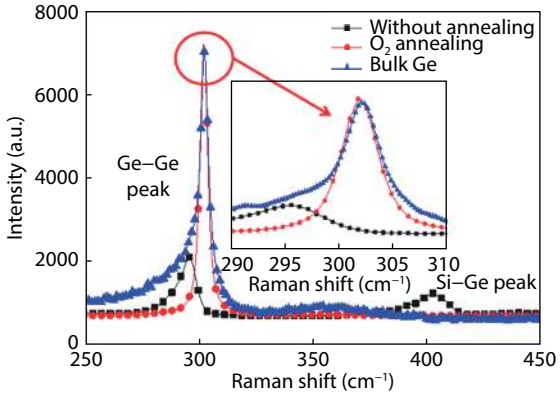

Fig. 14. (Color online) Raman spectroscopy of the Ge film on Ge-OI before and after annealing.

10^6 cm^{-2} after annealing and CMP.

To determine the alloy composition and strain of the Ge film, Raman spectroscopy was used. As shown in Fig. 14, there was no signal of the Si–Si vibration mode as the Si from the donor wafer was removed completely by TMAH. After O_2 annealing, the signal of the Si–Ge vibration mode disappeared as the Si/Ge intermixed layer was removed. The inset figure shows a blue shift of the Ge–Ge vibration peak from 296 to 302 cm^{-1} after O_2 annealing, indicating the Ge film of the Ge-OI was nearly stress-free after annealing. This may due to the amorphous nature of Al_2O_3 layer which acts as a stress-free buffer. Also, the Si and Ge/Si intermixed layer were

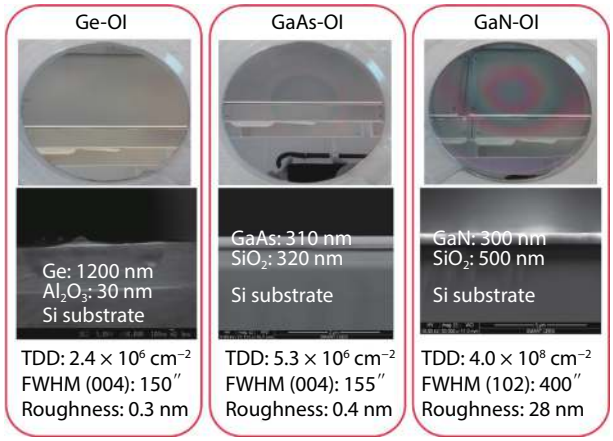

Fig. 15. (Color online) The fabricated 200 mm Ge-OI, GaAs-OI and GaN-OI substrate wafers.

removed by etching and subsequent O_2 annealing, therefore Ge is no longer constrained by Si, which led to a nearly stress-free state.

GaAs-OI and GaN-OI substrate can also be fabricated through similar bonding processes as shown in Fig. 15. Depending on applications, various bonding dielectrics (SiO_2, Al_2O_3 or AlN) can be chosen.

In summary, the 'X'-OI substrate can be fabricated through buffer-less III–V epitaxy, bonding and layer transfer. This method is scalable to various wafer sizes and makes the CMOS devices with III–V/Si integration on common Si wafers become possible.

3.2. Double bonding and layer transfer for Si-CMOS and III–V/Si integration

With the optimized bonding processes as described previously, in this section, we demonstrate a method to integrate III–V compound semiconductor materials with SOI-CMOS on a common Si substrate[11–13, 65, 66]. Firstly, the SOI-CMOS layer is temporarily bonded on a Si handle wafer. Then, the III–V on Si wafer is bonded to the SOI-CMOS + Si handle wafer. Finally, the SOI-CMOS on III–V/Si hybrid structure on a common Si substrate is realized by releasing the Si handle wafer. With this double bonding and layer transfer method, several issues encountered with SOI-CMOS and III–V/Si integration can be addressed: (i) the cross-contamination issue between CMOS and III–V materials in foundries processes, and (ii) high temperature CMOS processes which may cause serious damage for III–V material systems such as arsenide (As)/phosphide (P) containing III–V materials (e.g., InGaAs, InP, etc.). Hence, with this double bonding and layer transfer method, III–V material growth can be completely separated with CMOS processes, thus the damage to both the III–V layer and CMOS layer can be avoided.

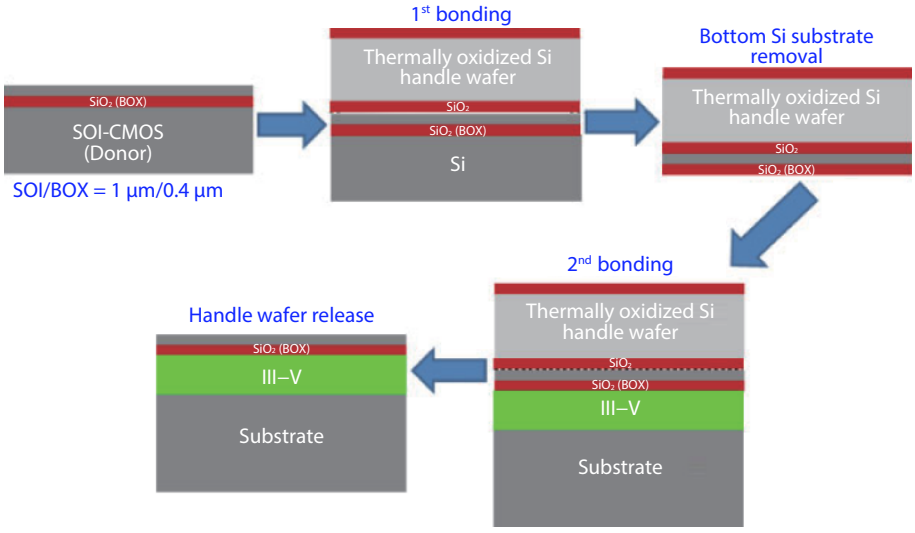

Fig. 16. (Color online) Schematic flow of the double bonding and layer transfer process.

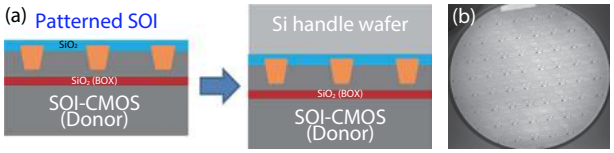

Fig. 17. (Color online) (a) Schematic flow of the first bonding process between SOI and thermally oxidized Si handle wafer and (b) IR image of the bonded wafer pair.

In this experiment, three sets of wafers were prepared: (i) p-type 200 mm Si (001) prime-grade wafers (as Si handle wafer), (ii) patterned silicon-on-insulator (SOI) wafer, with Si and buried oxide (BOX, thermal SiO_2), and (iii) III–V on Si wafer (e.g., InGaAs/GaAs/Ge-on-Si or GaN-on-Si) wafers. The schematic flow diagram of the process is shown in Fig. 16.

3.2.1. First bonding (between SOI wafer and thermal oxidized Si handle)

The first bonding was between the patterned SOI wafer and thermally oxidized Si handle wafer. The bonding quality was justified using the IR camera, where any interface voids formed between the bonded wafer pair can be observed. As shown in Fig. 17, no significant voids or particles are observed from the IR image, which indicates an excellent bonding quality between the SOI wafer and thermally oxidized Si handle wafer.

After the first bonding, the Si from the SOI-CMOS donor wafer was ground down to 50 μm, followed by TMAH chemical etching to completely remove the remaining Si, which etched stopped at the BOX layer. However, the BOX layer is slightly damaged by the TMAH solution, and a lot of pin-holes are formed and can be observed, as shown in Fig. 18. We believed that this could be due to the slight etching on the sub-standard quality BOX, where the thermal oxide of the BOX is grown using relatively low-quality wet oxidation instead of higher quality dry oxidation.

After the first layer transfer, the SOI-CMOS is now on the Si handle wafer. The second bonding is performed between the patterned SOI and III–V/Si wafer. The IR images of the InGaAs and GaN are shown in Fig. 19. Unbounded areas are observed due to pin-holes on the BOX layer. In addition, the particles from the III–V/Si may also contribute to the unbounded area.

3.2.2. Replacement of the BOX layer with PECVD oxide

To tackle the pin-holes issue associated with the BOX layer, the BOX surface was planarized by CMP process. Right after the CMP step, RCA-based cleaning was carried out, followed by a de-ionized (DI) water rinse and spin dry using spin rinse dryer (SRD). However, the pin-hole problem became more obvious and was worse after the CMP process, as shown in Fig. 20.

The next attempt to address the pin-hole problem was to use an additional 50 nm SiO_2 deposited by plasma-enhanced CVD (PECVD), as a compensation layer on top of the BOX layer. The addition of the PECVD oxide roughens the oxide surface, which prevents a successful wafer bonding in the subsequent step. Therefore, after the PECVD oxide, densification was carried out and followed by the CMP process to planarize the oxide surface. However, after the second bonding, there are still many unbonded areas observed in the bonded wafer pair, as shown in Fig. 21.

Then the third attempt to avoid the pin-holes problem was to remove the BOX layer completely and replace it with PECVD oxide. The sub-standard quality BOX layer was removed by diluted HF solution (with volume ratio HF : H_2O = 1 : 10), and followed by PECVD oxide deposition. CMP was carried out to smoothen the PECVD oxide for the second bonding process. Then, the wafer with the PECVD oxide was bonded to another Si prime wafer (no III–V layers). The bonding quality is verified with the IR image. No significant void is observed, as shown in Fig. 22.

3.2.3. Second bonding (between SOI-handle pair and Si prime wafer)

The second bonding was performed between the SOI-handle pair and a Si prime wafer. The Si handle wafer was then completely removed by grinding and chemical etching. With the CMP-on-BOX method, after the double bonding and layer transfer process, delamination is observed on the surface of the bonded SOI–Si wafer. The delamination area is corresponding to the un-bonded area due to the pin-hole issue. A similar delamination issue is also expected for the PECVD-ox-

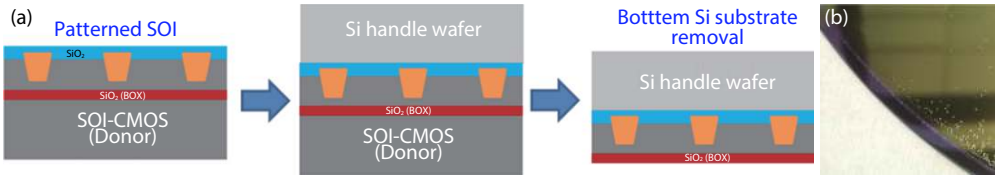

Fig. 18. (Color online) (a) Schematic flow of the first bonding and substrate removal and (b) optical image of the bonded pair after substrate removal where pin-holes are observed.

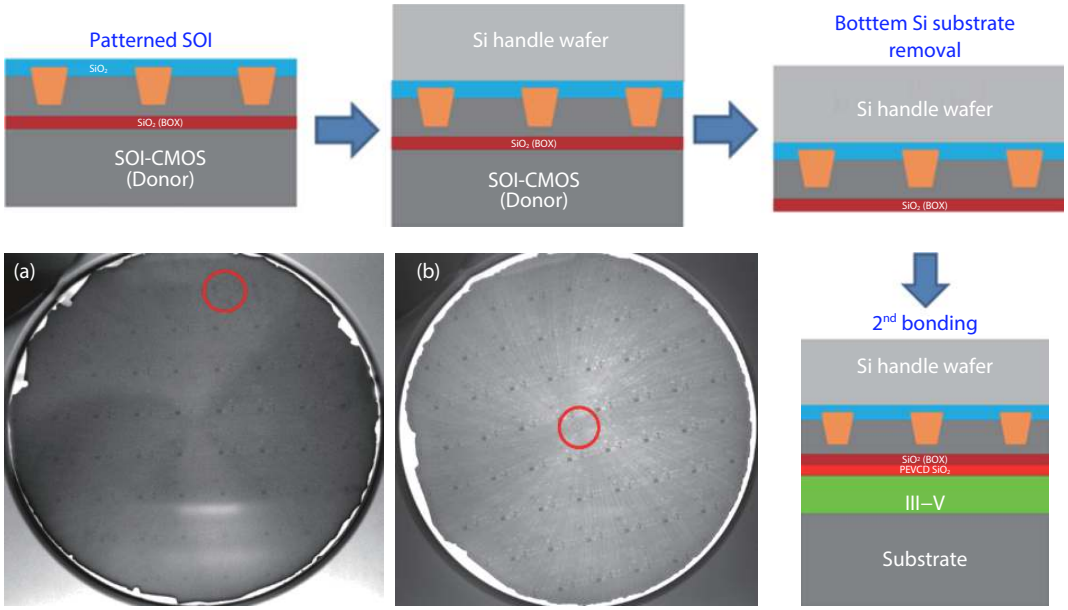

Fig. 19. (Color online) Schematic flow of the double bonding process. (a) IR image of bonded SOI–InGaAs pair and (b) IR image of bonded SOI–GaN pair.

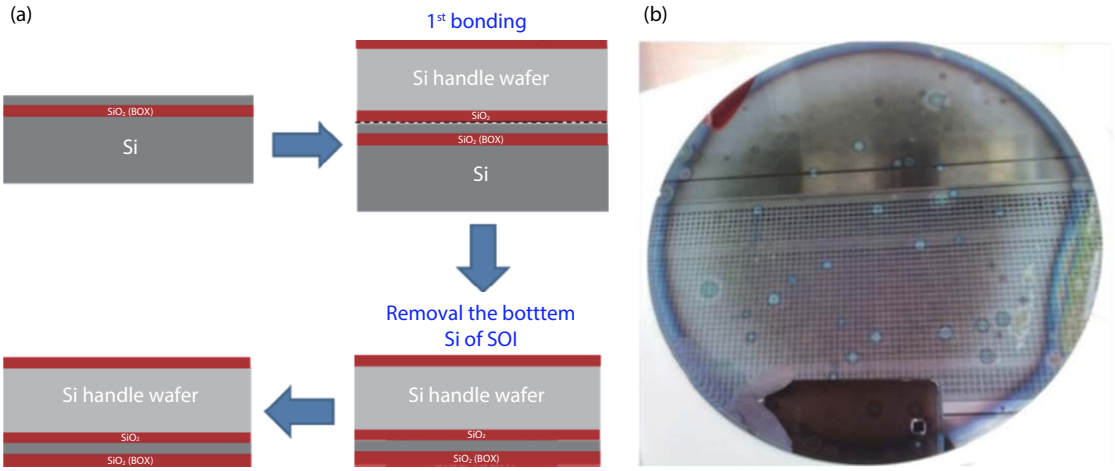

Fig. 20. (Color online) (a) Schematic flow of 1st bonding with CMP-ed BOX layer. (b) Optical image of the resultant wafer after the process, where pin-holes are observed.

ide-on-BOX method. By completely removing the BOX layer and replacing it with PECVD oxide, a clean surface with an almost defect-free SOI–Si wafer pair is successfully demonstrated after the second bonding and removal of the handle wafer.

Fig. 23 (the top row) shows a comparison after the second bonding. For the CMP-on-BOX method, unbonded areas are observed across the entire wafer. Many unbonded areas can be observed for the PECVD SiO_2 (-on-BOX) method as well. Almost defect-free wafer is observed for the BOX etching method.

The Si handle wafer was then removed by mechanical grinding and wet chemical etching as described previously. Film peeling was observed from the SOI–Si wafer as shown in Fig. 23 (the bottom row). The delaminated area is even larger than the unbounded area before Si handle removal, due to the weak bonding strength around the unbounded area, which leads to easier film delamination when the handle wafer is released.

Cross-sectional TEM is used to exam the quality of SOI–Si

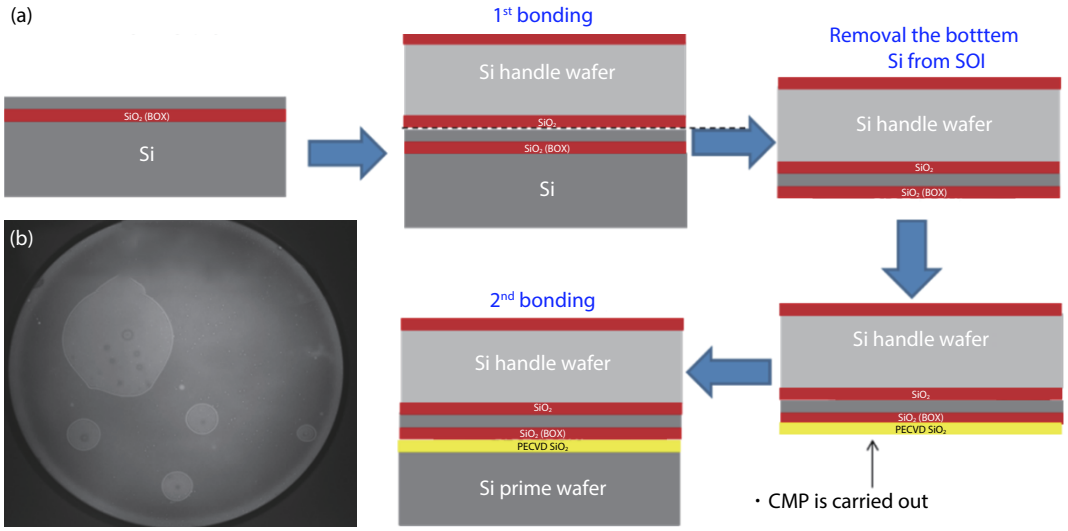

Fig. 21. (Color online) (a) Schematic flow of the double bonding process with additional SiO_2 layers. (b) IR image of the bonded wafer pair.

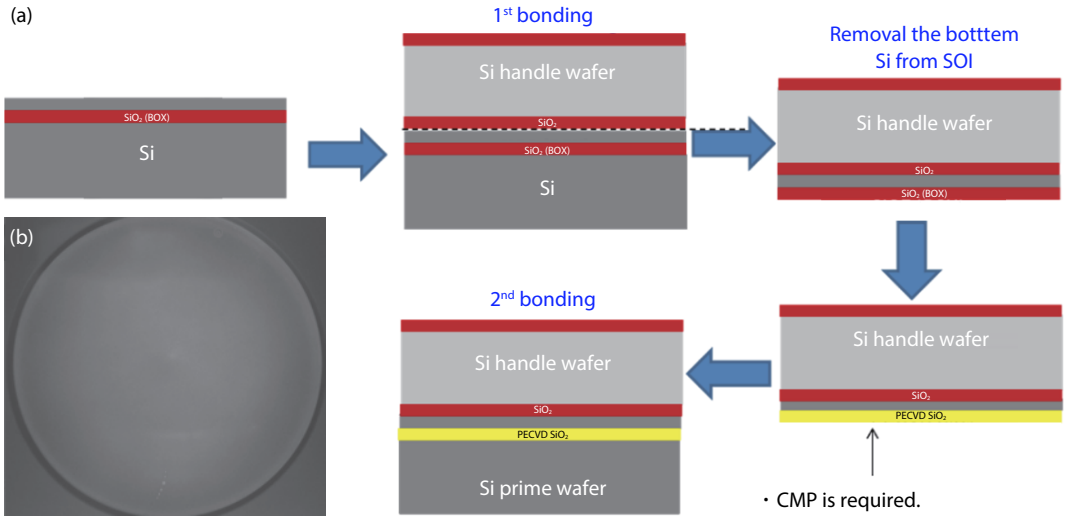

Fig. 22. (Color online) (a) Schematic flow of double bonding process with BOX layer completely replaced by PECVD oxide. (b) IR image of the bonded pair. No pin-holes are observed.

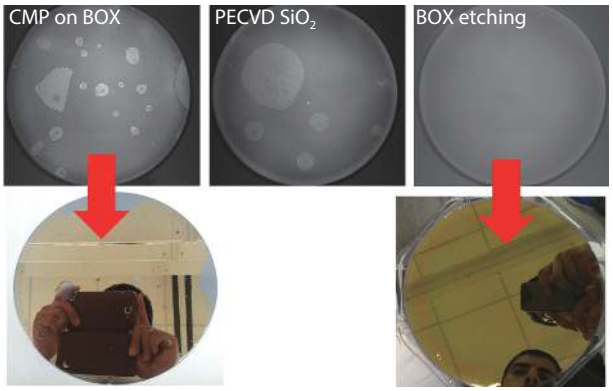

Fig. 23. (Color online) IR images and optical images of wafers after double bonding and layer transfer using different methods.

bonding interface after double bonding and layer transfer process using BOX etching method, as shown in Fig. 24. The bonding interface between PECVD oxide and Si prime wafer are smooth and uniform, with no significant micro-voids are observed in the field of view. Therefore, a seamless bonding at

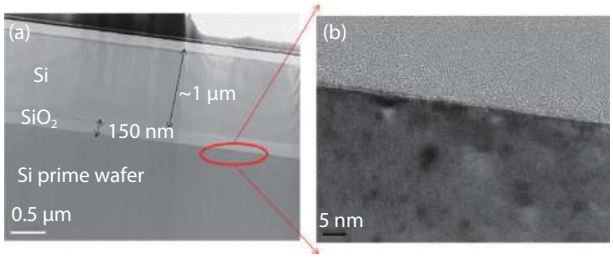

Fig. 24. Cross-sectional bright field TEM images of the bonded SOI-Si wafer pairs. (a) The overall view and (b) the bonding interface between PECVD oxide and Si prime wafer.

the microscale level with the PECVD-oxide-only method has been successfully achieved.

3.2.4. Applications: Bonding approach for Si-CMOS + III–As/P or III–N HEMT/LED wafers

We use the same process flow as described previously to demonstrate the integration of Si-CMOS + III–As/P HEMT or LED wafer. Now the actual Si-CMOS devices wafer and the III–As/P with device layers are used instead of the prime Si

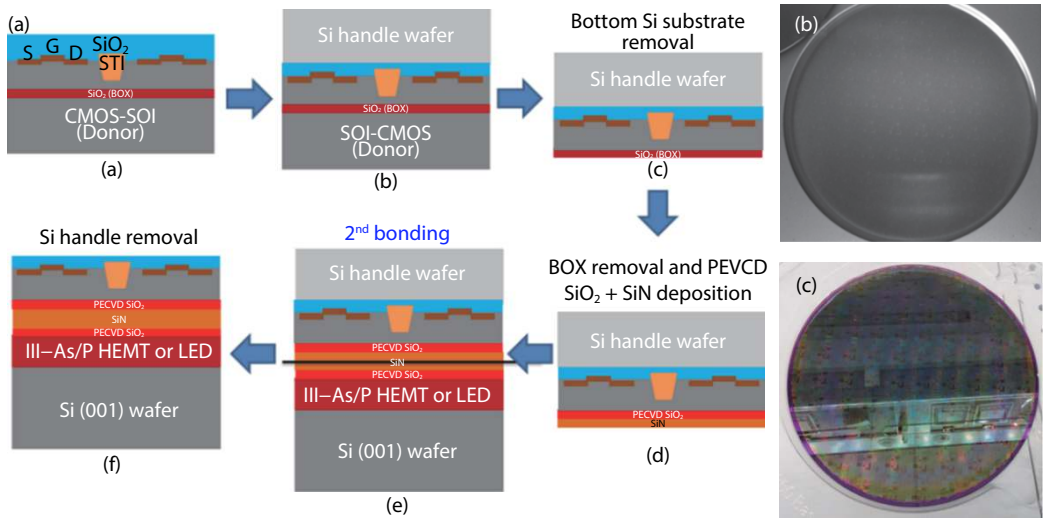

Fig. 25. (Color online) (a) Updated schematic diagram of the double bonding and layer transfer process. (b) IR image and (c) optical image of the resultant SOI–III–V/Si integrated wafer.

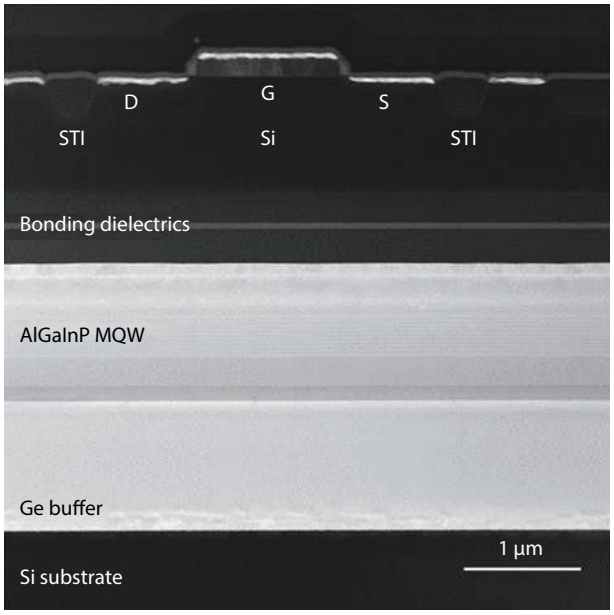

Fig. 26. Cross-sectional TEM image of the Si-CMOS/III–V/Si wafer after double bond and layer transfer.

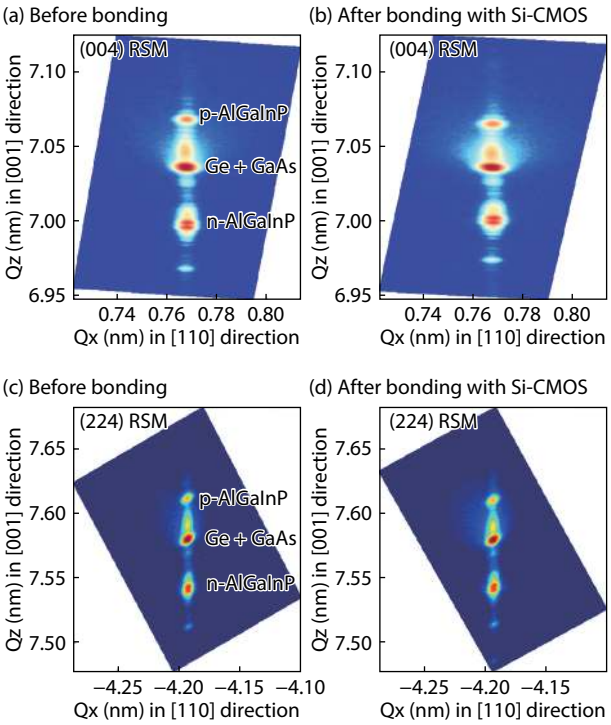

Fig. 27. (Color online) Symmetric (004) reciprocal space map (RSM) of an AlInGaP LED structure measured from XRD (a) before and (b) after bonding with Si-CMOS. Asymmetric (224) RSM of the AlInGaP LED structure (c) before and (d) after bonding with Si-CMOS.

wafer. Therefore, the second bonding Si_3N_4 to Si_3N_4 bonding discussed in the previous section will be used. The updated schematic flow is shown in Fig. 25 below.

Three sets of 200 mm wafers were prepared for this experiment: (i) Si (001) wafers, (ii) Si-CMOS/SOI wafers that have undergone front-end-of-line (FEOL) processing only in Si foundries, (iii) InGaAs HEMT or AlInGaP LED epitaxial films which were grown directly on GaAs/Ge/Si (001) wafers with 6° off-cut toward the [110] direction by MOCVD.

The Si-CMOS/SOI wafer was first deposited with 500 nm PECVD SiO_2 layer, followed by densification process in N_2 environment to eliminate the residual gas molecules and by-products incorporated into the layer during oxide deposition. Then the oxide surface was planarized by chemical mechanical planarization (CMP). Before the first bonding, both the SOI wafer and Si handle wafers were subjected to O_2 plasma exposure to increase the surface hydrophilicity. Then both wafers were rinsed with de-ionized (DI) water and spin-dried to clean the wafers and to populate the surface with hydroxyl (–OH) groups at a sufficiently high density to initiate wafer bonding. The post-bonding was performed at 300 °C in an atmospheric pressure N_2 ambient for 3 h to further increase the bond strength. The Si substrate from the SOI wafer was then completely removed by mechanical grinding and wet chemical etching in trtramethylammonium hydroxide (TMAH) solution, to realize the first layer transfer.

For the second bonding and layer transfer process, the BOX layer was first removed in HF solution and replaced with PECVD oxide, followed by densification and planarization, and additional PECVD Si_3N_4 (with densification) layer depos-

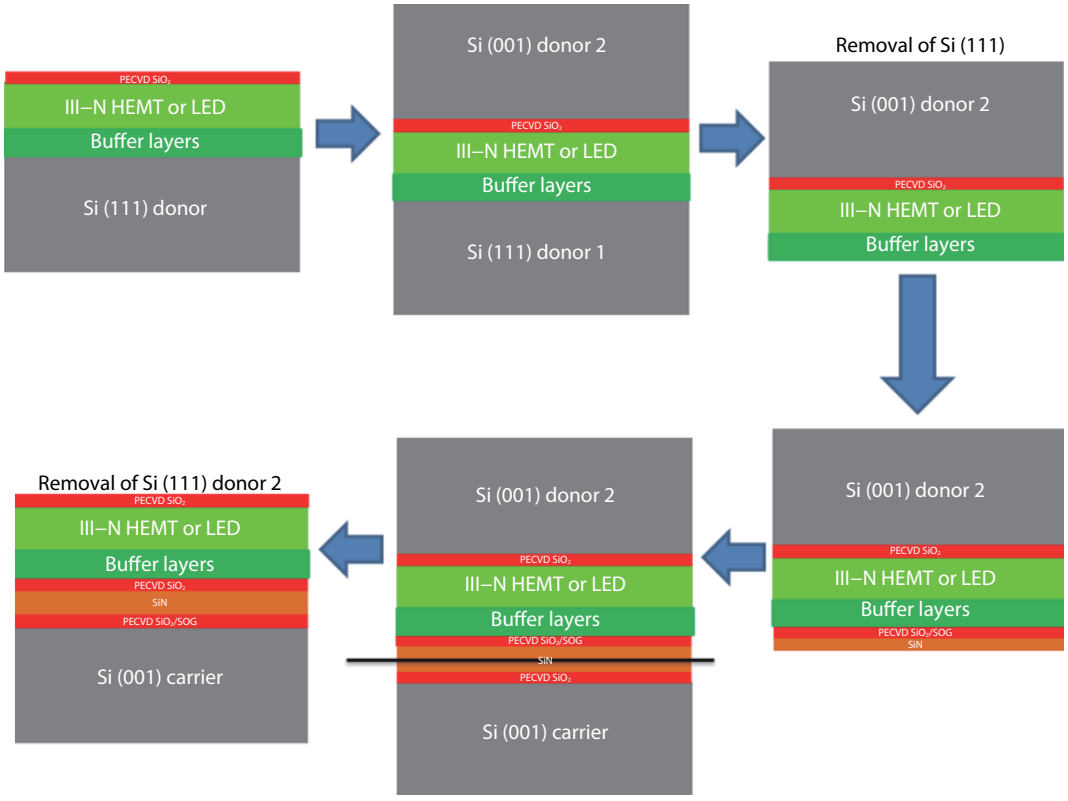

Fig. 28. (Color online) Schematic flow of replacing Si (111) substrate by Si (001) substrate for GaN HEMT/LED wafer.

ition, to address the pin-holes and outgassing issues. Then, the III–V/Si wafers (InGaAs HEMT, AlGaInP LED epitaxial films on Si) were also subjected to the same PECVD oxide and nitride deposition processes. After that, the two sets of wafer pairs were bonded together, followed by Si handle release to realize the Si-CMOS/III–V on Si wafer.

The cross-sectional TEM image in Fig. 26 shows the stack of Si-CMOS + InGaP LED on a common Si platform. A smooth and clean bonding interface can be observed with no microvoids between two PECVD Si_3N_4 layers. A uniform and seamless bonding at the microscale level is successfully demonstrated.

Non-destructive X-ray diffraction (XRD) measurements were used to characterize the properties of the AlInGaP LED wafer before and after the bonding process. There is no significant change in the peak positions and full widths at half maximum (FWHMs) of the active p-AlGaInP and n-AlGaInP layers, as well as the Ge + GaAs buffer layers, as shown in the reciprocal space map (RSM) from Fig. 27. This confirms that the bonding process does not significantly compromise the film quality.

Similar double bonding and layer transfer process described above was also applied for the integration of Si-CMOS + III–N (e.g., GaN) HEMT or LED wafers. However, due to the high-temperature MOCVD grown GaN on Si (111) wafers, the Si-CMOS + GaN HEMT/LED transfer yield is only ~50%.

This is mainly because during the high temperature GaN growth, slip lines formed at the wafer edge which propagated towards the center of the wafer weakens the Si (111) wafer and makes the wafer brittle. In addition, for the direct epitaxially grown GaN-on-Si wafer, the AlGaN buffer layers and GaN layers contribute different levels of stress and build up the stress levels on the Si (111) substrate which ultimately makes the Si substrate even more fragile.

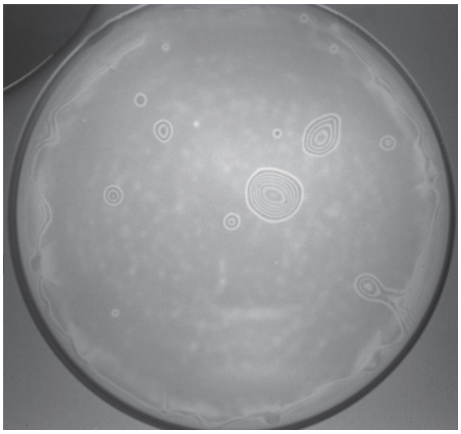

Fig. 29. IR image of a bonded GaN/Si wafer pair after substrate replacement.

Although minimizing the radical temperature difference across the Si (111) wafer during the III–N growth will reduce the slip line formation and improve the wafer fragility, it is impossible to fully eliminate vertical temperature differences through the wafer during the growth. In our MOCVD reactor, because the heating is only performed from the backside of the wafer. Thus, to address this issue, we introduced an additional wafer bonding and layer transfer processes, to replace the fragile Si (111) substrate by a new Si (001) substrate, the process flow of this substrate replacement is shown in Fig. 28.

First, a PECVD SiO_2 layer was deposited onto the III–N HEMT/LED on the Si (111) (donor 1) wafer, followed by densification and CMP processes. Then, a Si (001) (donor 2) wafer

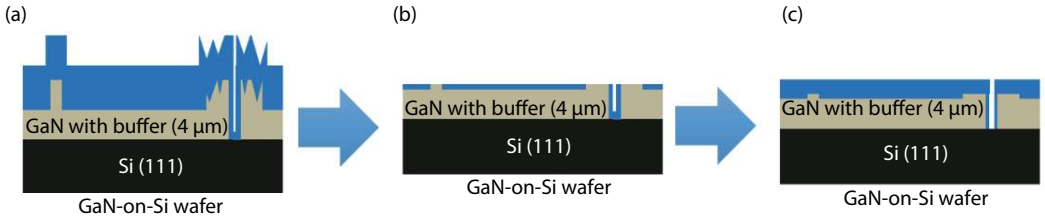

Fig. 30. (Color online) Schematic flow of the diamond CMP process. (a) After oxide deposition, (b) after CMP using slurry with the addition of diamond particles, and (c) another oxide deposition and CMP processes to smoothen the oxide surface which was roughened from the previous step.

was bonded to the III–N HEMT/LED wafer, followed by post-bonding annealing. After that, the Si (111) (donor 1) substrate was completely removed through a combination of mechanical grinding and wet-chemical etching in HNA solution (hydrofluoric + nitric + acetic acids). The bonded wafer and a new Si (001) (carrier) substrate were then subject to PECVD SiO_2 deposition, and the subsequent densification, CMP and Si_3N_4 deposition processes, as described previously. The two wafers were then bonded and annealed. The III–N HEMT/LED on a fresh Si (001) (carrier) substrate was realized by removing the Si (001) (donor 2) wafer. It was then can be bonded to the Si-CMOS-containing wafer to realize the Si-CMOS + III–N HEMT/LED integration.

Through this Si (111) substrate replacement method, the yield of the integrated Si-CMOS + GaN HEMT/LED wafers is almost 100% after the subsequent bonding and transfer processes without additional precautions.

For Si-CMOS + III–N bonding, particle issue is another problem that needs to be addressed. These particles found at the III-N surfaces are mainly melt-back etching and hillock sites come from the showerhead MOCVD reactor growth. The melt-back etching is characterized as a void on the surface of the wafer and a large surrounding area of materials with surface protrusions containing polycrystalline III–nitride and Si eutectic. In the epitaxy process of III–nitride, hillocks or hexagonal voids could be created due to material defects such as inversion domain boundary, stacking faults and threading dislocations. Since these particles are big protrusions on the wafer surface with the size of several micrometers, this affects the quality of the subsequent wafer bonding as shown in the IR image below, see Fig. 29. To solve this problem, we use diamond containing slurry for CMP to flatten the surface.

With PECVD SiO_2 deposition on the as-grown III–nitride wafers, the height difference caused by surface protrusions will remain after the PECVD process as illustrated in the schematic drawing, Fig. 30(a). To remove the hard III–nitride particles, additional diamond particles were added into the normal SiO_2 slurry. As a result, melt-back sites and hillocks were all reduced to about the same height as the remaining SiO_2, as shown in Fig. 30(b). A thin remaining layer of SiO_2 was left behind to protect the GaN surface from being damaged by the CMP process. After that, a thin layer of PECVD SiO_2 is deposited and CMP-ed for the subsequent bonding process.

With the substrate replacement and diamond CMP processes, robust and void-free bonding of Si-CMOS-containing wafer + III–nitride HEMT/LED on Si (001) substrate can be realized, as shown in Fig. 31.

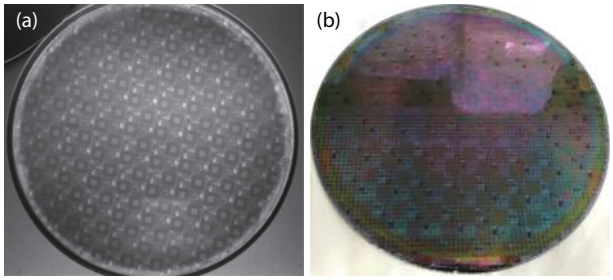

Fig. 31. (a) IR image, (b) optical image of Si-CMOS and GaN LED bonded pair on Si (001) substrate.

3.2.5. Applications: GaN LED-on-quartz

With the successful demonstration of Si-CMOS + GaN LED integration, there are two issues need to be addressed: (i) surface protrusions (which has been addressed in the previous section), and (ii) lower light-emitting efficiency of the GaN LEDs due to the absorption of photons by the Si substrate. In this section, we address the second issue by replacing the absorbing Si substrate with a transparent quartz substrate[67, 68], to achieve brighter GaN LEDs.

Three sets of wafers were prepared in this experiment: (i) Si (001) wafers, (ii) quartz substrate and (iii) GaN LED on Si (111) substrates epitaxially grown by metalorganic chemical vapor deposition (MOCVD). The schematic flow of the bonding process is shown in Fig. 32 below.

First, a 500 nm PECVD oxide layer was deposited on the GaN LED wafers to serve as a capping layer for CMP process as well as a bonding interface, followed by the densification process at 600 °C in N_2 environment. After densification, the oxide surface was CMP-ed, and subjected to O_2 plasma to increase the surface hydrophilicity, followed by DI water rinse and spin-dried to clean the surfaces and to populate the surface with hydroxyl (–OH) groups to initiate wafer bonding.

The bonded wafer pair was then subjected to post-bonding annealing at 300 °C in an atmospheric pressure N_2 ambient for 3 h to further increase the bond strength. The Si (111) substrate was then completely removed by mechanical grinding and wet-etching in HNA solution (hydrofluoric + nitric + acetic acids). The GaN LED epilayers were temporarily attached to the Si handle wafer.

Another 500 nm of PECVD oxide was deposited on the GaN LED + Si bonded pair, followed by 50 nm PECVD Si_3N_4 deposition and densification. The quartz substrate was also subjected to the same PECVD oxide and the nitride deposition processes. After that, the GaN-LED-handle wafer was bonded to quartz substrates. Similar grinding and wet-etching processes (TMAH solution was used in this case) were performed to remove the Si handle wafer to realize the GaN-LED

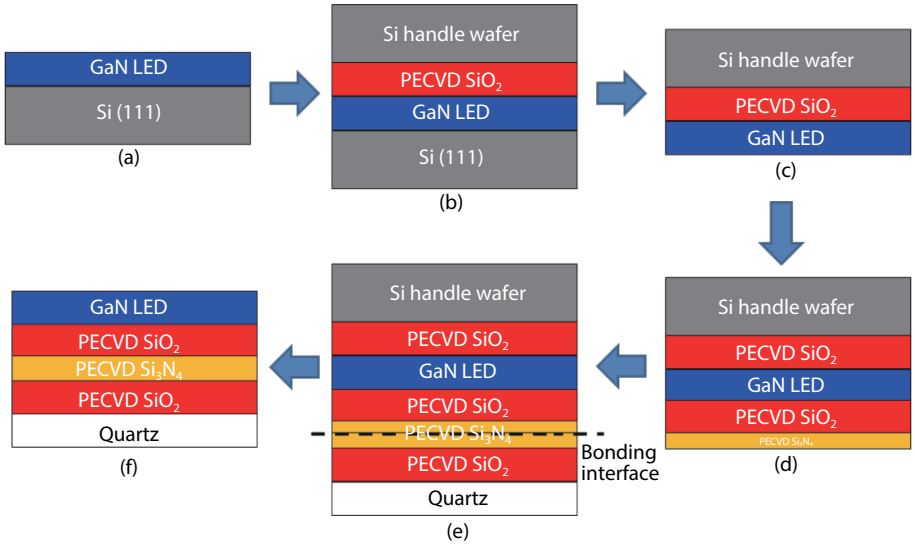

Fig. 32. (Color online) Schematic of the process flow to realize the GaN LED on quartz substrate. (a) A GaN LED epitaxial film on a Si (111) substrate. (b) First wafer bonding between the GaN LED on Si (111) and a Si handle wafers. (c) Removal of the Si (111) substrate. (d) Deposition of SiO_2 and Si_3N_4 layers. (e) Second wafer bonding between the GaN LED-containing handle and a quartz substrate. (f) GaN LED on quartz substrate is realized by releasing the Si handle wafer.

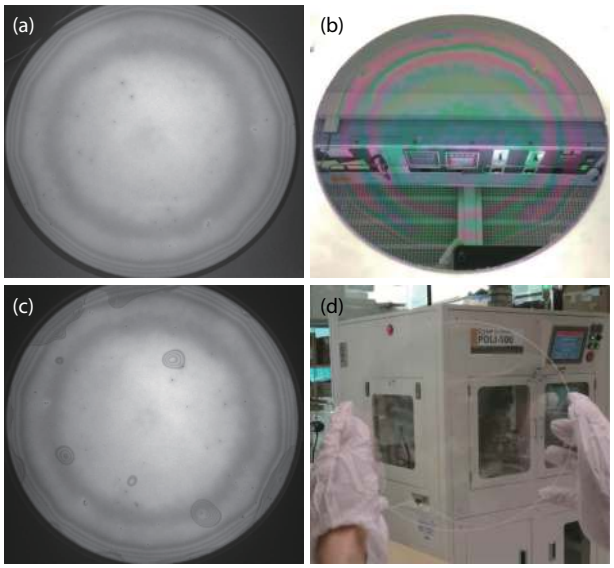

Fig. 33. (Color online) (a) IR image of a bonded GaN LED/Si (111) substrate and a Si handle wafer after step Fig. 32(b). (b) Photograph of the GaN LED layers temporarily attached to the Si handle wafer after Si (111) substrate removal, step Fig. 32(c). (c) IR image of the bonded GaN LED layers containing Si handle wafer and a quartz substrate after step Fig. 32(e). (d) Photograph of the GaN LED transferred to the quartz substrate, step Fig. 32(f).

on the quartz substrate.

As shown in the IR image in Fig. 33(a), the bonding quality between GaN LED on Si (111) substrate and a Si handle wafer is excellent with no observable voids or particles. Fig. 33(c) shows the GaN LED-containing handle wafer has an excellent bonding yield after the Si (111) substrate was removed completely. The bonding quality is slightly degraded due to the presence of undesired particles which cause unbounded areas.

The SEM image shows the cross-sectional view of the layer stack of the GaN LED on the quartz substrate, see Fig. 34. No micro-voids were observed at the bonding interface

Fig. 34. SEM image of the cross-sectional view of the bonded GaN LED on the quartz substrate.

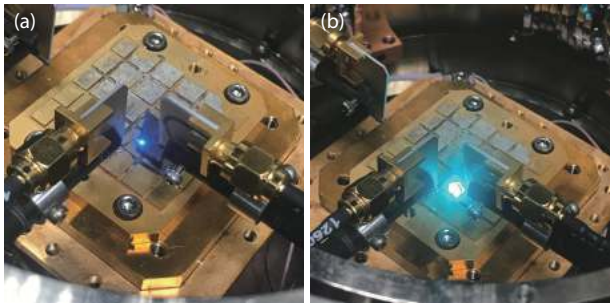

Fig. 35. (Color online) Light-up photo of the GaN LED devices on (a) Si and (b) quartz substrates.

between the two PECVD Si_3N_4 layers. This indicates a successful bonding at the microscale level, with a smooth and uniform bonding interface.

The light-up GaN LEDs on Si and quartz substrate are shown in Fig. 35. The light emitting efficiency is greatly enhanced when the GaN LED epitaxial layers are transferred to the quartz substrate.

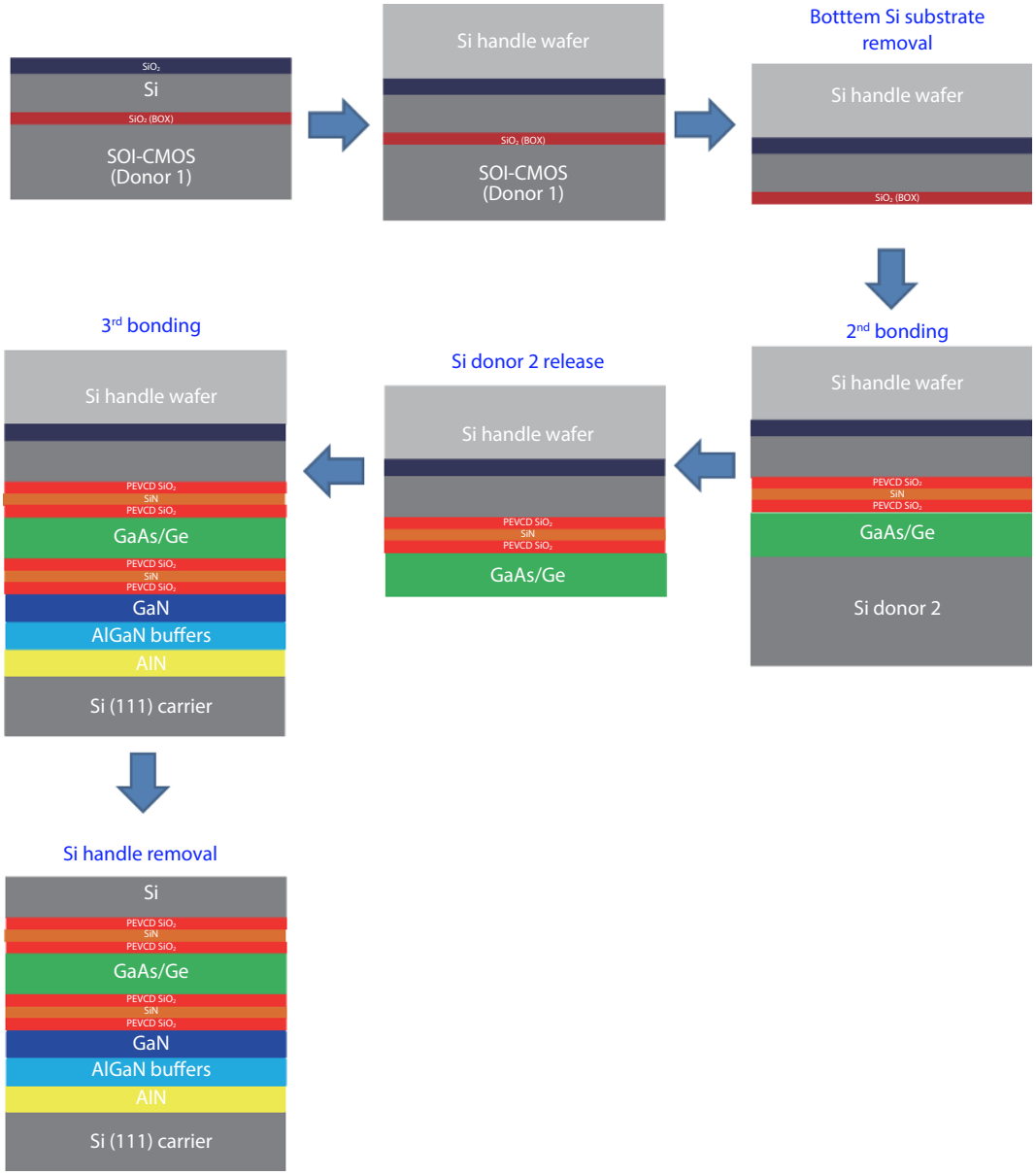

Fig. 36. (Color online) Schematic flow of the multi-bonding and layer transfer process for integration of Si-CMOS and GaAs and GaN together on a common 200 mm Si platform.

3.3. Multi-bonding and layer transfer for multi-wafer stacking

We have successfully demonstrated the integration of the Si-CMOS and III–V/Si or III–N/Si on a common 200 mm Si platform through a double bonding and layer transfer process in the above section. In this section, we would like to further extend the bonding capabilities to multi-layer stacking. Through this method, the integration of Si-CMOS control circuitry, III–As/P and III–N functional materials can be stacked together on a single 200 mm Si platform[69], to realize more complexed functionalities.

Four sets of wafers were prepared in this experiment: (i) Si handle wafer, (ii) silicon-on-insulator (SOI) wafer (with 1.3 μm Si, and 0.4 μm thermally oxidized BOX), (iii) GaAs/Ge/Si (001) donor wafer (GaAs/Ge layer were epitaxially grown on Si(001) wafer with 6° off-cut toward the [110] direction by MOCVD), and (iv) GaN/Si (111) carrier wafer (GaN layer were epitaxially grown on Si (111) wafer by MOCVD). The schematic flow of the bonding and layer transfer process is shown in Fig. 36.

The SOI wafer was first deposited with a 500 nm PECVD oxide, followed by the densification process in a furnace and planarization process by a CMP machine. Then the CMP-ed SOI wafer and Si handle wafers were subjected to O_2 plasma exposure to increase the surface hydrophilicity, followed by rinsing with de-ionized water and spin-dried to clean the wafer surface. After bonding, the same post-bonding annealing and Si substrate removal process were carried out, to realize the SOI layer on Si handle wafer. The details have been discussed in previous sections.

The BOX layer was removed on the SOI containing the Si handle to address the pin-holes issue as discussed previously. Then both the SOI and GaAs/Ge/Si donor wafer were subjected to PECVD oxide and nitride deposition processes for the subsequent bonding. The second bonding process was similar to that described above. After a combination of grinding and chemical etching processes to remove the Si donor

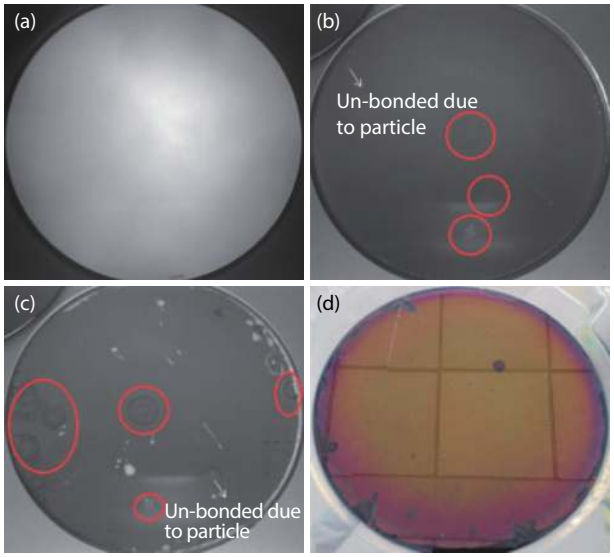

Fig. 37. (Color online) IR image of (a) the first bonding between SOI and Si handle wafer, (b) the second bonding between the SOI-handle and the GaAs/Ge/Si substrate, (c) the third bonding between the GaAs/Ge-SOI-handle and the GaN/Si substrate, and (d) optical image of the SOI-GaAs/Ge/GaN/Si substrate after the triple-bond process. The red circle indicates the defects from the backside of the wafer during TMAH etching caused by the poor adhesion of the protective layer, not affecting the bonding quality.

wafer from the GaAs/Ge/Si substrate, the GaAs/Ge-SOI-containing handle wafer was realized.

The same process was repeated for the third bonding between GaAs/Ge-SOI-handle and GaN/Si carrier substrate. Finally, the SOI-GaAs/Ge/GaN/Si substrate was realized.

From the IR image, as shown in Fig. 37(a), the quality of the first bonding is excellent and no significant voids or particles are observed. For the second bonding, as shown in Fig. 37(b), some unbonded areas are observed, especially at the wafer edge. This is due to the presence of particles trapped between the bonded pairs, which degrade the overall bonding quality. For the third bonding, as shown in Fig. 37(c), more unbonded areas are observed due to the presence of particles from the GaN/Si surface and the unbounded areas originating from the second bonding. Fig. 37(d) shows the optical image of the final SOI-GaAs/Ge/GaN/Si wafer stack.

Cross-sectional TEM is used to assess the quality of the SOI–GaAs/Ge/GaN/Si wafer after the triple-bonding and layer transfer process, as shown in Fig. 38. A smooth and uniform surface with no micro-voids is observed at the two bonding interfaces, indicating a successful bonding at the microscale level.

Through this multi-bonding and layer transfer process, different group III–V and group IV materials with different functionalities can be integrated on a single Si platform. As shown in Fig. 39, it is possible to integrate the Si-CMOS control circuitry, high-frequency devices (e.g., HEMTs on a GaAs layer), and high-power devices (e.g., power amplifier (PA) on a GaN layer) vertically onto a common substrate.

4. Summary and conclusion

In this paper, single-bonding, double-bonding, multi-bonding and layer transfer processes, and its applications have

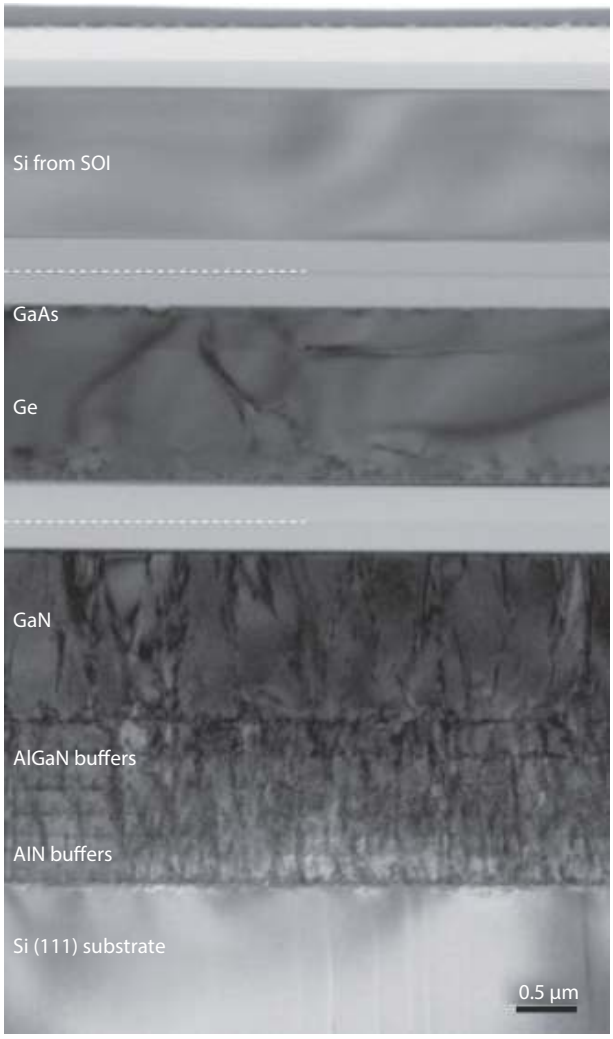

Fig. 38. The cross-sectional TEM of the SOI –GaAs/Ge/GaN/Si stack after the triple-bonding and layer transfer process.

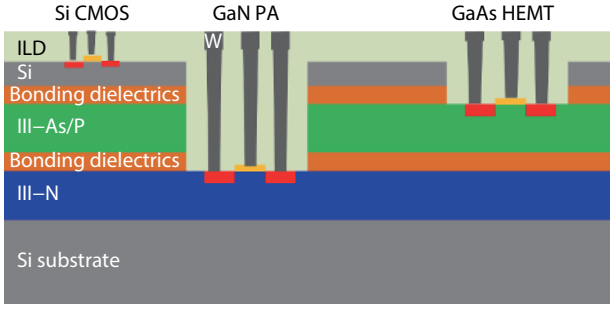

Fig. 39. (Color online) The schematic of Si-CMOS, high frequency GaAs HEMT, and high power GaN PA integrated on a single piece of wafer.

been demonstrated successfully. The associated pin-holes issues, surface roughness issues, bonding yield issues and particle issues have been addressed.

By the DWB and layer transfer processes, integration of Si-CMOS (on SOI) and III–V or III–N compound semiconductors (e.g., InGaAs HEMT, AlInGaP LED, GaN HEMT, or InGaN LED) on a common Si substrate is demonstrated. In addition, high temperature III–V or III–N materials growth can be completed without the presence of the CMOS layer, hence damage to the CMOS layer can be avoided.

The monolithic integration of Si-CMOS + III–V devices on a common Si platform enables a new generation of systems

with more functionality, better energy efficiency, and smaller form factor. This paves the way for new circuits and applications such as ultra-efficient circuits for handheld, mobile or remote applications, self-sensing and self-tuning/self-configuring circuits, and RGB (red, green, blue) micro-LED arrays with control circuitry, etc.

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