REVIEWS

Journal of Semiconductors
(2021) 42, 023101
doi: 10.1088/1674-4926/42/2/023101

Mobility enhancement techniques for Ge and GeSn MOSFETs

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Abstract: The performance enhancement of conventional Si MOSFETs through device scaling is becoming increasingly difficult. The application of high mobility channel materials is one of the most promising solutions to overcome the bottleneck. The Ge and GeSn channels attract a lot of interest as the alternative channel materials, not only because of the high carrier mobility but also the superior compatibility with typical Si CMOS technology. In this paper, the recent progress of high mobility Ge and GeSn MOSFETs has been investigated, providing feasible approaches to improve the performance of Ge and GeSn devices for future CMOS technologies.

Key words: germanium; germanium-tin; MOSFET; mobility

Citation: R Cheng, Z Chen, S C Yuan, M Takenaka, S Takagi, G Q Han, and R Zhang, Mobility enhancement techniques for Ge and GeSn MOSFETs[J]. *J. Semicond.*, 2021, 42(2), 023101. http://doi.org/10.1088/1674-4926/42/2/023101

1. Introduction

In the past few decades, the device scaling of Si metal–oxide–semiconductor field-effect transistors (MOSFETs), following Moore's Law, drives the fast development of complementary metal–oxide–semiconductor (CMOS) integrated circuits[1–3]. Recently, the performance enhancement of Si MOSFETs is increasingly difficult to achieve as the conventional device scaling is approaching its physical limit[4]. Higher channel mobility is effective to improve the MOSFETs performance, which has been well demonstrated by the application of strained-Si techniques[5, 6]. However, advanced MOSFET technology is still desired to further improve the performance of CMOS' devices. Alternative channel materials with mobility higher than Si have been attracting a lot of interest for the potential to improve the MOSFET performance. Among these high mobility materials, Ge and GeSn are promising candidates owing to their high mobility as well as the superior integrability on the Si platform[7–12].

It is essential to employ the high-*k* dielectrics (such as Al_2O_3, HfO_2, etc.) for thinner equivalent oxide thickness (EOT), to satisfy the requirement of device scaling. Although the thin EOT high-*k*/Ge and high-*k*/GeSn MOSFETs have been demonstrated, the relatively low inversion carrier mobility severely limits the application of Ge and GeSn channels. This phenomenon attributes to the large interface state density (D_{it}) at the Ge and GeSn metal–oxide–semiconductor (MOS) interfaces, especially for the ultrathin Ge and GeSn gate stacks[13–18]. Thus the suppression of D_{it} in ultrathin EOT high-*k*/Ge and high-*k*/GeSn gate stacks would be one of the key issues to be resolved, in order to obtain high performance Ge and GeSn MOSFETs.

In this paper, the MOS interface passivation techniques from our previous work will be summarized for Ge and GeSn MOSFETs. Ge and GeSn MOSFETs with ultrathin EOT and superior channel mobility have been demonstrated, suggesting the great potential of Ge and GeSn MOSFETs as the alternative device structures in future advanced CMOS technologies.

2. Ge MOSFETs

2.1. EOT scaling and MOS interface passivation

Because of the large D_{it} at direct high-*k*/Ge interface, an interfacial layer (IL) is necessary to obtain the high mobility in Ge MOSFETs. It has been confirmed that the thermally oxidized GeO_2/Ge interfaces are effective to passivate the Ge MOS interface, with a GeO_2 thickness of ~20 nm[19–21]. However, the relatively low permittivity of GeO_2 (5–6) requires the aggressive scaling down of the GeO_2 thickness to achieve an ultrathin EOT high-*k*/GeO_2/Ge gate stack. Unfortunately, it is difficult to fabricate a thin GeO_2/Ge MOS interface with superior interface qualities, since the D_{it} in the IL significantly increases as the GeO_2 thickness decreases[22, 23]. Therefore, the D_{it} reduction for thin GeO_2/Ge MOS interfaces is one of the technical bottlenecks for the realization of high-performance Ge pMOSFETs.

To fabricate ultrathin Ge MOS interfaces with low D_{it}, a plasma post oxidation (PPO) method was proposed by using oxygen plasma exposure to oxidize the high-*k*/Ge interface (Fig. 1), yielding a high-*k*/GeO_x/Ge gate stack[22, 24–25]. Here the high-*k* layer serves as a protecting layer to prevent damage to GeO_x IL from the subsequent device fabrication process, and also as a sufficient oxygen barrier that suppresses the growth of unnecessarily thick GeO_x IL. Fig. 2 shows the angel-resolved X-ray photoelectron spectroscopy (AR-XPS) spectra taken from an Al_2O_3 (1 nm)/Ge structure after PPO. The in-

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Received 22 SEPTEMBER 2020; Revised 2 DECEMBER 2020.

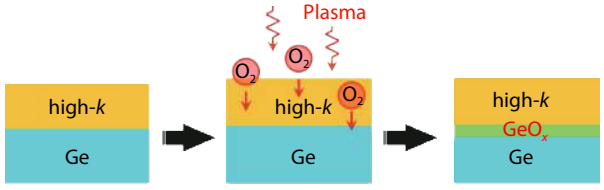

Fig. 1. (Color online) The fabrication process of the high-k/GeO_x/Ge gate stacks with PPO method.

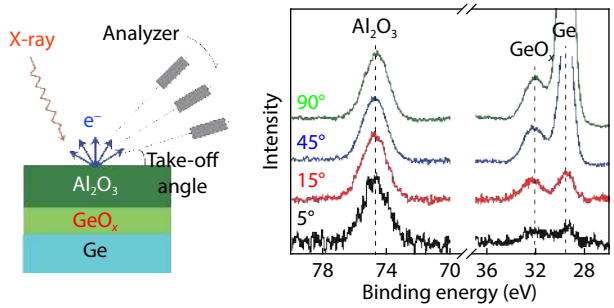

Fig. 2. (Color online) The AR-XPS spectra taken from an 1-nm-thick Al_2O_3/Ge structure with 650 W PPO for 10 s.

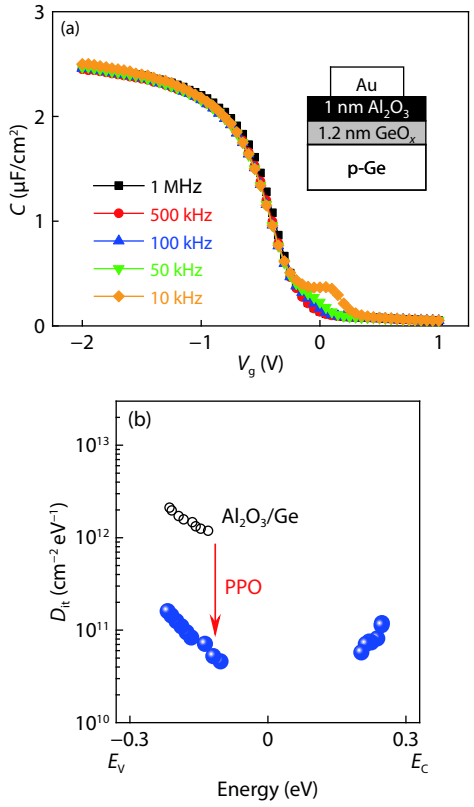

Fig. 3. (Color online) (a) The C–V characteristics of an Au/Al_2O_3 (1 nm)/GeO_x (1.2 nm)/Ge MOS capacitor fabricated with the PPO method. (b) The D_{it} at the Al_2O_3/Ge MOS interfaces w/ and w/o PPO treatment.

tensity of the Ge 3d peak corresponding to GeO_x decreases more pronounced than that of the Al 2p peak corresponding to Al_2O_3, from which it is confirmed that the GeO_x is formed underneath the Al_2O_3 layer after PPO.

The electrical properties of the PPO GeO_x/Ge MOS interfaces were investigated using the Au/Al_2O_3/GeO_x/Ge MOS capacitors. Fig. 3(a) shows the C–V curves of an Au/Al_2O_3 (1 nm)/GeO_x (1.2 nm)/Ge MOS capacitor fabricated by PPO. The superior C–V characteristics are observed with an EOT of

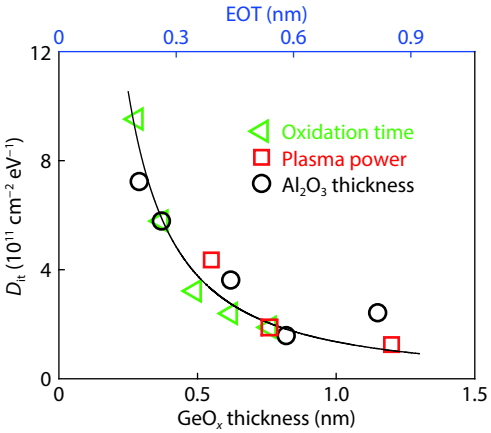

Fig. 4. (Color online) The D_{it} at E_i – 0.2 eV taken from PPO Al_2O_3/GeO_x/Ge MOS interfaces fabricated with different Al_2O_3 capping thickness, plasma power and oxidation time.

1.06 nm. The D_{it} of this MOS capacitor was evaluated by the low temperature conductance method with the correction of surface potential fluctuation[26–29]. It is found that the reduction in D_{it} by one order of the magnitude is obtained after the PPO, as compared with that of the direct Al_2O_3/Ge MOS interface (Fig. 3(b)). The minimum D_{it} detected in this MOS capacitor is 5×10^{10} cm^{-2} eV^{-1}. These results show a clear correlation between the high-k/Ge MOS interface quality with the existence of GeO_x IL. The relationship between the GeO_x/Ge MOS interface quality and the GeO_x IL thickness is further studied. Here, the Al_2O_3 layer thickness (1 to 1.5 nm), oxygen plasma power (300 to 650 W), and plasma oxidation time (5 to 30 s) were varied to obtain different GeO_x IL thicknesses. A thinner GeO_x IL can be realized by lowering the plasma power, shortening the oxidation time, and increasing the thickness of the Al_2O_3 layer, which is attributable to the reduced diffusion of oxygen species through the Al_2O_3 layer. The GeO_x ILs with the thickness ranging from 1.2 to 0.23 nm can be grown by changing the PPO conditions. Fig. 4 shows the D_{it} at the energy of E_i – 0.2 eV for the Au/Al_2O_3/GeO_x/Ge MOS capacitors as a function of the GeO_x IL thickness, fabricated with various conditions. It is found that the D_{it} values of the Au/Al_2O_3/GeO_x/Ge MOS capacitors fabricated with different conditions generally obey the universal relationship against the GeO_x thickness. These results indicate that D_{it} at GeO_x/Ge MOS interface is determined by neither the Al_2O_3 thickness nor the plasma conditions, but by the thickness of GeO_x IL only. It is observed from this relationship that a significant degradation of D_{it} at the MOS interfaces starts around 0.5 nm. This phenomenon suggests that a GeO_x IL with the thickness of one GeO_2 unit cell (0.5–0.57 nm[30]), can sufficiently passivate a Ge MOS interface. This physical thickness of 0.5 nm corresponds roughly to a EOT of 0.35 nm under an assumption that the permittivity of GeO_x is 5.5. As a result, the GeO_x/Ge MOS interfaces with D_{it} lower than half of 10^{11} cm^{-2} eV^{-1} can be realized at the expense of increasing EOT by ~0.35 nm.

The GeO_x IL shows a superior scalability to maintain the low D_{it} for Ge MOS interfaces, indicating a possibility to realize high quality Ge gate stacks with ultrathin EOT. The suppression of EOT contributed by a high-k layer is also important. The formation of high quality GeO_x/Ge MOS interfaces has been studied for HfO_2/Ge structures. The strong inter-mixing between HfO_2 and Ge at high temperature induces the genera-

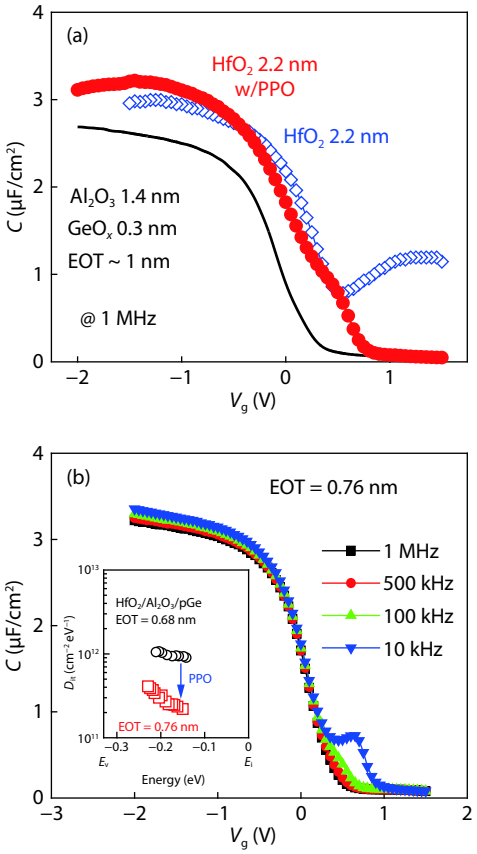

Fig. 5. (Color online) (a) The *C*–*V* curves of the Au/HfO_2/p-Ge MOS capacitors w/ and w/o PPO, compared with that of Au/Al_2O_3/GeO_x/p-Ge MOS capacitor. (b) The *C*–*V* curves of of the Au/HfO_2/Al_2O_3/p-Ge MOS capacitor after PPO. The inset of it shows the energy distribution of D_{it} of this MOS capacitor.

tion of MOS interface defects[31, 32]. Thus, the HfO_2/Al_2O_3/Ge structure was used as the starting sample for PPO instead of the direct HfO_2/Ge structure. Fig. 5(a) shows the *C*–*V* characteristic of an Au/Al_2O_3/GeO_x/p-Ge MOS capacitor after PPO, as compared with that of the Au/HfO_2 (2.2 nm)/p-Ge MOS capacitors w/ and w/o PPO. It is found that the capacitance increases for the gate stack using the HfO_2 dielectrics, thanks to its large permittivity. However, the Au/HfO_2 (2.2 nm)/p-Ge MOS capacitor shows a large stretch-out of the *C*–*V* curve even after PPO, suggesting that the PPO method is not effective to the HfO_2/Ge gate stacks. This phenomenon is attributable to the significant degradation of Ge MOS interface quality and generation of D_{it} due to the $HfGeO_x$ formation induced by the HfO_2–Ge inter-mixing. In contrast, the good *C*–*V* characteristics of the Au/HfO_2/Al_2O_3/GeO_x/p-Ge MOS capacitor indicate the sufficient passivation of the Ge MOS interface. The hysteresis of the *C*–*V* curves is ~150 mV for this MOS capacitor with a sweep scan from 1 to –1.5 V (data not shown), which is attributable to the slow traps in the HfO_2 layer. A much smaller hysteresis was confirmed for the Al_2O_3/GeO_x/Ge gate stack even with a much thicker EOT[22]. It is evaluated from a germanium based *C*–*V* simulator that the EOT of this MOS capacitor is 0.76 nm. The evaluated D_{it} values are plotted as a function of energy in the inset of Fig. 5(b). It is found that D_{it} of the Au/HfO_2/Al_2O_3/GeO_x/Ge MOS capacitor is suppressed by around one order of magnitude through PPO and that a minimum D_{it} value of 2 × 10^{11} cm^{-2} eV^{-1} is detected in this MOS capacitor. It is confirmed from the transmission electron microscopy (TEM) image that this gate stack is composed of HfO_2/Al_2O_3/GeO_x/Ge structure (Fig. 6). The ~0.55-nm-thick interfacial layer is observed between the 2.2-nm-thick HfO_2 layer and the Ge substrate, corresponding to the 0.2-nm-thick Al_2O_3 diffusion control layer and the 0.35-nm-thick GeO_x interfacial layer.

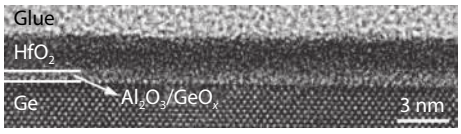

Fig. 6. The cross section TEM image of an HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/Ge structure after 15 s' PPO using 500 W plasma.

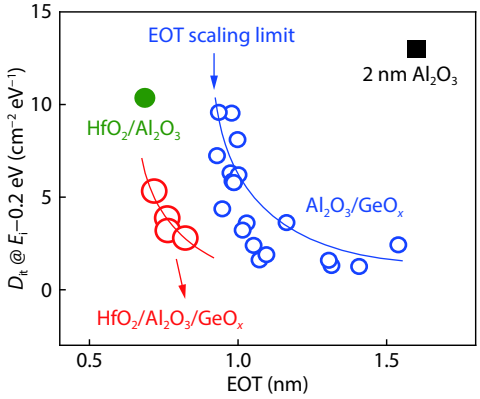

Fig. 7. (Color online) The D_{it} at the energy of E_i – 0.2 eV of the HfO_2/Al_2O_3/GeO_x/Ge and Al_2O_3/GeO_x/Ge gate stacks, as a function of EOT.

The impact of the PPO time on D_{it} and EOT of the Au/HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/GeO_x/p-Ge MOS capacitors were examined. The D_{it} values at E_i – 0.2 eV of these MOS capacitors are summarized in Fig. 7 as a function of EOT. The D_{it} taken from the PPO Al_2O_3/GeO_x/Ge gate stacks is also shown for comparison. Due to the drastic increase of the gate leakage of the Al_2O_3/GeO_x/Ge gate stacks with decreasing Al_2O_3 thickness, the thickness of GeO_x IL has to be reduced to further scale down the EOT of Al_2O_3/GeO_x/Ge gate stacks. As a result, the clear degradation of the MOS interface quality is observed as EOT approaches ~1 nm for Al_2O_3/GeO_x/Ge gate stacks because of the insufficient GeO_x IL thickness[24]. On the other hand, further EOT scaling is realized down to 0.7–0.8 nm for the HfO_2/Al_2O_3/GeO_x/Ge gate stacks because of the higher permittivity of HfO_2. A rapid reduction of D_{it} at E_i – 0.2 eV is observed from 5.3 to 3.9, 3.2, until 2.8 × 10^{11} cm^{-2} eV^{-1} with an increase in the PPO time from 5 to 10, 15, until 25 s for the HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/Ge gate stacks which have EOT of 0.72, 0.75, 0.76 and 0.82 nm, respectively. It is also confirmed from these results that the GeO_x IL is necessary to maintain low D_{it} at the Ge MOS interface.

It is noted that in the HfO_2/Al_2O_3/GeO_x/Ge gate stacks, the thickness of the HfO_2 layer was fixed at 2.2 nm to sufficiently suppress the gate leakage, while the EOT scaling capability of this gate stack structure is dominated by the GeO_x IL thickness. Thus, it is still challenging to realize Ge gate stacks with thinner EOT but decently passivated MOS interface. Additionally, due to the directional nature of the oxygen plasma, it is difficult to realize an isotropic oxidation to 3D-structured Ge channels with the oxygen plasma. This phenomenon re-

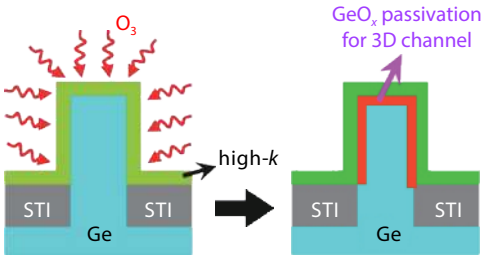

Fig. 8. (Color online) The schematic illusion of the ozone post oxidation process.

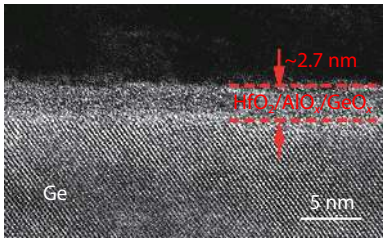

Fig. 9. Cross section TEM of an HfO_2 (2 nm)/Al_2O_3 (0.3 nm)/Ge structure after OPO for 60 s at 300 °C.

duces the effectiveness of the PPO method to Ge FinFET or Ge gate-all-around devices, which are the most promising device structures for future Ge CMOS technology.

To solve these problems, an ozone post oxidation (OPO) was employed to form ultrathin Ge gate stacks with an isotropic oxidation (Fig. 8). After the ALD deposition of HfO_2/Al_2O_3/Ge structures, the *in-situ* OPO was carried out at 300 °C in the 10% O_3/O_2 ambient with a pressure of ~100 Pa. The formation of the GeO_x/Ge interface by OPO was examined by the cross-sectional TEM observation. As shown in Fig. 9, the gate stack with 60 s OPO shows a total physical thickness of 2.7 nm after 60 s OPO, indicating the growth of 0.4-nm-thick GeO_x IL compared with the gate stack before OPO (2 nm HfO_2/0.3 nm Al_2O_3). Here, the 0.3-nm-thick Al_2O_3 layer serves as a blocking layer to prevent the inter-mixing between HfO_2 and GeO_x during OPO. The partially crystallized HfO_2 regions were observed in the HfO_2 layer, which results in the increase of k value for HfO_2[33]. The crystallization of HfO_2 after OPO might be attributed to the slight Ge diffusion into the HfO_2 film. Similar phenomena have also been reported in literature that the cubic phase HfO_2 could be stabilized by Ge doping[34–37]. As a result, the EOT of the HfO_2/Al_2O_3/GeO_x/Ge gate stack is suppressed by the OPO treatment, and the ultrathin EOT of 0.6 nm has been obtained for the HfO_2/Al_2O_3/GeO_x/Ge gate stack with 60 s OPO. On the other hand, the EOT of the OPO HfO_2/Al_2O_3/GeO_x/Ge gate stack is thinner than the as-deposited HfO_2/Al_2O_3/Ge gate stack (0.82 nm), although the total physical thickness of the gate stack increases after OPO due to the GeO_x IL growth. This phenomenon is also observed for the HfO_2/Al_2O_3/GeO_x/Ge gate stacks with different Al_2O_3 layer thicknesses of 0.1 and 0.2 nm (Fig. 10). The relationship between D_{it} and EOT of the OPO HfO_2/Al_2O_3/GeO_x/Ge gate stacks is shown in Fig. 11, as compared with the PPO gate stacks. It is found that the D_{it} in the PPO HfO_2/Al_2O_3/GeO_x/Ge and Al_2O_3/GeO_x/Ge gate stacks increase rapidly with the scaling down of the total EOT because it is mandatory to sacrifice the GeO_x IL thickness during EOT scaling. The trade-off between EOT and D_{it} severely

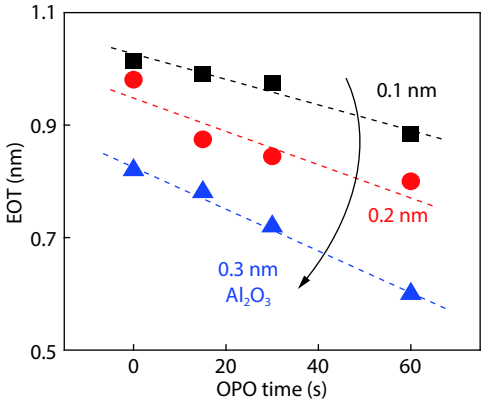

Fig. 10. (Color online) The EOT of the OPO HfO_2/Al_2O_3/GeO_x/Ge gate stacks with different Al_2O_3 thicknesses and OPO times.

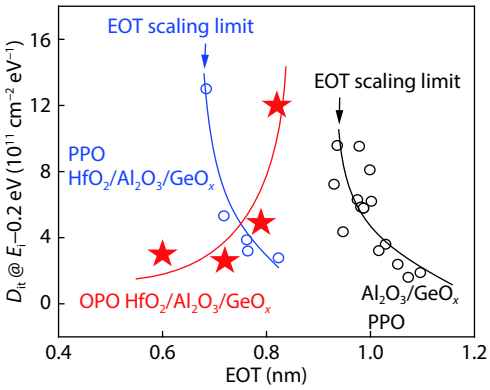

Fig. 11. (Color online) The D_{it} at the energy of E_i – 0.2 eV in OPO HfO_2/Al_2O_3/GeO_x gate stacks, compared with the PPO gate stacks as a function of EOT.

limits the scalability of these PPO gate stacks. In contrast, the lower D_{it} is obtained for the OPO HfO_2/Al_2O_3/GeO_x/Ge gate stacks with thinner EOT by increasing the OPO time, since the HfO_2 crystallization compensates the EOT increase contributed by GeO_x IL. These phenomena indicate that the OPO HfO_2/Al_2O_3/GeO_x/Ge gate stack features the superiority of both D_{it} suppression and EOT scalability, which is a promising gate stack technique for the future high performance Ge MOSFETs.

The effectiveness of the OPO method to the 3D-structured Ge channels was also examined using a series of Ge fins with the same fin height and different fin widths. The EOT on the sidewall and the EOT on the fin top are extracted for the PPO Al_2O_3/GeO_x/Ge and the OPO HfO_2/Al_2O_3/GeO_x/Ge gate stacks. As shown in Fig. 12, the PPO Al_2O_3/GeO_x/Ge gate stack has a thinner oxide thickness on the sidewall region than that at the bottom region, due to the insufficient formation of GeO_x IL at the sidewall. In contrast, the OPO HfO_2/Al_2O_3/GeO_x/Ge gate stack shows almost the same oxide thickness for sidewall and bottom regions, meaning that the OPO exhibits an isotropic formation of GeO_x IL. These results indicate the feasibility of OPO passivation for 3D-structured Ge channels.

2.2. Ultrathin EOT and high mobility Ge MOSFETs

The Ge MOSFETs have been demonstrated with the ultrathin EOT HfO_2/Al_2O_3/GeO_x gate stacks with OPO treatment. Gate first process was employed to fabricate the Ge MOS-

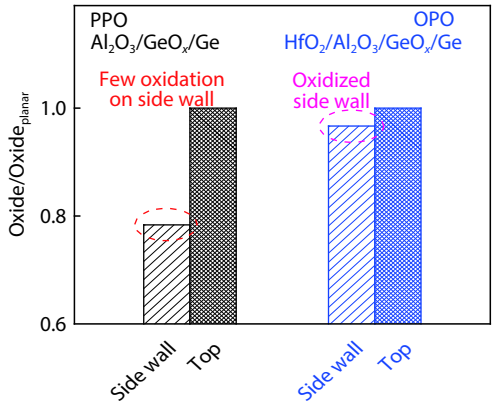

Fig. 12. (Color online) The oxide thickness of the PPO and OPO gate stacks at side wall and top regions of a 3D structured Ge channel.

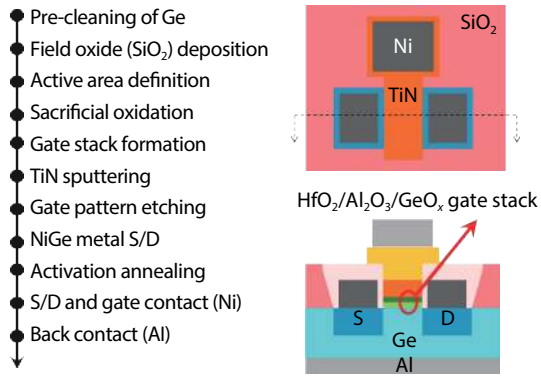

Fig. 13. (Color online) The fabrication process of the Ge MOSFETs with OPO $HfO_2/Al_2O_3/GeO_x$ gate stacks.

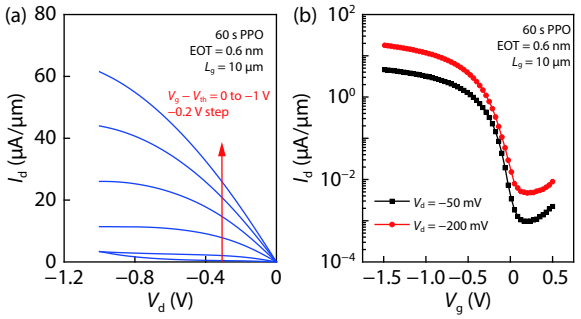

Fig. 14. (Color online) The I_d–V_d (a) and I_d–V_g (b) characteristics of an (100)/<110> $HfO_2/Al_2O_3/GeO_x$/Ge pMOSFET fabricated by 60 s OPO.

FETs with a structure shown in Fig. 13. The (100) n-Ge substrates with a resistivity of 1–10 Ω·cm were used. The SiO_2 field oxide was deposited and the active areas were defined by etching off the SiO_2. The $HfO_2/Al_2O_3/GeO_x$ gate stacks were fabricated, and TiN gate electrodes were sputtered for the compatibility of process integration. The NiGe metal S/D structures were formed by Ni deposition and

NiGe metallization at 400 °C for 1 min. Finally, Ni contact pads were deposited on gate and S/D regions by thermal evaporation, for electrical characterization.

Figs. 14(a) and 14(b) show the I_d–V_d and I_d–V_g characteristics of an $HfO_2/Al_2O_3/GeO_x$/Ge pMOSFETs with 60 s OPO, respectively. The ON/OFF ratios of the NiGe S/D pMOSFETs are ~3.5 orders of magnitude. The S factor of 85 mV/decade could be obtained for the device, which corresponds to a D_{it} of 2.3 × 10^{12} cm^{-2} eV^{-1} and agrees well with the D_{it} measured by the conductance method. The normal operations of the Ge pMOSFETs with different OPO times are also observed (data not shown). The effective hole mobility of the Ge pMOSFETs were evaluated by the split *C*–*V* method. Fig. 15 shows the hole mobility in $HfO_2/Al_2O_3/GeO_x$/Ge pMOSFETs with different OPO times. The Ge pMOSFETs with OPO $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks exhibit a much better improved hole mobility than that in HfO_2/Al_2O_3/Ge pMOSFETs, attributing to the MOS interface passivation by OPO treatment. The peak hole mobility of 130, 332, 417 $cm^2/(V{\cdot}s)$ were achieved with ultrathin EOT of 0.78, 0.72, and 0.58 nm, respectively. Conventionally, the mobility decreases with the scaling down of EOT for Ge MOSFETs, due to the degradation of MOS interfaces in the thinner gate stacks. However, it is interestingly noted that the hole mobility in the OPO $HfO_2/Al_2O_3/GeO_x$/Ge pMOSFETs increases with the decrease of EOT. This phenomenon is attributable to the different mechanisms of EOT scaling by OPO treatment and the conventional interface engineering techniques for Ge gate stacks. The EOT scaling was achieved by the permittivity enhancement of HfO_2 after OPO treatment for the $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks, rather than the decrease of GeO_x interfacial layer thickness obtained from the conventional Ge gate stack treatments. Thus, the EOT scaling and mobility improvement are both realized for the OPO $HfO_2/Al_2O_3/GeO_x$/Ge MOSFETs.

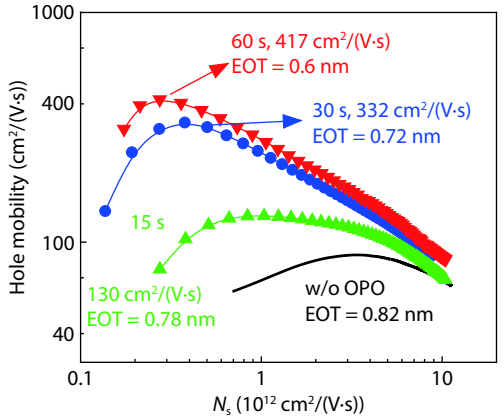

Fig. 15. (Color online) The hole mobility in $HfO_2/Al_2O_3/GeO_x$/Ge pMOSFET fabricated by OPO with different oxidation times, compared with that in the HfO_2/Al_2O_3/Ge pMOSFET.

3. GeSn MOSFETs

3.1. MOS interface passivation

From the viewpoint of pursuing high mobility transistors, the alternative semiconductor materials are desired to further improve the CMOS performance. Although the Ge MOSFETs show promising properties to achieve an enhanced performance than the Si MOSFETs, the alternative channel materials are still mandatory for higher mobility MOSFETs. The GeSn channel MOSFETs are investigated as one of the possible solutions for future high mobility MOSFETs, especially for the high mobility pMOSFET applications. In contrast to the superior interface qualities of oxidation SiO_2/Si and GeO_2/Ge MOS interfaces, the oxidation $GeSnO_x$/GeSn interface exhibits relatively high defect density[17]. Thus the passivation of GeSn MOS interface is one of the key issues that needs to be resolved in order to realize high-performance GeSn MOSFETs.

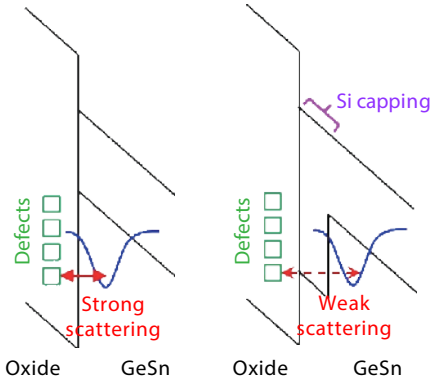

Fig. 16. (Color online) The mechanism of suppressed carrier scattering in the Si passivated GeSn channel, compared with the direct oxide/GeSn channel.

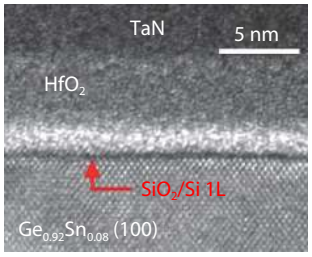

Fig. 17. The cross section TEM image of a GeSn MOS structure having the Si passivation.

Thanks to the different electrical potentials of the valence band of Si and GeSn, the Si IL passivation indicates a promising solution for GeSn MOS devices[38–40]. Due to the carrier confinement effect, the holes are repelled from the gate dielectric interface, resulting in a GeSn quantum well layer with a decreased inversion carrier scattering with reduced Coulomb and surface roughness scattering centers (Fig. 16).

The Si passivation layers are grown on the surface of 6-nm-thick (100), (110) and (111) $Ge_{0.92}Sn_{0.08}$/Ge structures using MBE, with Si_2H_6 as the precursor. Fig. 17 shows the cross-section TEM image of a GeSn pMOSFET fabricated with the Si passivated GeSn substrate. Uniform layer thickness and sharp interface are observed for the Si/GeSn structure, indicating the successful formation of the GeSn quantum well channel. The pMOSFET devices with Si passivated $Ge_{0.92}Sn_{0.08}$ quantum well channels were fabricated with a gate first process. The TaN/HfO_2 gate stacks were deposited on the Si/GeSn/Ge structures, followed by a post deposition annealing at 450 °C. After the gate patterning, the boron implantation and activation annealing were carried out to form the source/drain regions. The fabricated GeSn pMOSFETs exhibit normal operations as indicated by the I_d–V_g and I_d–V_d characteristics (Fig. 18). The peak mobility of 685, 745, and 845 $cm^2/(V{\cdot}s)$ are obtained for (100), (110), and (111) GeSn pMOSFETs, respectively (Fig. 19). Additionally, the (100), (110), and (111) GeSn pMOSFETs exhibit the mobility of 445, 571, and 576 $cm^2/(V{\cdot}s)$ at an N_s of 10^{13} cm^{-2}, which is improved by 1.5 times as compared with those in the Ge pMOSFET control sample. The much higher hole mobility in the GeSn pMOSFETs as compared with that in Ge pMOSFETs are attributable to the high bulk mobility in GeSn and the carrier confinement effect by the Si passivation layer.

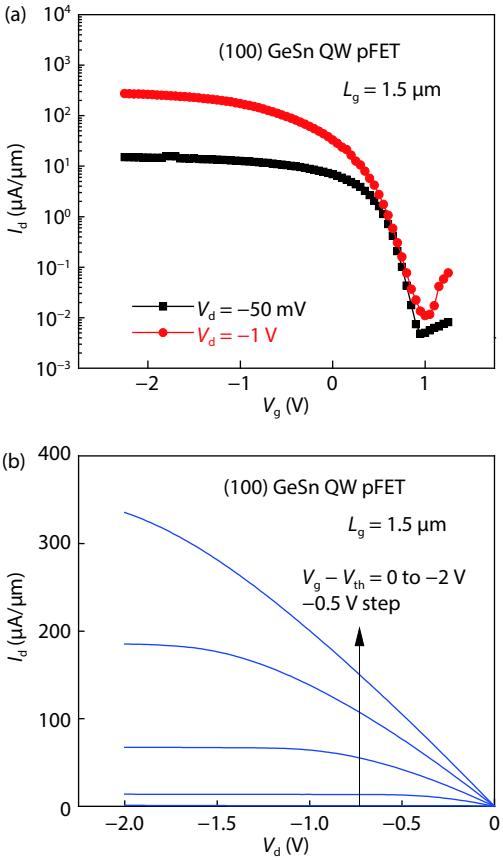

Fig. 18. (Color online) (a) I_d–V_g and (b) I_d–V_d characteristics of the (100) GeSn QW pMOSFET with Si passivation.

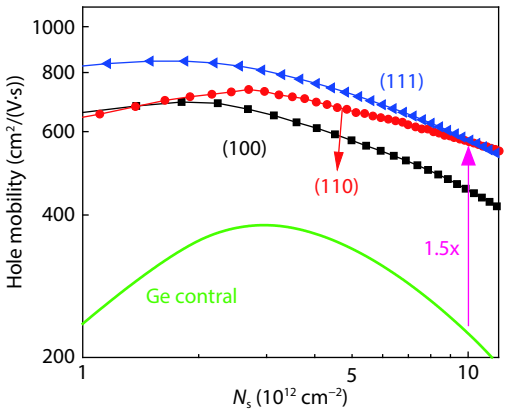

Fig. 19. (Color online) The hole mobility in the Si passivated GeSn QW pMOSFETs with different channel orientations of (100), (110) and (111).

3.2. Channel strain engineering

Beside of the MOS interface passivation, the strain engineering is also an effective performance booster to improve the mobility for GeSn pMOSFETs. It is found that the compressive strain induces the reduction of the hole effective mass and valence band edge lifting for GeSn channels, resulting in a higher hole mobility, which is similar to those in strained SiGe and Ge channels[5, 41–45]. Thus, it is essential to obtain the higher hole mobility in GeSn channels by enhancing the compressive strain. Since the GeSn channels are typically epitaxially grown on Si or Ge surfaces, the advantage of compressive strain for hole mobility improvement is expected to increase by improving the Sn composition in the GeSn channel.

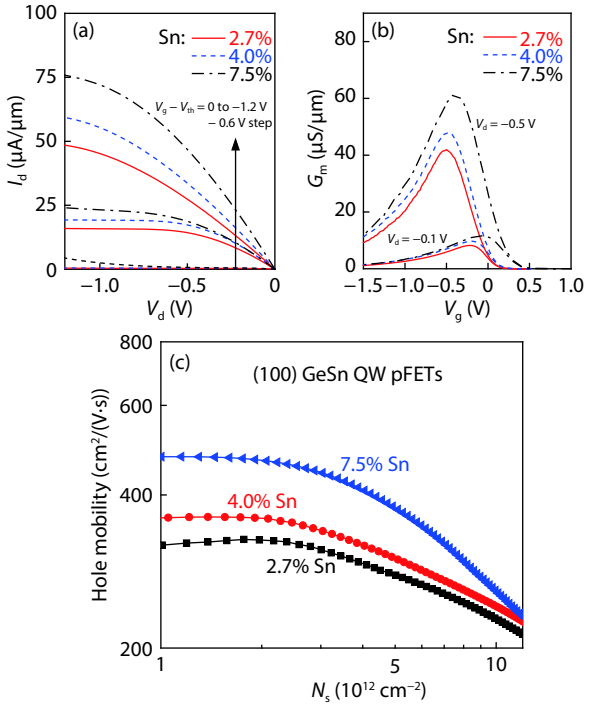

Fig. 20. (Color online) The comparison of (a) I_d– V_d curves, (b) G_m curves and (c) hole mobility of GeSn QW pMOSFETs with different Sn contents of 2.7%, 4.0% and 7.5%.

The 11-nm-thick GeSn channels were grown on (100) Ge surfaces with different Sn contents of 2.7%, 4.0%, and 7.5%, respectively. As a result, the biaxial compressive strain of 0.50%, 0.73%, and 1.35% were obtained in the GeSn channels. The *in-situ* Si_2H_6 treatment was employed to form the SiO_2/Si passivation for GeSn channels, to suppress the inversion carrier scattering by MOS interface defects. It is confirmed from the cross-sectional TEM image that the total thickness of SiO_2/Si passivation layers is ~1 nm for all samples, giving the same MOS interface passivation effect for GeSn channels with different Sn contents.

Fig. 20(a) shows the I_d–V_d characteristics of the GeSn pMOSFETs with different Sn contents of 2.7%, 4.0% and 7.5%. The I_d increase has been obtained for the GeSn pMOSFETs with the increased Sn content, which is attributable to the mobility enhancement. A similar phenomenon is also observed in the transconductance curves of these devices (Fig. 20(b)). It is also noted that the OFF-state current is larger for the GeSn pMOSFET with a higher Sn content, possibly caused by the reduced band gap due to the valent band edge lifting. The hole mobility in the GeSn pMOSFETs with different Sn contents are shown in Fig. 20(c). The improved hole mobility is confirmed for the GeSn pMOSFETs with an increase of Sn content, as theoretically predicted. The peak mobility of 340, 378, and 496 cm^2/(V·s) are achieved for the GeSn pMOSFETs with Sn contents of 2.7%, 4.0%, and 7.5%, respectively.

The physical origin of the enhanced hole mobility in the GeSn channel with increased Sn content is investigated by performing the subband calculation using the 8 × 8 *k·p* method, Schrödinger equation, and Poisson equation, with the material parameters taken from the Refs. [46, 47]. Fig. 21 shows the equi-energy contour plots of heavy hole (HH) bands for GeSn with different Sn contents of 2.7%, 4.0%, and 7.5%. It is found that the effective mass of hole decreases with the increase of Sn content, which is responsible for the increase of hole mobility in GeSn pMOSFETs.

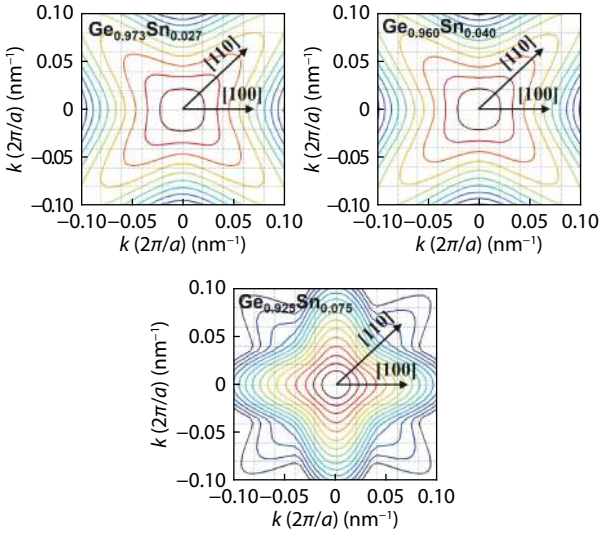

Fig. 21. (Color online) The equienergy contours of heavy hole subband for GeSn pMOSFETs with different Sn contents of 2.7%, 4.0% and 7.5%, at a N_s of 5 × 10^{12} cm^{-2}. The equienergy contour lines are for multiples of 20 meV.

4. Conclusion

The Ge and GeSn channel MOSFETs have been examined to further improve the performance of CMOS technology. It is found that through the interface passivation with ultrathin GeO_x layer grown by plasma post oxidation method, the mobility of Ge MOSFETs is sufficiently improved due to the D_{it} reduction. In addition, it is also confirmed that the Si passivation technique is an effective technique to enhance the mobility in the GeSn channel by suppressing the carrier scattering and reducing the hole effective mass especially for transistors with higher Sn content. These results indicate that the Ge and GeSn channels are one of the most promising solutions to realize future high-performance CMOS devices.

Acknowledgements

This work was supported, in part, by the Zhejiang Provincial Natural Science Foundation of China under Grant LR18F040001 and in part by the Fundamental Research Funds for the Central Universities.

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