COMMENTS AND OPINIONS

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Design technology co-optimization towards sub-3 nm technology nodes

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Over the past half century, Moore's Law has played a crucial role in the development of the semiconductor field, which depends on straightforwardly dimensional scaling with approximately a two-year cadence. Significant benefits of performance, power, area, and cost (PPAC) in microchips are expected at each technology node. However, aggressive pitch-based scaling by resolution enhancement techniques becomes increasingly challenging to sustain. Short-channel effects, e.g. high leakage current, drain induced barrier lowering effect, deteriorate the device performance greatly. Therefore, the migration of device architecture from planar to 3D fin structures has been adopted to continue the pace of further scaling due to superior electrostatic controllability. Currently, the gate length at 5 nm technology node in 2020 is shrunk incredibly to less than 12 nm, approaching quantum-mechanical limitations. To address the continuous scaling issues, a joint design-technology co-optimization (DTCO) effort between process flow and design definition has been already developed, which helps to manage ramping advanced technology nodes by identifying scaling bottlenecks early and finding paths without overburdening either the design or the process points. With this methodology, Moore's Law can continue to fuel its life towards sub-3 nm nodes.

FinFETs: Most advanced transistors nowadays. Continuous miniaturization at each node provides the benefit of PPAC scaling, which aims at enhancing circuit performance by 30%, decreasing the power dissipation by 50%, reducing the chip area by 50%, and lowering the manufacturing cost by 30%. The aggressive scaling targets cannot be satisfied by planar transistors and call for significant innovations beyond 22 nm nodes. In 2011, an unprecedented 3D tri-gate transistor (FinFET) structure was brought into high-volume manufacturing and has already developed several generations (Fig. 1). The tri-gate transistor has a fin-like channel that stands up vertically. A gate wraps around 3 sides of a fin, thereby increasing gate electrostatic control over the channel. This can deliver more current drivability and lower leakage current, allowing shorter gate length and lower supply voltage in transistors.

In the logic designs, standard cells are considered where the size of standard cells is determined by contacted gate pitch (CGP) and track height. The principle is to reduce the size of standard cells with the optimization of DTCO for further scaling. The width of a standard cell depends on CGP, which still relies on lithography advancement. This is why extreme ultraviolet (EUV) lithography tools are set in for advanced nodes. One key aspect to reduce track height is fin depopulation, which is to decrease the number of fins per P- or N-type transistors. Currently, for a 6 track cell, only 2 fins are for each transistor, which was implemented at 7 nm node. Nevertheless, to keep enough current drive, increasing fin height while decreasing fin width is thus a common trend. In recent years, DTCO has focused on scaling boosters for standard cells, such as self-aligned gate contacts, buried power rails, air-gap spacers.

Nanowire or nanosheet transistors: Next leading mainstream. The era of FinFETs has transitioned from 22 nm to 5 nm nodes as the typical feature sizes further decrease to get desired PPAC targets. However, as it rigorously follows the scaling rules, FinFETs also encounter the same problems as planar transistors did. What is more, a single tall and thin fin per device is needed to reduce the track height, whereas the device with a single silicon fin may not provide sufficient current drive, novel semiconductors with high carrier mobility should thus be taken into account.

Based on the aforementioned issues, gate-all-around (GAA) nanowire or nanosheet transistors are considered promising candidates, both semiconductor academia and industry have reached a consensus to adopt this structure beyond 5 nm node[1]. The platform owns ideal gate electrostatics and to a large degree, inherits the process flow of FinFETs, which ultimately provides a better power/performance tradeoff in comparison with FinFETs techniques. One noteworthy point facing nanosheet transistors is process complexity, e.g. high-quality material growth, inner spacer formation, which may need well-developed processes to reduce the chip cost in the industry.

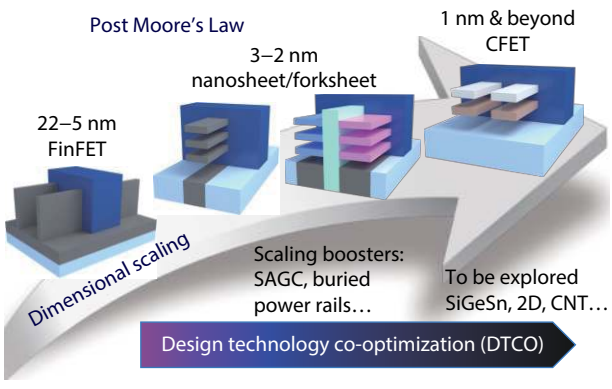

Fig. 1. (Color online) Logic transistor roadmap in the era of post Moore's Law.

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Sub-3 nm nodes with DTCO. As CGP scaling slows down, common scaling boosters based on FinFETs or GAA nanosheet transistors cannot afford enough benefits. Usually, two dummy fin spacing is typically required between N- and P-regions, which consumes up to 40%–50% of total free space in a standard cell. One strategy with DTCO is to apply a vertically stacked horizontal nanosheet architecture with a forked gate structure (forksheet), which is viewed as a natural extension of nanosheet structure[2]. By introducing a "dielectric wall", N/P regions are physically isolated with a self-aligned process, simultaneously achieving tight N/P separation. Besides, with the combination of buried power rail, the track height can be further reduced. An optimized SRAM design based on forksheet transistors contributes to enhanced standard cell area scaling and performance improvement.

Subsequently, to achieve maximum device footprint reduction potentially for 1 nm node, the complementary FET (CFET) is proposed with vertically stacked N- and P-type devices using a common gate[3]. A detailed DTCO analysis shows that the standard cell or SRAM cell can achieve 50% area reduction, moreover, similar inverter performance by 4 track CFET cell can be obtained compared to 6 track cell with 2 FinFETs through simulation. One point to be addressed in CFET is the parasitic resistance and capacitance by the compact structures, e.g. deep vias from the power rails. From a 3D scaling perspective, CFET will eventually result in a paradigm shift in the device architecture and circuit design, especially with the promotion of DTCO.

When it comes to device architecture, recently vertical GAA nanowire transistors have emerged as strong candidates to extend the CMOS roadmap since they provide further scalability, more layout efficiency, and less power dissipation in comparison to FinFETs and horizontal GAA nanowire devices[4]. Until now, group III/V and IV-based vertical nanowire transistors have been experimentally fabricated and achieved remarkable progress, which provides another CMOS scaling option.

Other than device architecture investigation, novel semiconductor materials to replace silicon have driven the industry towards alternate high-mobility channel materials. So far, state-of-the-art planar transistors and FinFETs have been manufactured based on Si and SiGe. In this regard, more investigations on SiGeSn alloys should be exploited in terms of band engineering and strain engineering. Excellent group III/V-based N-type transistors are viable whereas the P-type counterparts are still elusive to realize, primarily due to the inherent asymmetry in electron and hole mobilities in III/V materials. Besides, major issues, e.g. incompatibility with Si processing, high wafer cost, make the industrial manufacturers cautious about the III/V application into the logic platform. Additionally, low-dimensional semiconductor materials have attracted numerous attention for ultra-scaled transistors, two-dimensional layered transition metal dichalcogenides (TMDs), such as MoS_2, own atomically thin body, naturally passivated surface, and high mobilities (few tens to few hundreds $cm^2/(V{\cdot}s)$), offering promising options for high performance, low power logic applications. However, the main challenges facing 2D nanoelelectronics e.g. large-scale high-quality synthesis and contact resistance, still need to be explored. One dimensional carbon nanotube (CNT) with superior electrical properties have been also studied in the logic field, it is reported that CNT deposition with wafer-scale uniformity and reproducibility across 200 mm wafers have been achieved and a 16-bit microprocessor based on 14 000 CNT transistors was designed[5]. These attempts validate a convincing path towards beyond-silicon techniques.

To sum up, these semiconductor explorations need to consider fabrication cost metrics for the overall wafer yield, meaning they have to be wafer-scale, high-throughput, and compatible with existing silicon processing before they are put into volume production.

In the era of post-Moore's Law, simply pursuing feature size shrinking in the transistors cannot be sustainable, PPAC targets at each technology node have to be at an appropriate tradeoff. Relying on DTCO to optimize the semiconductor processing and circuit design is playing an increasingly important role in the advanced nodes. In the future, system technology co-optimization (STCO) can be even seen, that is, to consider the collaborative optimization of 3D integrated circuits (logic, memory, analog modules, etc.). Therefore, DTCO together with STCO will bring these significant innovations into sub-3 nm nodes.

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