EDITORIAL

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Preface to the Special Issue on Beyond Moore: Three-Dimensional (3D) Heterogeneous Integration

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In the past few decades, the Moore's Law has been the revolutionary force for our integrated circuit (IC) industry. However, the tremendous challenges faced in continuous transistor physical down-scaling and the unprecedented demands for computing and storage capabilities require our urgent search for strategies and solutions to integrate diverse materials, devices, circuits, and architectures in a 3D vertically stacked manner so that they can orchestrate in the most effective way to provide significantly enhanced functionalities as well as superior speed, energy, bandwidth, form fact, and cost.

To trace the recent progress and highlight the latest breakthroughs in the field of 3D heterogeneous integration, we organized a special issue on beyond Moore in *Journal of Semiconductors.* Following the first issue of resistive switching devices for emerging memory and neuromorphic computing, this issue focuses on 3D heterogeneous integration, which consists of six high-quality comprehensive review papers and four original research articles, covering the topics ranging from new materials and device architectures to integration technologies. Cheng *et al.* comprehensively review the mobility enhancement techniques using Ge and GeSn as the channel materials of FETs with a variety of interface passivation methods for enhanced performance in future high performance and low power logic applications[1]. Sun *et al.* provide a systematic review on the process challenges and its reliability issues in 3D multi-gate FETs[2]. In terms of the memory applications, Tang *et al.* propose a new idea to enhance the refresh time of quasi-non-volatile memory by engineering the density of states, demonstrating the great potential for high-speed and low-power memory technology[3]. Yang *et al.* build a non-equilibrium anomalous Hall effect model based on the analysis of the interaction between γ-ray and magnetic materials as well as the Hall device, advancing the radiation-hardened SOT-MRAM device design[4]. When it comes to silicon photonics technology, a short communication from Wu *et al.*, report the Ge-on-Si photodetector with 100 Gbit/s non-return-to-zero (NRZ) on-off-keying (OOK) and 64 Gbaud four-level pulse amplitude modulation (PAM-4) clear open eye diagrams[5]. Yang *et al.* give an exciting review on the recent progress of on-chip PCNC devices for lasing, modulation, switching/filtering, and label-free sensing, etc.[6]. Tan *et al.* propose a unified model for thermo-optic feedback tuning that can be specialized to different applications. Review on recent advances and discussion on future trends are included as well[7]. Xiang *et al.* summarize the major challenges faced in the field of photonic neuromorphic computing, propose promising solutions, and provide interesting perspectives[8]. Finally, Bao *et al.* discuss the silicon-based wafer bonding processes and the approaches to realize the monolithic integration of Si-CMOS and III–V devices on the Si wafers[9]. Li *et al.* report a comparator based on resistor-transistor logic (RTL) gates, contributing to the integration of GaN analog building blocks on p-GaN wafers for GaN ICs[10].

We hope that the readers will enjoy the present issue. We believe that it will be useful and beneficial to people working in the field of 3D heterogeneous integrated circuits, from materials and device architectures to 3D integration technologies. We also sincerely appreciate the distinguished contributions from all the authors and the tremendous assistance from the editorial and production staff of the *Journal of Semiconductors.*

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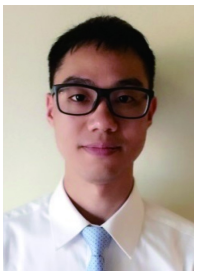

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