# Fabrication and characterization of AlGaN/GaN HEMTs with high power gain and efficiency at 8 GHz

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**Abstract:** State-of-the-art AlGaN/GaN high electron mobility structures were grown on semi-insulating 4H-SiC substrates by MOCVD and X-band microwave power high electron mobility transistors were fabricated and characterized. Hall mobility of 2291.1 cm<sup>2</sup>/(V·s) and two-dimensional electron gas density of 9.954 × 10<sup>12</sup> cm<sup>-2</sup> were achieved at 300 K. The HEMT devices with a 0.45- $\mu$ m gate length exhibited maximum drain current density as high as 1039.6 mA/mm and peak extrinsic transconduct-ance of 229.7 mS/mm. The  $f_T$  of 30.89 GHz and  $f_{max}$  of 38.71 GHz were measured on the device. Load-pull measurements were performed and analyzed under (-3.5, 28) V, (-3.5, 34) V and (-3.5, 40) V gate/drain direct current bias in class-AB, respectively. The uncooled device showed high linear power gain of 17.04 dB and high power-added efficiency of 50.56% at 8 GHz when drain biased at (-3.5, 28) V. In addition, when drain biased at (-3.5, 40) V, the device exhibited a saturation output power density up to 6.21 W/mm at 8 GHz, with a power gain of 11.94 dB and a power-added efficiency of 39.56%. Furthermore, the low  $f_{max}/f_T$  ratio and the variation of the power sweep of the device at 8 GHz with drain bias voltage were analyzed.

Key words: AlGaN/GaN heterostructure; MOCVD; HEMTs; power amplifier

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# 1. Introduction

Since the first realization of AlGaN/GaN high electron mobility transistors (HEMTs)<sup>[1]</sup>, GaN-based devices have made great progress over the past three decades. AlGaN/GaN HEMTs are promising candidates for high frequency and highpower microwave applications due to superior properties such as large band gap energy, high electron saturation velocity, high critical electric field strength, and high sheet charge densities at the interface resulting from large conduction band offset and strong polarization effects<sup>[2, 3]</sup>. Due to the absence of large-sized and high-quality GaN homogeneous substrates, foreign substrates for instance, sapphire, SiC, Si are widely used in GaN-based HEMTs<sup>[4, 5]</sup>. Among them, semi-insulating (SI) SiC remains the best choice of substrates, owing to its high thermal conductivity, high resistivity and the maturity in large-wafer mass production up to 6 inches<sup>[6, 7]</sup>.

X-band power amplifiers are used in military and commercial radar systems, as well as communication data links; indeed, these applications demand high power gain (*G*), high

Correspondence to: X L Wang, xlwang@semi.ac.cn; X G Xu, xxu@sdu.edu.cn Received 26 APRIL 2021; Revised 1 JUNE 2021. ©2021 Chinese Institute of Electronics power efficiency and suitable power specifications. GaN HEMTs have been proved to be an ideal candidate with high power densities<sup>[8–10]</sup>. In our previous work, the output power (Pout) of X-band GaN HEMT devices reached 22.4, 45.2 and 110.9 W, respectively<sup>[11–13]</sup>. Although the performance of GaN HEMTs is getting better and better, it is still not easy to fabricate GaN HEMTs operating at X-band with high power gain and high efficiency. One of the key challenges is the limitation of the material guality. Due to heteroepitaxy on semi-insulating SiC substrate, the two-dimensional electron gas (2DEG) structure materials always have large number of defects, for example, the dislocation density is in the order of 10<sup>8</sup> cm<sup>-2</sup>. The 2DEG mobility and concentration are necessary further improved to decrease the access resistances of the HEMT devices<sup>[14]</sup>. Another important issue is the trap-induced current collapse under high drain voltage bias, which severely degrades the performances of the device at high-frequency operation<sup>[15, 16]</sup>. Although the passivation layer<sup>[17]</sup> and field plates<sup>[18]</sup> were introduced to mitigate the trapping effects, the current collapse was still difficult to be eliminated.

In this paper, AlGaN/GaN HEMT structural materials with high mobility, high two-dimensional electron gas density and high uniformity were grown using a metal-organic chemical vapor deposition (MOCVD) system. HEMT devices were fabricated and their small and large signal properties were character-



Fig. 1. (Color online) The schematic of the grown AlGaN/GaN HEMT structure.

Table 1. The growth parameters of the AlGaN / GaN HEMT structure.

Order	Material	Purpose	Thickness (nm)	Temperature (°C)	
1	AIN	Nucleation layer	50	1000–1050	
2	GaN	Buffer layer with high resistivity	2000	1050	
3	GaN	High mobility channel layer	100	1050	
4	AIN	Interlayer	1	1000	
5	Al <sub>0.255</sub> Ga <sub>0.745</sub> N	Barrier layer	21.5	1000	
6	GaN	Cap layer	3	1050	

ized. HEMT devices operating at 8 GHz with high power gain and high power-added efficiency (PAE) were realized although trapping effects were not removed completely.

#### 2. HEMT structure growth and device fabrication

# 2.1. HEMT structure growth

The schematic of the AlGaN/GaN HEMT structure used in this study is shown in Fig. 1, which was grown by MOCVD on 4-inch SI 4H-SiC substrate. AlN nucleation layer, GaN buffer layer with high resistivity, GaN layer with high mobility, AlN interlayer, AlGaN barrier layer and GaN cap layer were grown in sequence. The specific growth parameters are shown in Table 1.

The introduction of the GaN channel layer with high crystal quality can enhance the mobility of 2DEG. Compared with the conventional AlGaN/GaN heterostructures, the insertion of the AlN interlayer can provide higher barrier, which improve the discontinuity of the conduction band and the confinement of the electron wave function<sup>[19]</sup>. As a consequence, the higher electron mobility can be further achieved by reducing the alloy disorder scattering from the AlGaN barrier layer, and the 2DEG sheet density is also increased<sup>[20]</sup>. As for the GaN cap layer, it provides larger effective Schottky barrier height<sup>[21]</sup>, reduces the ohmic contact resistance<sup>[22]</sup>, and alleviates the current-collapse effect<sup>[23]</sup>.

High-resolution X-ray diffraction (HRXRD, by PANalytical X'Pert<sup>3</sup> MRD) was adopted to study the crystalline quality and structural properties, while electrical properties were obtained by the room temperature (300 K) non-contact Hall measurements (by Semilab LEI 1610E 100AM). Non-contact sheet resistance measurements (by Semilab LEI 1510C) were carried out at 300 K to characterize the square resistance and their uniformity of the epi-wafers.

## 2.2. Device fabrication

The fabrication of devices begins with the formation of



Fig. 2. (Color online) The microscope photograph of the fabricated double-finger GaN HEMT with a  $L_{\rm G}$  of 0.45  $\mu$ m and total  $W_{\rm G}$  of 200  $\mu$ m. The pad is designed to be suitable for ground-signal-ground (GSG) probe.

drain and source ohmic contacts. The selected metals for ohmic contacts are composed of Ti (20 nm)/Al (120 nm)/Ni (55 nm)/Au (50 nm), deposited by electron beam evaporation, and followed by rapid thermal annealing (RTA) at 850 °C for 30 s in N<sub>2</sub> ambient. The specific ohmic contact resistance of  $1.67 \times 10^{-6} \Omega \cdot cm^2$  was measured by the transmission line method (TLM). Mesa isolation was conducted by inductively coupled plasma (ICP) dry etching. Afterwards, Si<sub>3</sub>N<sub>4</sub> was deposited by plasma enhanced chemical vapor deposition (PECVD) as the passivation layer. By reactive ion etching (RIE), a 0.45- $\mu$ m gate recess was formed, then the Schottky T-gate composed of Ni/Au was evaporated and lifted off. Finally, a silicon nitride film was deposited using PECVD to passivate the devices. The measured double-finger device has a gate length ( $L_{\rm G}$ ) of 0.45  $\mu$ m and total gate width ( $W_{\rm G}$ ) of 200  $\mu$ m, a source-to-gate distance ( $L_{SG}$ ) of 1.1  $\mu$ m, and a source-to-drain distance  $(L_{SD})$  of 4.5  $\mu$ m. A microscope photograph of the fabricated GaN HEMT is shown in Fig. 2. In order to facilitate onchip testing, the pad is designed to be suitable for a groundsignal-ground (GSG) probe.

The direct current (DC) and pulsed output *I–V* characteristics of the double-finger device were carried out using an Agilent B2902A dual-channel precision source/measure unit (SMU). The extrinsic small-signal characteristics of the devices was measured by on-wafer probing from 0.1 to 35 GHz using a SUSS |Z| probe and Agilent E8363B vector network analyzer. The Focus load-pull system were used to carried out the Al-GaN/GaN HEMT device source-pull and load-pull measurements in pulse wave (PW) mode with a pulse width of 100  $\mu$ s and a duty cycle of 1% at the frequency of 8 GHz without intentional harmonic matching. For all the measurements above, the devices were not cooled and the measurements were carried at 300 K.

#### 3. Results and discussion

Shown in Fig. 3 is the HRXRD measured results of the MOCVD-grown AlGaN/GaN HEMT structure. The full widths at half maximum (FWHM) of the (0002) and (10-12) peaks are presented in Figs. 3(a) and 3(b), with values of 266 and 324 arc seconds, respectively. Screw-type dislocation densities (STDDs) and edge-type dislocation densities (ETDDs) can be calculated using the FWHM as  $1.422 \times 10^8$  and  $8.768 \times 10^8$  cm<sup>-3</sup>, respectively<sup>[24]</sup>. These reasonable dislocation densities indicates that the epitaxial crystal materials are in good quality. Fig. 3(c) shows the HRXRD  $\omega$ –2 $\theta$  scan of the grown Al-



Fig. 3. (Color online) The HRXRD results of the AlGaN/GaN HEMT structure with (a)  $\omega$ -scan of (0002) and (b) (10-12) diffraction peaks, and (c)  $\omega$ -2 $\theta$  scan of (0004) planes.



Fig. 4. (Color online) The results of Non-contact Hall measurements at room temperature with average values of 2DEG (a) mobility and (b) concentration being 2291.1 cm<sup>2</sup>/(V·s) and  $9.954 \times 10^{12}$  cm<sup>-2</sup>, respectively.

GaN/GaN HEMT structure for the (0004) planes. The aluminum (Al) component and AlGaN thickness are fitted to be 25.5% and 21.5 nm respectively, and the measured curve is in excellent consistency with the simulated results.

The results of non-contact Hall measurements are given in Fig. 4. Mapping results in Figs. 4(a) and 4(b) show that the average value of 2DEG mobility is as high as 2291.1 cm<sup>2</sup>/(V·s) and 2DEG concentration is  $9.954 \times 10^{12}$  cm<sup>-2</sup>, respectively. Furthermore, the epi-wafer exhibited an average sheet resistance ( $R_{sh}$ ) of 301.6  $\Omega$ /square with a uniformity of 1.64%. All these measured results indicate that our MOCVD-grown Al-GaN/GaN HEMT structures are among the state-of-the-art in literature, having excellent properties and being suitable for the fabrication of high-performance devices.

Since the processed AlGaN/GaN HEMT devices were on a 330- $\mu$ m thick SI-SiC substrate without thinning, to evaluate and decrease the self-heating effect<sup>[24]</sup>, both DC and pulsed *I*-*V* (PIV) measurements were performed. During PIV mode, the quiescent bias point Q ( $V_{GSQ}$ ,  $V_{DSQ}$ ) was set at (0 V, 0 V), and each pulse cycle included an on-state pulse of 300  $\mu$ s



Fig. 5. (Color online) Typical output characteristic (a)  $I_{DS}-V_{DS}$  and transfer characteristics (b)  $I_{DS}-V_{GS}$ . In PIV mode, each pulse cycle includes an on-state pulse of 300  $\mu$ s with a duty cycle of 0.3%.

with a duty cycle of 0.3%. The typical on-wafer measured DC and PIV results are illustrated in Fig. 5 with  $I_{DS}$ - $V_{DS}$  output characteristics and  $I_{DS}-V_{GS}$  transfer characteristics of the devices. The device shows good pinch-off with a threshold voltage of  $V_{\rm th} = -5$  V. The breakdown voltage ( $V_{\rm br}$ ) over 100 V was measured. As seen from Fig. 5(a), at a gate bias of 2.0 V the maximum DC and PIV drain saturation current density (I<sub>Dmax</sub>) are 1039.60 and 1086.35 mA/mm, respectively. The knee voltage  $(V_{\rm K})$  extracted from the DC output characteristics is 4.2 V. From Fig. 5(b), peak extrinsic transconductances  $(g_m)$  are obtained to be 226.70 and 229.70 mS/mm at a gate bias of -3.0 V, respectively, for two kinds of measurements of DC and PIV. There are no obvious  $I_{DS}$  drop took place under high  $V_{DS}$  bias due to the effective heat dissipation through highly thermally conductive substrate of 4H-SiC. Except for the evident kink effect observed in DC measured output characteristics, there are little difference between the two kinds of measurement results.

The kink effect<sup>[25]</sup> is a hysteretic instability of FET drain current, which is observed during a slow drain bias sweep. The drain current shows a small step to increase a few volts above the knee region on the forward-sweep, with a little or no reduction on the return sweep. It has been observed in all generations of field-effect transistors (FETs), irrespective of the material system, whenever the substrate or surface is able to store charge and achieve a potential which diverges from ground. The observed evident kink effect in the DC characteristics imply that traps exist in the AlGaN/GaN HEMT devices. This phenomenon is related to impact ionization, hot electrons, and the presence of traps and surface states in the HEMT structure<sup>[26, 27]</sup>.

Small signal microwave performance was characterized. Measured current-gain  $H_{21}$  and maximum available powergain (MAG) as a function of frequency are shown in Fig. 6. The unit current gain cut-off frequency ( $f_T$ ) and the maximum frequency of oscillation ( $f_{max}$ ) was obtained from the extrapolation of  $H_{21}$  and MAG to unity using a –6 dB/octave slope. When the source–drain bias voltage was fixed at 15 V and the source–gate bias voltage at –3.0 V, the measured  $f_T$  and  $f_{max}$  is 30.89 and 38.71 GHz, respectively.

Physically, for a FET,  $f_{\rm T}$  is the inverse of the total transit time  $\tau^{[28]}$ ,



Fig. 6. (Color online) The extrinsic small signal characteristics of the fabricated AlGaN/GaN HEMT device.

$$f_{\rm T} = \frac{1}{2\pi\tau} = \frac{1}{2\pi \left(\frac{L_{\rm G}}{v_{\rm ch}} + \frac{L_{\rm GDd}}{2v_{\rm d}}\right)},\tag{1}$$

where  $L_{\rm G}$  is the gate length,  $v_{\rm ch}$  is the effective electron velocity in the channel,  $L_{\rm GDd}$  is the gate–drain depletion length and  $v_{\rm d}$  is the electron velocity in the depletion region. While the extrinsic small-signal characteristics of the AlGaN/GaN device was measured, the source–drain bias voltage was fixed at 15 V larger than the knee voltage 4.2 V. Due to either velocity saturation or pinch-off under the drain side of the channel,  $f_{\rm T}$  approaches its peak. The gate length of the device is 0.45  $\mu$ m. Supposing that the drain extension is zero and that the electron velocity arrives at the high field saturation velocity of  $1.5 \times 10^7$  cm/s by Monte Carlo simulation<sup>[29]</sup>, using the formula above we get intrinsic current gain cut-off frequency ( $f_{\rm TI}$ ) to be 58.26 GHz. The measured extrinsic  $f_{\rm T}$  = 30.89 GHz, smaller than the calculated  $f_{\rm TI}$  = 58.26 GHz, is due to the effects of the parasitic resistances and capacitances.

Fig. 6 shows that the  $f_{max}/f_T$  ratio is 1.253.  $f_{max}$  has the following dependence on parasitics<sup>[30]</sup>:

$$f_{\max} = \frac{f_{\rm T}}{2\left(\frac{R_{\rm G} + R_{\rm GS} + R_{\rm S}}{R_{\rm DS}} + 2\pi f_{\rm T} C_{\rm GD} R_{\rm G}\right)^{\frac{1}{2}}},$$
 (2)

where  $R_{\rm G}$  is the gate resistance,  $R_{\rm S}$  is source resistance,  $C_{\rm GD}$  is gate–drain capacitance,  $C_{\rm GS}$  is gate–source capacitance and  $R_{\rm GS}$  is the channel resistance in series with  $C_{\rm GS}$ . Generally,  $C_{\rm GD}$  is very small, which can be ignored. The low  $f_{\rm max}/f_{\rm T}$  ratio is related to the access resistance, the relatively low resistance of the semi-insulating GaN buffer, and output conductance. For our devices, because the T-gate cap is 150 nm thick much smaller than 1.0  $\mu$ m, large  $R_{\rm G}$  is one of the possible reasons responsible for the low  $f_{\rm max}/f_{\rm T}$  ratio. By shortening the gate length, gate-recessing, and reducing parasitics,  $f_{\rm T}$  and  $f_{\rm max}/f_{\rm T}$  ratio can be increased.

Large signal microwave measurements were performed on the wafer without cooling. Fig. 7 shows load-pull results of a 2 × 100 × 0.45  $\mu$ m AlGaN/GaN HEMT device measured in PW-mode with a pulse width of 100  $\mu$ s and a duty cycle of 1% by the Focus load-pull system at the frequency of 8 GHz without intentional harmonic matching. The bias was in class-AB operation, under (-3.5, 28) V, (-3.5, 34) V and (-3.5, 40) V gate/drain direct current (DC) bias, respectively. The de-



Fig. 7. (Color online) The power performances of the fabricated Al-GaN/GaN HEMT device. The measurement was performed under PW-mode with a pulse width of 100  $\mu$ s and a duty cycle of 1%. The bias was in class-AB operation, under (a) (-3.5, 28) V, (b) (-3.5, 34) V and (c) (-3.5, 40) V gate/drain direct current (DC) bias, respectively.

tailed measurement results are shown in Table 2.

Fig. 7(a) shows the power sweep at a drain bias of 28 V with a linear gain of 17.04 dB. A maximum  $P_{out}$  of 30.54 dBm achieved at  $P_{in} = 19.54$  dBm with an associated power gain of 11.00 dB and PAE of 50.56%, the gain compression being 6 dB. The saturated output power density is 5.66 W/mm.

Fig. 7(b) gives the power sweep at a drain bias of 34 V with a linear gain of 18.22 dB. A maximum  $P_{out}$  of 30.61 dBm achieved at  $P_{in} = 18.52$  dBm with an associated power gain of 12.09 dB and PAE of 46.67%, the gain compression being 6 dB. The saturated output power density is 5.75 W/mm.

Fig. 7(c) indicates the power sweep at a drain bias of 40 V with a linear gain of 18.19 dB. A maximum  $P_{out}$  of 30.94 dBm achieved at  $P_{in} = 19.00$  dBm with an associated power gain of 11.94 dB and PAE of 39.56%, the gain compression being 6 dB. The saturated output power density is 6.21 W/mm.

In Fig. 8, the obtained  $P_{outr}$  power gain, PAE and drain efficiency, are depicted as a function of  $V_{DS}$ , during the measurement, the  $P_{in}$  was fixed to 18 dBm, and the  $V_{GS}$  was fixed in –3.5 V. The output power and power gain increase with increasing  $V_{DS}$ , from 30.15 to 30.71 dBm, and 12.15 to 12.70 dB, respectively. The PAE and drain efficiency decrease with increasing  $V_{DS}$  from 50.43% to 39.94%, and 54.35% to 42.21%, respectively.

For an ideal HEMT in class-AB operation, the DC and the corresponding fundamental current components of the output current waveform can be calculated by Fourier analysis according to<sup>[31]</sup> yielding:

$$I_{\rm DC} = \frac{I_{\rm Dmax}}{2\pi} \cdot \frac{2\sin(a/2) - a\cos(a/2)}{1 - \cos(a/2)},$$
 (3)

$$l_1 = \frac{l_{\text{Dmax}}}{2\pi} \cdot \frac{\alpha - \sin\alpha}{1 - \cos(\alpha/2)},\tag{4}$$

where *a* is the conduction angle.

The maximum output power can be calculated according to the following formula:

$$P_{\rm out} = \frac{1}{8} \left( \Delta I \cdot \Delta V \right), \tag{5}$$

where  $\Delta I = 2I_1$  and  $\Delta V = 2(V_{DS} - V_K)$  are the RF current swing

and voltage swing. This predicts a possible output power density provided that an ultimate thermal management is properly done. For the devices fabricated by us, the  $V_{\rm K}$  extracted from the DC output characteristics is 4.2 V, and the  $I_{\rm Dmax}$  was obtained to be 1039.60 mA/mm at a gate bias of 2.0 V. The conduction angle was calculated to be 105.83°. From the formulas above it is easy to know the possible output power and maximum drain efficiency ( $\eta_{\rm D}$ ) corresponding to different  $V_{\rm DS}$  from 28 to 40 V. The calculated results are given in Table 3, showing that with increasing the  $V_{\rm DS}$ , both the DC power supply and the output fundamental power as well as the maximum  $\eta_{\rm D}$  will increase.

The  $\eta_{\rm D}$  almost keeps constant at about 62.8% with a slightly increase when  $V_{DS}$  increases from 28 to 40 V. If the  $V_{\rm K}$  = 0 V, the calculated maximum  $\eta_{\rm D}$  will be 71.87% being constant for all  $V_{DS}$ . The calculated maximum output power is 6.53, 8.17 and 9.82 W/mm, respectively, when V<sub>DS</sub> are 28, 34 and 40 V. However, our measured output power at the corresponding V<sub>DS</sub> are 5.66, 5.71 and 6.21 W/mm, respectively, as shown in Fig. 7 and Table 2. It is evident that the higher the  $V_{DS}$ , the more difference between the ideal maximum output power and the measured output power at a power gain compression of 6 dB. The most evident is that the measured maximum  $\eta_{\rm D}$  is much lower than the calculated counterpart and they decrease faster and faster with increasing the  $V_{DS}$ , implying that the decrease of the measured  $\eta_{\rm D}$  is correlated to the increase of the  $V_{DS}$ , which therefore make the output power at  $V_{\rm DS} = 40$  V nearly the same as that of  $V_{\rm DS} = 28$  V.

The above calculation is based on an important condition that both the RF current swing  $\Delta I$  and the  $V_{\rm K}$  are constants while changing the  $V_{\rm DS}$ . When this condition is not satisfied, the change of the ideal maximum output power density with  $V_{\rm DS}$  will not be linear.

One of the main limiting factors to high performance in GaN HEMTs is the current collapse or DC-to-RF dispersion caused by trapping effects<sup>[15, 16]</sup>. The effects of current collapse can be assessed with PIV measurements. To explore why increase in output power is lower than the expected when the  $V_{DS}$  increased from 28 to 40 V, the device performance under different quiescent bias were investigated using the PIV measurement method. Each test pulse period consists of a 1  $\mu$ s on-state pulse, followed by a 999  $\mu$ s off-state pulse (0.1% duty cycle) at the quiescent bias point Q ( $V_{GSQ}$ ,  $V_{DSQ}$ ). Here, three quiescent points are adopted, as shown in Fig. 9. (a)  $Q_0$ : negligible electron trapping with ( $V_{GSQ0}$ ,  $V_{DSQ0}$ ) = (0 V, 0 V); (b)  $Q_1$ : gate stress with ( $V_{GSQ1}$ ,  $V_{DSQ1}$ ) = (-8 V, 0 V); (c)  $Q_2$ : gate and drain stress with ( $V_{GSQ2}$ ,  $V_{DSQ2}$ ) = (-8 V, 12 V). The measured PIV results are shown in Fig. 9. The on-resistance  $R_{\rm on}$  under different Q has been extracted, and the  $V_{\rm K}$  is estimated with reference<sup>[32]</sup>. At the quiescent bias point of Q<sub>2</sub>, the current collapse degradation is about 5.9%.

Fig. 9 shows there exist trapping effects in our devices and gives an idea of the amount of trapping in the structure. The  $R_{on}$  increase is obvious in large  $V_{DS}$  stress and inconspicuous in large  $V_{GS}$  bias, and the output current  $I_{DS}$  also decrease under the influence of stress. As a result, large  $V_{DS}$  stress leads to an increase in  $V_K$  and decrease in  $I_{DS}$ . Moreover, with further increase of  $V_{DS}$  stress, the current collapse will become more serious<sup>[15, 16]</sup>. According to Eq. (5), the increase of  $V_K$  and the decrease of  $I_{DS}$  will lead to the degradation of power characteristics of the device under large  $V_{DS}$  bias.

Table 2. The detailed measurement results of power performances of the fabricated AlGaN/GaN HEMT device.

DC bias ( $V_{GS}$ , $V_{DS}$ ) (V)	P <sub>out</sub> (max) (dBm)	P <sub>in</sub> (dBm)	<i>G</i> (dB)	PAE (%)	G (compression) (dB)	G (linear) (dB)	P <sub>out</sub> density (saturated) (W/mm)
(-3.5, 28)	30.54	19.54	11.00	50.56	6	17.04	5.66
(-3.5, 34)	30.61	18.52	12.09	46.67	6	18.22	5.75
(-3.5, 40)	30.94	19.00	11.94	39.56	6	18.19	6.21



Fig. 8. (Color online) The obtained  $P_{out}$ , PAE and power gain, depicted as a function of  $V_{DS}$ . During the measurement, the  $P_{in}$  was fixed in 18 dBm, and the  $V_{cS}$  was fixed in -3.5 V.

Table 3. The calculated possible output power and drain efficiency corresponding to different  $V_{DS}$  from 28 to 40 V when  $V_{GS} = -3.5$  V.

DC bias (V <sub>GS</sub> , V <sub>DS</sub> ) (V)	V <sub>DS</sub> - V <sub>K</sub> (V)	P <sub>DC</sub> (W/mm)	$P_{\rm RF}$ (W/mm) ( $V_{\rm K}$ = 4.2 V)	η <sub>D</sub> (%)
(-3.5, 28)	23.80	10.68	6.53	61.09
(-3.5, 34)	29.80	12.97	8.17	62.99
(-3.5, 40)	35.80	15.26	9.82	64.32



Fig. 9. (Color online) Pulsed current-voltage characteristics of the device. Measurements are taken under different quiescent bias point ( $V_{GSQ}$ ,  $V_{DSQ}$ ), as indicated in the graph. Each test pulse period consists of a 1  $\mu$ s on-state pulse, followed by a 999  $\mu$ s off-state pulse (0.1% duty cycle). Here  $V_{GS}$  is taken from -6.0 to 2.0 V in steps of 1.0 V.

The power and efficiency performance of an AlGaN/GaN HEMT is mainly limited due to the following factors: (a) Knee voltage  $V_{\rm K}$ ; (b) Drain leakage current  $I_{\rm min}$ ; (c) Current collapse or DC-to-RF dispersion  $\Delta I_{\rm DC-RF}$ ; (d) Feedback; (e) Compression behavior; (f) Thermal effects and reliability. Taking all these factors from (a) to (e) into consideration, the realizable power-added efficiency amounts can be estimated by<sup>[33]</sup>:

$$PAE = \eta_{\rm D} \cdot \frac{1}{1 + V_{\rm K}/V_{\rm DC}} \cdot \frac{1}{1 + I_{\rm min}/I_{\rm DC}} \cdot \frac{1}{1 + \Delta I_{\rm DC-RF}/I_{\rm DC}} \times \left(1 - \omega^2 C_{\rm GD}^2 + R_{\rm GD} R_{\rm L}\right) \left(1 - \frac{1}{G}\right),$$
(6)

PAE is mainly determined by the  $V_{\rm K}$  and  $\Delta I_{\rm DC-RF}/I_{\rm DC}$ . The  $V_{\rm K}$ has a deep impact on the PAE behavior of a transistor due to the fact that it will always be a significant percentage of the DC supply<sup>[31]</sup>. The RF  $V_{\rm K}$  increases with increasing  $V_{\rm DS}^{[34]}$ . The current collapse at high V<sub>DS</sub> also lead to reduced load-pull measurement results of output power and PAE<sup>[35]</sup>. Therefore, we believe that for our devices the decrease of the maximum PAE with increasing the  $V_{DS}$  is mainly caused by trapping effects and that the output power at  $V_{DS} = 40$  V is nearly the same as that of  $V_{DS} = 28$  V is because the DC-to-RF dispersion is more severe at high V<sub>DS</sub>. Although the DC-to-RF dispersion still exists in our devices, by using the state-of-the-art HEMT structural materials, surface passivation technology and field plate, HEMTs with high gain and high efficiency were achieved. The origin of the related traps in the devices will be further investigated in detail.

## 4. Conclusion

We have grown state-of-the-art AlGaN/GaN HEMT structure materials on 4-inch SI 4H-SiC substrates and fabricated X-band HEMT microwave power devices of 0.45-µm gate length with high linear power gain of 17.04 dB and high power-added-efficiency of 50.56% at 8 GHz when drain biased at 28 V in class-AB operation. The 2DEG mobility and concentration of the HEMT structure were measured to be 2291.1 cm<sup>2</sup>/(V·s) and  $9.954 \times 10^{12}$  cm<sup>-2</sup>, respectively. A low average  $R_{\rm sh}$  of 301.6  $\Omega$ /square with uniformity of 1.64% is achieved. For the fabricated HEMT devices, DC and PIV drain saturation current density are 1039.60 and 1086.35 mA/mm, and the peak extrinsic transconductances are obtained to be 226.70 and 229.70 mS/mm at a gate bias of -3.0 V, respectively. The  $f_{T}$  and  $f_{max}$  of the device were measured to be 30.89 and 38.71 GHz, respectively. Large  $R_{\rm G}$  is one of the possible reasons responsible for the low  $f_{max}/f_T$  ratio of 1.253. When device drain was biased at 28, 34 and 40 V and gate at -3.5 V in class-AB, our measured output power density of the device without cooling is 5.66, 5.71 and 6.21 W/mm, with power gains and PAEs of 11.00 dB and 50.56%, 12.09 dB and 46.67%, and 11.94 dB and 39.56%, respectively. The measured output power densities are lower than the ideally expected maximum output power of 6.53, 8.17 and 9.82 W/mm at corresponding drain–source biases, due to the effects of possibly existing traps in the HEMTs on RF knee voltage and maximum output current with increasing drain–source bias. Although the DC-to-RF dispersion still exists in our devices, by using the state-of-the-art HEMT structural materials, surface passivation technology and field plate, HEMTs with high gain and high efficiency were achieved.

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#### 8 Journal of Semiconductors doi: 10.1088/1674-4926/42/12/122802



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