

High-performance junction field-effect transistor based on black phosphorus/ β -Ga₂O₃ heterostructure

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Abstract: Black phosphorous (BP), an excellent two-dimensional (2D) monoelemental layered p-type semiconductor material with high carrier mobility and thickness-dependent tunable direct bandgap structure, has been widely applied in various devices. As the essential building blocks for modern electronic and optoelectronic devices, high quality PN junctions based on semiconductors have attracted widespread attention. Herein, we report a junction field-effect transistor (JFET) by integrating narrow-gap p-type BP and ultra-wide gap n-type β -Ga₂O₃ nanoflakes for the first time. BP and β -Ga₂O₃ form a vertical van der Waals (vdW) heterostructure by mechanically exfoliated method. The BP/ β -Ga₂O₃ vdW heterostructure exhibits remarkable PN diode rectifying characteristics with a high rectifying ratio about 10^7 and a low reverse current around pA. More interestingly, by using the BP as the gate and β -Ga₂O₃ as the channel, the BP/ β -Ga₂O₃ JFET devices demonstrate excellent n-channel JFET characteristics with the on/off ratio as high as 10^7 , gate leakage current around as low as pA, maximum transconductance (g_m) up to 25.3 μ S and saturation drain current (I_{DSS}) of 16.5 μ A/ μ m. Moreover, it has a pinch-off voltage of -20 V and a minimum sub-threshold swing of 260 mV/dec. These excellent n-channel JFET characteristics will expand the application of BP in future nano-electronic devices.

Key words: two-dimensional semiconductor; black phosphorous; β -gallium oxide; vdWs heterostructure; junction field-effect transistor

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1. Introduction

As an emerging material with an ultra-wide bandgap (4.9 eV) at room temperature, high theoretical critical field strength (8 MV/cm), superior power switching capability and large Baliga's figure of merit, β -gallium oxide (β -Ga₂O₃) has been considered a competitive material for the next generation of high power electronic and optoelectronic devices. The unintentionally doped β -Ga₂O₃ exhibits inherent n-type conductivity because the oxygen vacancy acts as a donor^[1–5]. Until now, the epitaxially grown β -Ga₂O₃ thin films and single-crystalline β -Ga₂O₃ wafers were successfully obtained for fabricating various metal–oxide–semiconductor field-effect transistors (MOSFETs)^[4–7]. Nevertheless, the performances of MOSFETs are severely influenced by oxide dielectrics. Charge

transport will be suppressed due to the poor-quality dielectric surface^[8]. Alternatively, as an important part of field-effect transistors (FETs), junction field-effect transistors (JFETs) have a simple device structure without dielectric layers. The working mechanism of JFETs is controlling the depletion region in the semiconducting channel with a reverse biased PN junction^[9]. In detail, it is controlling the source–drain current (I_{ds}) by the gate–source voltage (V_{gs}). For n-channel JFET, the conductive channel became narrow with V_{gs} decreased, resulting in the channel resistance increasing and the I_{ds} decreasing. When V_{gs} up to pinch-off voltage, the channel will be fully depleted, resulting in the JFET being switched off. Unlike MOSFETs, β -Ga₂O₃ is rarely applied to JFETs due to the difficulty of effective hole doping for n-type β -Ga₂O₃^[10].

Recently, Barman *et al.* proved the single-crystalline β -Ga₂O₃ can be exfoliated into nanoflakes along the (100) plane direction while maintaining the superior properties of bulk crystals, even though it's not a layered 2D material bound together through the van der Waals (vdW) force^[11]. As a quasi-

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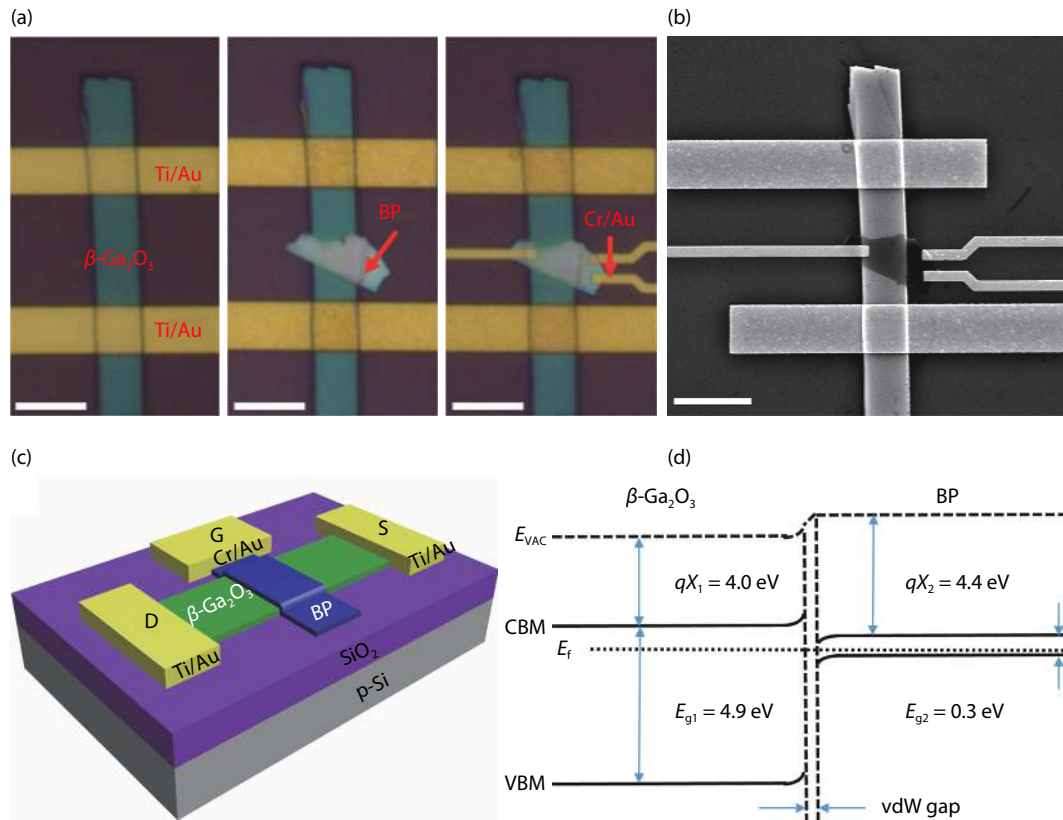


Fig. 1. (Color online) (a) Optical microscope images of fabrication steps of BP/ β -Ga₂O₃ heterojunction device. The channel length and width of the β -Ga₂O₃ were 16 and 6 μm , respectively. (b) SEM image of an as-fabricated BP/ β -Ga₂O₃ heterojunction device. (c) Schematic illustration of the JFET device fabricated on a Si/SiO₂ (285 nm) substrate. (d) Energy band diagram of multilayer p-type BP and n-type β -Ga₂O₃ heterojunctions with a vdW gap. Scale bars are 10 μm .

2D material, exfoliated β -Ga₂O₃ flakes had formed vdW heterojunctions by integrating with various 2D materials without lattice matching^[12]. For example, β -Ga₂O₃/graphene vertical vdW heterostructure with a high breakdown electric field^[13], double graphene-gate β -Ga₂O₃ metal-semiconductor FETs (MESFETs) for a logic inverter^[14], β -Ga₂O₃/hexagonal boron nitride (h-BN) metal-insulator-semiconductor FET (MISFETs) with superior performances^[15], etc. And more notably, Kim *et al.* reported that a typical JFET structure with a low-dimensional heterojunction PN diode. It was formed between mechanically exfoliated p-type WSe₂ and n-type β -Ga₂O₃^[8]. This approach provides one way to fabricate JFETs based on β -Ga₂O₃ and achieve a high on/off ratio. However, due to the limitation of intrinsic properties of WSe₂, the integral performances of JFET based on β -Ga₂O₃/2D materials still need to improve.

As a novel 2D layered semiconductor material, black phosphorous (BP) is gradually receiving considerable attention, because it possesses a tunable direct bandgap (0.3 to 1.5 eV) by thickness (bulk to monolayer), high carrier mobility over 1000 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, strong light-matter coupling, excellent intrinsic in-plane anisotropy and exciting biocompatibility^[16–23]. Therefore, BP demonstrated remarkable performance in versatile applications, such as broadband photo-detection^[24–26], solar cells^[27–30], biomedicine^[31–34], logic circuit^[35–38], catalysts^[39, 40]. Moreover, BP shows the p-type intrinsic conduction although most 2D semiconductors are n-type because of inherent structural defects and strong electron doping from interfacial charge impurities^[41]. Actually, the p-type materials are essential for forming PN heterojunc-

tions which apply to electronic and optoelectronic devices. A variety of PN heterojunctions were produced between BP and other n-type materials, such as ZnO^[37], MoS₂^[42], InSe^[43].

In this work, we demonstrate a vdW heterojunction JFET based on BP and β -Ga₂O₃. The mechanically exfoliated multilayer BP flakes as the gate and multilayer β -Ga₂O₃ flakes as the channel. The BP/ β -Ga₂O₃ PN junction exhibits preeminent rectification characteristics with rectifying ratio higher than 10⁷ and the reverse current as low as pA. The BP/ β -Ga₂O₃ JFETs show excellent n-channel JFET characteristics with high on/off ratio about $\sim 10^7$, low gate leakage current around pA, high g_m of 25.3 μS and I_{DSS} of 16.5 $\mu\text{A}/\mu\text{m}$. Moreover, it has a pinch-off voltage of -20 V and a minimum subthreshold swing of 260 mV/dec. Additionally, the electrical performances of the BP/ β -Ga₂O₃ JFET device at different temperatures are also discussed. This work not only expands the applications of BP in future nanoelectronic devices but also paves the way for vdW heterojunctions based on 2D semiconductors applying to realize high performance JFET devices.

2. Experiments

Material Characterizations: All nanoflakes were measured for thickness information and surface morphology through an atomic force microscope (AFM, Bruker Dimension ICON). Raman measurements were conducted in a micro-Raman system (LABRAM HR) with visible laser light ($\lambda = 532 \text{ nm}$). The morphology and elemental mapping of the heterojunction were observed by scanning electron microscope (SEM, Quanta FEG 250).

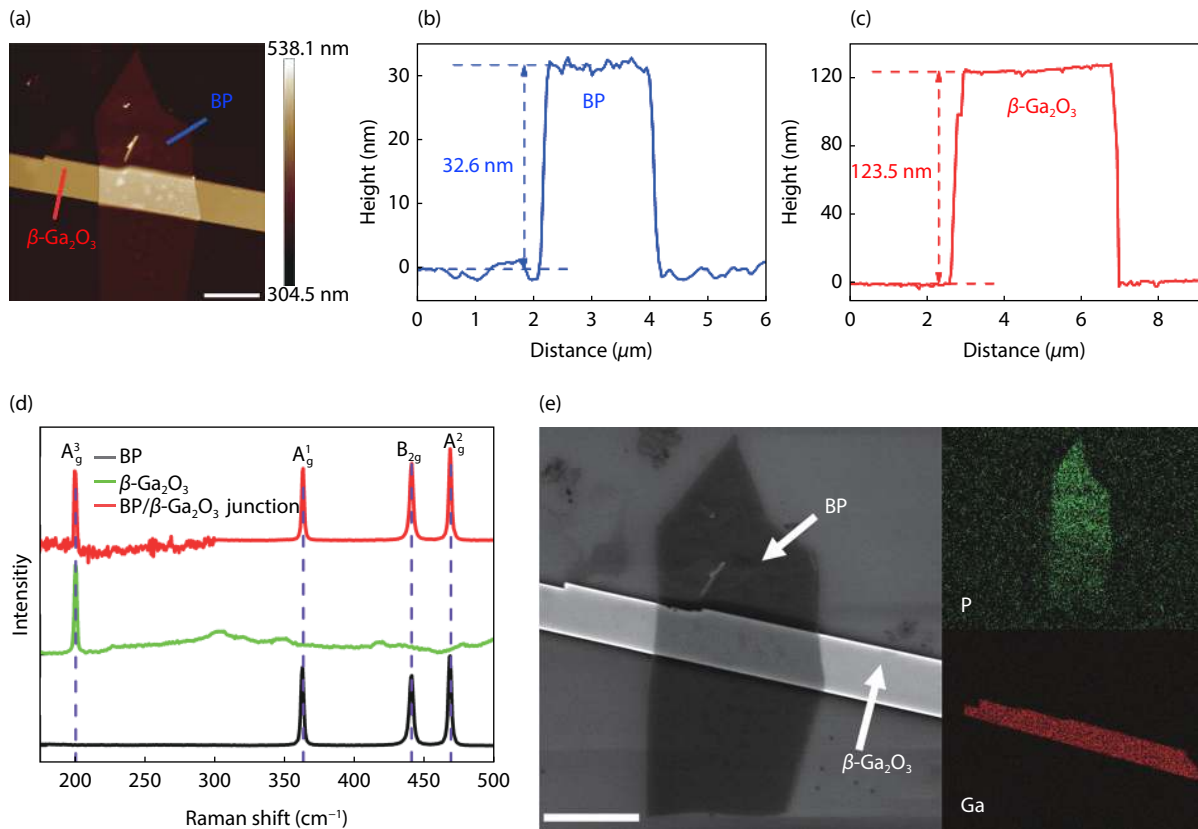


Fig. 2. (Color online) (a) AFM image of the BP/ β -Ga₂O₃ heterojunction. (b, c) Height profiles of the exfoliated BP and β -Ga₂O₃ flakes in (a). The thicknesses of the nanoflakes are 32.6 and 123.5 nm, respectively. (d) Raman spectra of the BP, β -Ga₂O₃ and the BP/ β -Ga₂O₃ overlapped regions obtained under a 532 nm laser. The black and green curve demonstrated typical multilayer BP flake and β -Ga₂O₃ flake. The red curve shows the peaks of the overlapped region. (e) SEM image of the BP/ β -Ga₂O₃ heterostructure device (left) and corresponding EDS element mappings for Ga and P (right). Scale bars are 5 μ m.

Device Fabrication: Using traditional dry transfer technology, the BP/ β -Ga₂O₃ heterojunction was fabricated inside a glove box. First, β -Ga₂O₃ flakes were prepared from a bulk single-crystalline (100) β -Ga₂O₃ through the conventional mechanical exfoliation method and transferred onto Si/SiO₂ (285 nm) substrates. In order to remove the organic impurity, the substrates with β -Ga₂O₃ flakes were soaked into acetone for several hours before the device fabrication. Then, the source-drain electrodes of Ti/Au (30/120 nm) were fabricated using electron-beam lithography (JEOL JBX 5500) to define patterns, electron beam evaporator (ULVAC Ei-5Z) to deposit metal films and lift-off process. In order to achieve ohmic contact, rapid thermal annealing was carried out for 60 s at 475 °C in a nitrogen ambient. Afterwards, using the same way, few-layer BP flakes were separated from bulk BP crystals synthesized by mineralizer-assisted gas-phase transformation method. The exfoliated BP flakes were precisely transferred onto β -Ga₂O₃ through a picking-up and dropping process using the polydimethylsiloxane (PDMS) transfer technique. Finally, the contact metallization with BP was performed by depositing Cr/Au (10/70 nm) using the same method mentioned above. To avoid oxidation from O₂ and H₂O, the exposure time in ambient was limited within one hour during the fabrication process.

Electrical Characterizations: The electrical characteristics of the fabricated JFET were measured by a Sussmicrotec probe station with a Keithley 4200 semiconductor parameter analyzer.

3. Results and discussion

Fig. 1(a) shows the fabrication process of the BP/ β -Ga₂O₃ heterojunction JFET device by using optical microscope images. Multilayer β -Ga₂O₃ flakes are prepared via mechanically exfoliation. BP/ β -Ga₂O₃ heterojunctions are fabricated by the vdW force using an alignment dry transfer method (for more details, see Experiments). The quality of the as-fabricated BP/ β -Ga₂O₃ heterojunction can be obtained from the SEM image (Fig. 1(b)). The surfaces of both BP and β -Ga₂O₃ materials were smooth and the heterojunction interface was clean. Fig. 1(c) shows schematic illustration of the BP/ β -Ga₂O₃ heterojunction device on the Si/SiO₂ substrate. In this heterojunction device, the source-drain voltages (V_{ds}) is applied on β -Ga₂O₃, BP and Si/SiO₂ act as the gate and back gate, respectively. As shown in Fig. 1(d), the energy band diagram of BP/ β -Ga₂O₃ heterojunction demonstrates the formation of a typical PN junction. According to the previous reports, the electron affinity (χ) and bandgap (E_g) values of multilayer β -Ga₂O₃ are about 4.0 and 4.9 eV, respectively^[6–8]. For multilayer BP, the electron affinity (χ) and bandgap (E_g) values are about 4.4 and 0.3 eV, respectively^[16–19]. The Fermi energy (E_f) of β -Ga₂O₃ almost close to conduction band minimum (CBM) but the E_f of BP close to valence band maximum (VBM), because multilayer β -Ga₂O₃ and multilayer BP are unintentional n-type and p-type doped, respectively. The heterojunction band diagram is extremely important to understand the operation mechanism of the heterojunction JFET device.

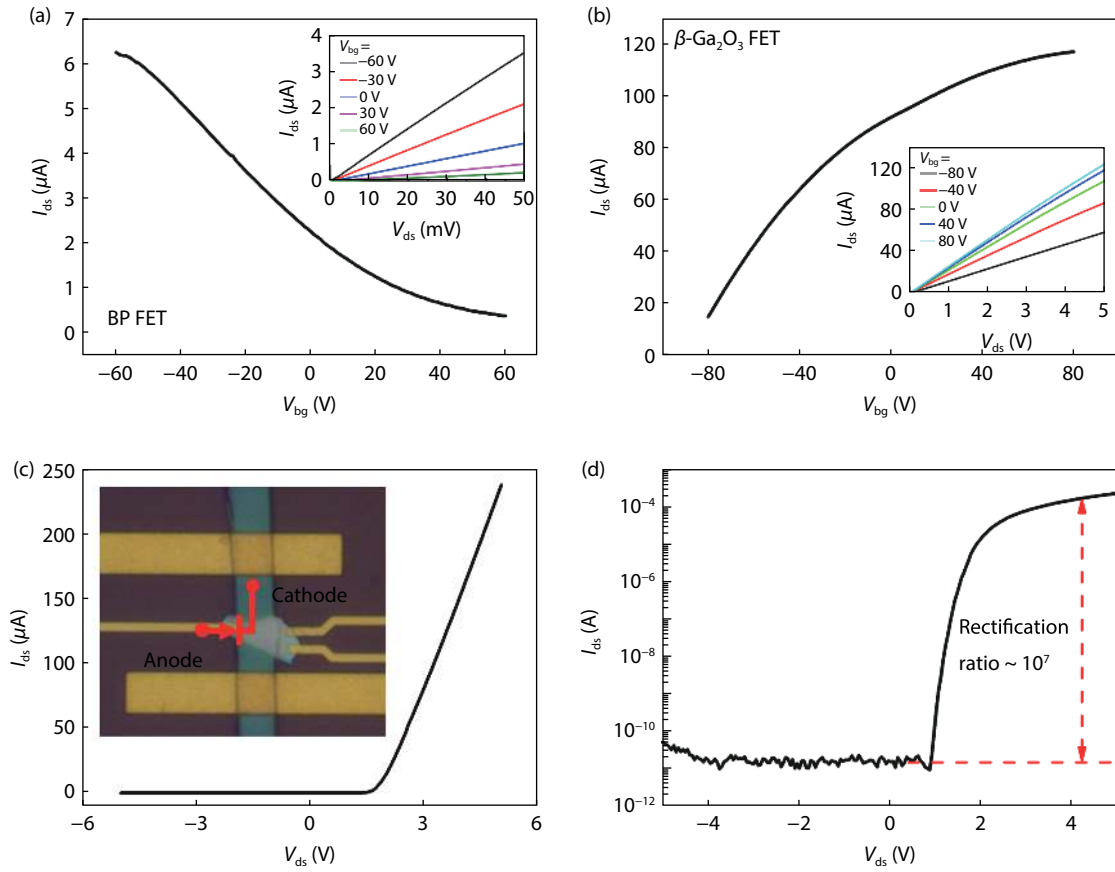


Fig. 3. (Color online) (a) Transfer characteristics for back-gate BP FET. Back gate voltage V_{bg} swept from -60 to 60 V with a fixed source-drain bias voltage $V_{ds} = 0.1$ V. (Inset: output characteristics for back gated BP FET. V_{bg} ranging from -60 to 60 V with steps of 30 V under V_{ds} swept from 0 to 50 mV.) (b) Transfer characteristics for back gate β -Ga₂O₃ FET. V_{bg} swept from -80 to 80 V with a fixed $V_{ds} = 5$ V. (Inset: output characteristics for back-gate β -Ga₂O₃ FET. V_{bg} ranging from -80 to 80 V with steps of 40 V under V_{ds} swept from 0 to 5 V.) (c) I_{ds} - V_{ds} curve of BP/ β -Ga₂O₃ PN heterojunction. It shows a typical rectifying behavior. (Inset: the circuit schematic diagram of the PN heterojunction.) (d) I_{ds} - V_{ds} semi-log plot of the BP/ β -Ga₂O₃ PN heterojunction.

In order to obtain the thickness and surface morphology of the BP/ β -Ga₂O₃ heterojunction, the AFM image and height profiles are presented in Figs. 2(a)–2(c). The thickness of BP is about 32.6 nm with β -Ga₂O₃ flakes of 123.5 nm. Moreover, AFM image indicates that a vertical heterojunction can be fabricated by directly covering the multilayer BP on the β -Ga₂O₃ flake. Fig. 2(d) shows the Raman spectrum of BP, β -Ga₂O₃ and the BP/ β -Ga₂O₃ heterojunction (overlapped region) on the Si/SiO₂ substrate. Three characteristic peaks of BP located at 362, 440, and 467 cm⁻¹, corresponding to A_g¹, B_{2g}, and A_g² vibration modes, respectively^[17]. The peak about 200 cm⁻¹ corresponds to the A_g³ vibration mode of the β -Ga₂O₃^[2]. The observed peaks are consistent with previously reported data. The peaks of both BP and β -Ga₂O₃ can be observed in the overlapped region without significant changes comparing to non-overlapped regions. These results confirm the good quality of the flakes in the heterostructure and neither materials have obvious destruction after exfoliation and device fabrication. Fig. 2(e) shows the SEM image (left) of BP/ β -Ga₂O₃ heterojunction, which reveals the material surfaces are smooth. Element mappings (right) indicate that Ga atoms and P atoms are evenly distributed in the heterostructure device.

To demonstrate the fabricated BP/ β -Ga₂O₃ PN heterojunction is available, the electrical properties of the as-fabricated BP/ β -Ga₂O₃ heterojunction FETs as well as the individual BP

and β -Ga₂O₃ devices are exhibited in Fig. 3. Fig. 3(a) shows the source-drain current I_{ds} as a function of back gate voltage (V_{bg}) at a fixed source-drain bias voltage ($V_{ds} = 0.1$ V) for the BP FET. Meanwhile, the I_{ds} - V_{ds} curves under different V_{bg} (ranging from -60 to 60 V with steps of 30 V) are presented in the inset of Fig. 3(a). The device shows a typical p-type ambipolar transistor, which is consistent with previous reports^[16]. Similarly, Fig. 3(b) shows I_{ds} - V_{bg} curve at a fixed $V_{ds} = 5$ V for the β -Ga₂O₃ FET, the I_{ds} - V_{ds} curves under different V_{bg} (ranging from -80 to 80 V with steps of 40 V) are presented in the inset of Fig. 3(b). The device exhibits an obvious n-type semiconducting transistor behavior. According to the linear I_{ds} - V_{ds} curves shown in the inset of Figs. 3(a) and 3(b), there is a good ohmic contact between the materials and the electrodes. The circuit schematic diagram of the PN heterojunction is shown in the inset of Fig. 3(c). As shown in Figs. 3(c) and 3(d), the I_{ds} - V_{ds} curve and semi-log plot for the BP/ β -Ga₂O₃ heterojunction exhibit a clear rectifying behavior with a rectification ratio about 10^7 , reverse current around pA and threshold voltage near 1.0 V. The rectification ratio is defined as the ratio of the forward/reverse current, which is usually used to check the degree of rectification^[41]. These strong rectifying behaviors reveal that there is a good van der Waals PN heterojunction formed between p-type BP and n-type β -Ga₂O₃.

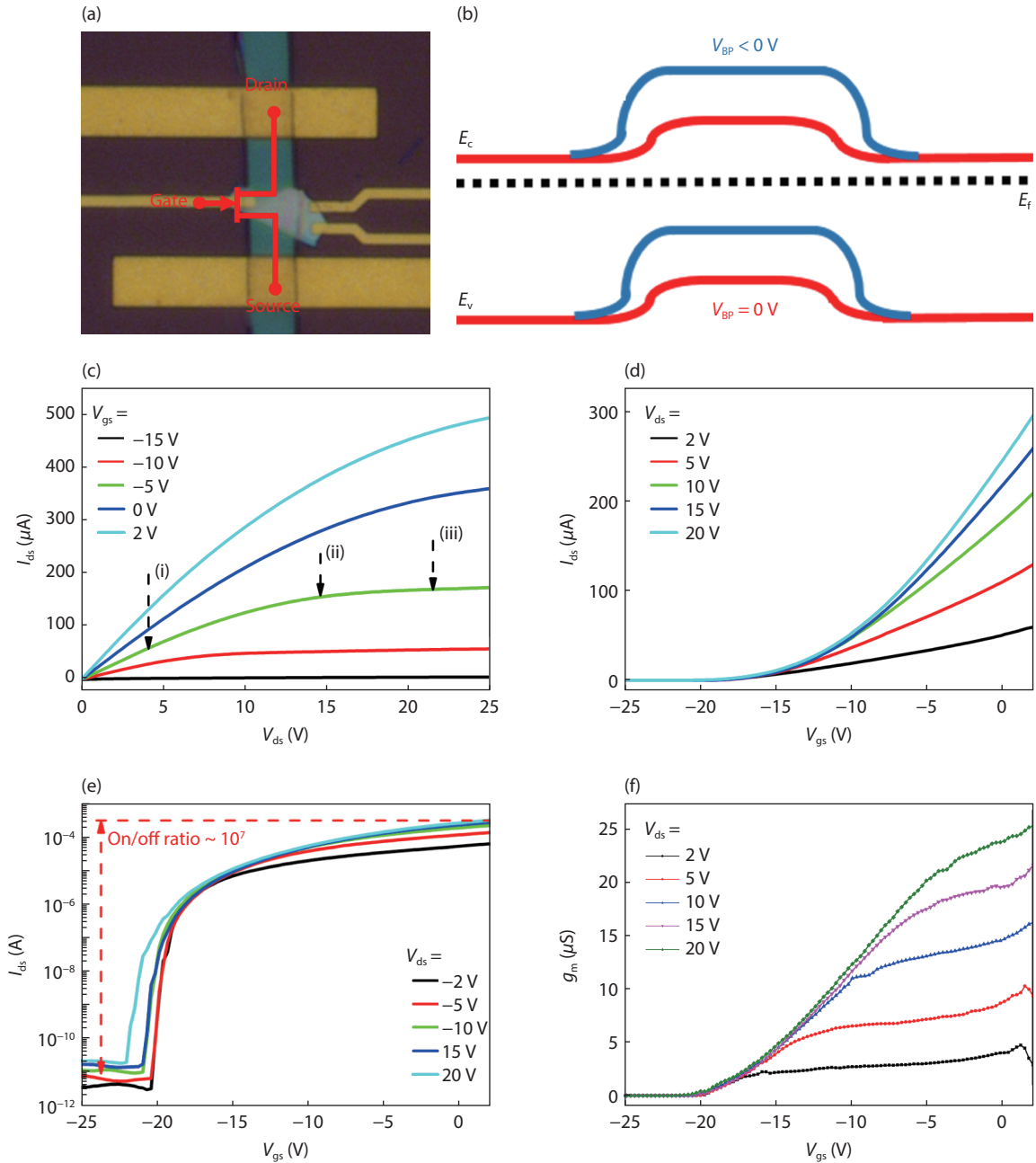


Fig. 4. (Color online) (a) Circuit schematic diagram and optical image of the BP/β-Ga₂O₃ JFET. (b) Band diagram of β-Ga₂O₃ along the channel length direction. The red and blue curve shows the band bending at zero and negative gate voltage, respectively. (c) Output characteristics (I_{ds} – V_{ds}) of the JFET. V_{gs} ranging from –15 to 2 V under V_{ds} swept from 0 to 25 V. (d) Transfer characteristics (I_{ds} – V_{gs}) of the JFET. V_{ds} ranging from 2 to 20 V under V_{gs} swept from –25 to 2 V. (e) Semi-log plot of the transfer characteristics of the JFET. It shows a high on/off ratio beyond 10⁷. (f) Transconductance curves (estimated from transfer curves of (d)) of BP/β-Ga₂O₃ JFET as function of V_{gs} with V_{ds} sweeping from 2 to 20 V.

To further investigate the properties of the BP/β-Ga₂O₃ PN heterojunction, BP/β-Ga₂O₃ JFET devices were fabricated. The circuit schematic diagram and optical image of the BP/β-Ga₂O₃ JFET are shown in the Fig. 4(a). Using the p-type BP as the gate and n-type β-Ga₂O₃ as the channel, a PN heterojunction formed at the BP/β-Ga₂O₃ vdW interface. According to the operational mechanism of JFETs, the diode characteristics within the gate-channel PN junction are crucial in determining the final JFET characteristics^[9]. Fig. 4(b) shows the band diagram of β-Ga₂O₃ along the channel length direction at different V_{gs} . When $V_{gs} = 0$ V, the energy band of β-Ga₂O₃ is expected to shift upwards slightly (red lines) due to Fermi level alignment. If a negative voltage is applied on BP ($V_{gs} < 0$ V), the β-

Ga₂O₃ energy band will go further upward (blue lines) and the channel will be fully depleted. Therefore, the JFET switched on or off can be modulated effectively by gate voltage on BP. Output characteristics (I_{ds} – V_{ds}) of the JFET with different V_{gs} (ranging from –15 to 2 V) are shown in Fig. 4(c) and obvious I_{ds} saturation are observed. According to a previous report^[38], the output curves were divided into three stages for typical JFET characteristics: (i) linear, (ii) pinch-off, and (iii) saturation. When V_{ds} was small, I_{ds} – V_{ds} curves displayed a linear function. As V_{ds} increased further, the channel reached to pinch-off state with a knee V_{ds} about 15 V. At last, I_{ds} appeared as a saturation phenomenon (also called constant current) where I_{ds} remained constant as V_{ds}

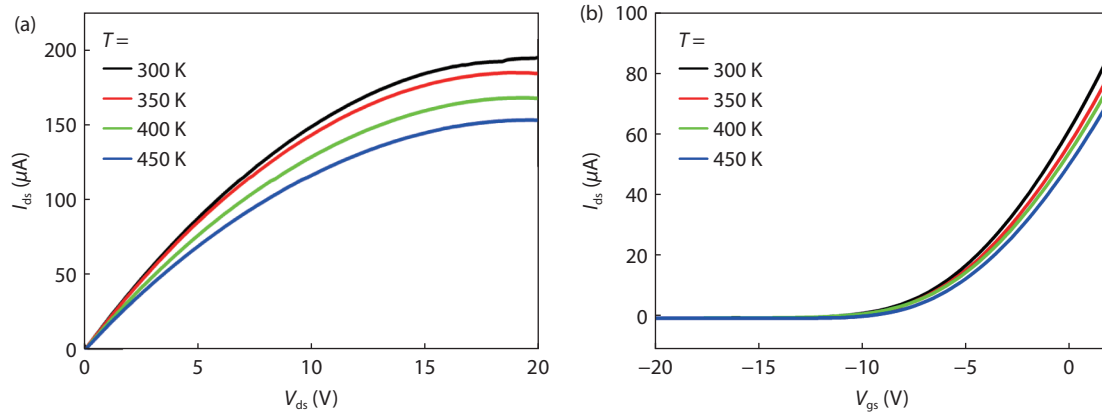


Fig. 5. (Color online) (a) Output characteristics curves of the BP/ β -Ga₂O₃ JFET under different temperatures (ranging from 300 to 450 K with steps of 50 K) at $V_{gs} = 1$ V. (b) Transfer characteristics curves of the BP/ β -Ga₂O₃ JFET under different temperatures (ranging from 300 to 450 K with steps of 50 K) at $V_{ds} = 10$ V.

continuously increased. Figs. 4(d) and 4(e) show the typical transfer characteristics (I_{ds} – V_{gs}) and semi-log plot of the JFET at various V_{ds} (ranging from 2 to 20 V). When a negative voltage was applied on BP, the depletion region of the gate-channel PN junction widened and the channel of β -Ga₂O₃ became synchronously narrower, resulting in the channel resistance increased and the I_{ds} decreased. The threshold voltage was about -20 V. Thus the source-drain current was switched on (demonstrating n-type transport) when $V_{gs} > -20$ V and switched off when $V_{gs} < -20$ V, corresponding to effectively switched on/off of the JFET. The ON/OFF ratio is beyond 10^7 indicating high heterojunction interface quality with low trap density. Fig. 4(f) shows the transconductance plots at various V_{ds} extracting from Fig. 4(d). The maximum transconductance (g_m) is of $25.3 \mu\text{S}$. The field-effect mobility is one of the most important parameters for both MOSFET and JFET, which can be directly estimated from transfer characteristics. The g_m can be calculated by the following equation^[9]:

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{qN_d\mu tW}{L},$$

where N_d is the unintentional doping carrier density; μ is the field-effect mobility; q is an electronic charge; and L , t , and W are the length, thickness and width of the channel, respectively. So, the field-effect mobility μ can be calculated as follows,

$$\mu = \frac{Lg_m}{qN_d tW}.$$

The maximum field-effect mobility μ_{\max} of the BP/ β -Ga₂O₃ JFET is $14.7 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ when g_m is $25.3 \mu\text{S}$. The subthreshold swing (SS) is another important parameter for describing the performance of transistors. To achieve lower power consumption and higher integration, it is essential to minimize the SS. The theoretical limit of JFET SS value is 60 mV/dec due to the lack of complicated dielectric engineering. To investigate the performance of BP/ β -Ga₂O₃ JFET in the subthreshold regime, the minimum SS of 260 mV/dec is reached when $V_{ds} = 20$ V and $V_{gs} = -21$ V. Reducing the thickness and effective carrier concentration of β -Ga₂O₃ nanosheets will be available for further improving the SS of BP/ β -Ga₂O₃ JFET devices.

To understand the working regimes of the BP/ β -Ga₂O₃ JFET device at different temperatures, temperature-depend-

ent electrical characteristics tests were carried out. The typical output and transfer characteristics at various temperatures (ranging from 300 to 450 K with steps of 50 K) are presented in Figs. 5(a) and 5(b), respectively. Obviously, the JFET characteristics were well maintained. According to the output characteristics curves of the BP/ β -Ga₂O₃ JFET device under various temperatures (Fig. 5(a)), obvious I_{ds} saturation and three stages for typical JFET characteristics (linear, pinch-off and saturation) are observed. While, the I_{ds} decreased with the increasing temperature probably because of lower carrier mobility and enhanced phonon scattering. As shown in Fig. 5(b), transfer characteristics curves of the BP/ β -Ga₂O₃ JFET device under different temperatures demonstrate typical JFET characteristics that V_{gs} control I_{ds} . The pinch-off voltage is about -18 V, I_{ds} is switched off when $V_{gs} < -18$ V and switched on when $V_{gs} > -18$ V, corresponding to effectively switched off/on of the JFET.

4. Conclusion

Herein, we have successfully fabricated vdW heterojunction JFET devices based on multilayer p-type BP as the gate and n-type β -Ga₂O₃ flakes as the channel by mechanically exfoliated methods. The BP/ β -Ga₂O₃ heterojunctions possess clean interfaces. Furthermore, the BP/ β -Ga₂O₃ PN junction devices show clear rectification characteristics of a high rectifying ratio about 10^7 and low reverse current around pA. These strongly rectifying behaviors demonstrate that a good van der Waals PN heterojunction formed between p-type BP and n-type β -Ga₂O₃. More importantly, the fabricated JFET devices show excellent n-channel JFET properties such as high I_{ds} on/off ratio of 10^7 , low gate leakage current around pA, high g_m of $25.3 \mu\text{S}$ and I_{DSS} of $16.5 \mu\text{A}/\mu\text{m}$. In addition, the devices have a pinch-off voltage of -20 V and a minimum subthreshold swing of 260 mV/dec. The temperature-dependent electrical characteristics of JFET devices are also discussed. The JFET characteristics are well maintained although the I_{ds} decreased with the increasing temperature. This work paves the way for vdW heterojunctions based on 2D semiconductors whose application will realize high-performance JFET devices.

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