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Charge transport and quantum confinement in MoS_2 dual-gated transistors

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Abstract: Semiconductive two dimensional (2D) materials have attracted significant research attention due to their rich band structures and promising potential for next-generation electrical devices. In this work, we investigate the MoS_2 field-effect transistors (FETs) with a dual-gated (DG) architecture, which consists of symmetrical thickness for back gate (BG) and top gate (TG) dielectric. The thickness-dependent charge transport in our DG-MoS_2 device is revealed by a four-terminal electrical measurement which excludes the contact influence, and the TCAD simulation is also applied to explain the experimental data. Our results indicate that the impact of quantum confinement effect plays an important role in the charge transport in the MoS_2 channel, as it confines charge carriers in the center of the channel, which reduces the scattering and boosts the mobility compared to the single gating case. Furthermore, temperature-dependent transfer curves reveal that multi-layer MoS_2 DG-FET is in the phonon-limited transport regime, while single layer MoS_2 shows typical Coulomb impurity limited regime.

Key words: MoS_2; field effect transistors; dual-gate; quantum confinement; Coulomb impurity

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1. Introduction

Atomic thick two-dimensional (2D) layered materials, such as semi-metallic graphene and semiconductive transition metal dichalcogenides (TMDCs), have emerged as an attractive candidate for future electronic and optoelectrical materials[1–6]. Among them, molybdenum disulphide (MoS_2) is a typical member of TMDCs and considered as a promising candidate for various device applications, mainly due to its prolific, thickness-dependent band structures[7–10]. The single-gated field-effect transistors (SG-FETs) based on MoS_2 exhibit excellent carrier mobility (~ 200 $cm^2/(V{\cdot}s)$), high current on/off ratio (> 10^8), and low subthreshold swing approaching the fundamental thermal limit at room temperature[2]. The short channel effects (SCE) can also be suppressed due to the ultra-thin channel body[7, 11].

Since the bandgap size is dependent on the MoS_2 layer number[12–14], bilayer (BL) or multilayer (ML) MoS_2 tend to achieve higher mobility to carry larger driving current than that of monolayer MoS_2. However, the BL or ML-MoS_2 suffer from the degradation of SS and the current on/off ratio due to weaker channel electrostatic control. To overcome such a problem, the dual-gated (DG) structure, similar to that of Fin-FET technology, provides better electrostatic control over the channel region and is more achievable for 2D-TMDCs[15–18]. Liu *et al*. achieved a back-gate mobility of up to 517 $cm^2/(V{\cdot}s)$ and an on/off ratio higher than 10^8 based on SiO_2, Al_2O_3 as the back-gated and top-gated dielectric[19]. Our previously reported results based on a DG-FET with symmetrical back and top gates also indicate that the DG structure is able to modulate the threshold voltage (V_{TH}) and SS by tuning back and top gates separately, and a superior channel current (I_D) modulation can be achieved under the DG gating[20–22]. Nevertheless, the charge transport and current distribution influenced by DG structure have not been systematically discussed in TMDCs devices.

Here, we successfully fabricate the MoS_2 DG-FETs with symmetric back gate (BG) and top gate (TG) based on monolayer and multilayer MoS_2 films. The thickness-dependent charge transport in our MoS_2 DG structure is revealed by a four-probe electrical measurement which excludes the contact influence, and TCAD simulation shows that the impact of quantum confinement effect exists in thin MoS_2 sheet sandwiched by the DG. Such effect attenuates with larger thickness, but still exist in a 5-nm-thick channel. The temperature-

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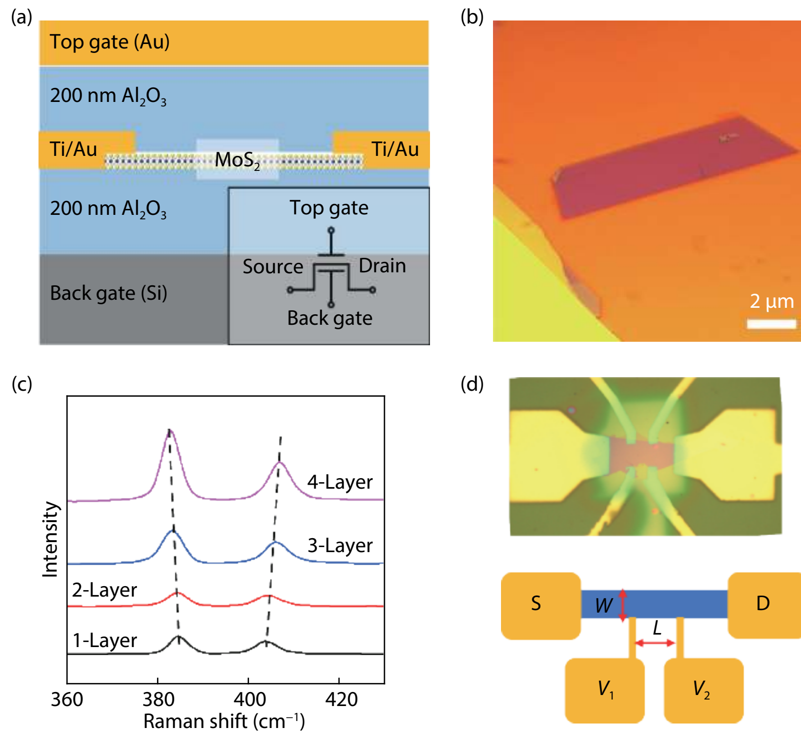

Fig. 1. (Color online) (a) Side-view schematic illustration of a MoS_2 DG-FET. (b) Optical microscopic image of an exfoliated MoS_2 sheet on a 200-nm-thick Al_2O_3 substrate. (c) Raman spectra of MoS_2 sheets with thickness ranging from 1L to 4L. (d) Optical image of a typical 4-terminal device, the top gate electrode is relatively thin (15 nm) but still conductive. The lower graph is a schematic of the 4-terminal device in which W is the channel width and L is the distance between two inner pads. V_1 and V_2 are used to gauge the voltage drop between two inner contacts.

dependent electrical measurement of our device also indicates that transport of multilayer MoS_2 DG-FET is in the phonon-limited transport regime, while single layer MoS_2 device shows typical Coulomb impurity (CI) limited regime.

2. Device structure and material characterization

The cross-sectional schematic of MoS_2 DG-FET is depicted in Fig. 1(a). The fabrication process for such devices starts from the deposition of a 200-nm-thick Al_2O_3 layer by atom layer deposition (ALD, MNT-100-4) on a heavily doped Si substrate, which acts as a BG dielectric layer. Then multilayer MoS_2 flakes are mechanically exfoliated on top of Al_2O_3, and a typical optical microscopic image is shown in Fig. 1(b). Uniform and rectangular shaped MoS_2 sheets are selected for subsequent device fabrication. Raman characterization (laser excitation wavelength of 514 nm) is then carried out to confirm the layer number and crystalline quality, as shown in Fig. 1(c). To avoid lithography contamination, electrical contacts (5 nm Ti/30 nm Au) are patterned using a stencil mask technique[23]. Immediately after the contact deposition, another layer of 200-nm-thick Al_2O_3 is deposited by ALD as TG dielectric, followed by the formation of TG electrodes by traditional photo-lithography, metal evaporation, and lift-off. Electrical transport measurements are performed under an ambient condition with a semiconductor analyzer (Agilent, B1500a). Temperature-dependent measurement was carried out in a cryogenic vacuum probe-station.

The field-effect mobility μ is a crucial factor to characterize the FET performance. For most TMDCs-based FETs, the effective value of μ is mainly governed by the contact rather than the channel itself[24, 25]. In order to isolate the intrinsic mobility, we compensate for this effect by utilizing a four-terminal structure to exclude the contact effect. The upper graph of Fig. 1(d) is an optical image of our four-terminal device and the lower graph is a schematic diagram where the two inner voltage probes V_1 and V_2 are used to gauge the voltage drop. Then the four-terminal conductivity $\sigma_{4prob} = \frac{I_D}{V_1 - V_2}\frac{L}{W}$, where I_D is the channel current and L and W are the length and width of the MoS_2 channel inside the inner voltage probes, respectively.

3. Experimental result and discussion

The measured σ_{4prob} as functions of BG, TG and DG modes are shown in Fig. 2(a). It is noted that results from BG and TG modes are highly coincident due to their symmetric gating capability, while a weak mismatch at negative gate voltage region can also be observed, which may result from their different dielectric-MoS_2 interfaces. As for the BG, MoS_2 is directly transferred on to the pre-deposited Al_2O_3, while for the TG, the interface quality degrades because of the absence of dangling bonds on MoS_2 for deposition of Al_2O_3.

It also shows that DG mode displays an improved channel electrostatic control than that of BG or TG. To further illustrate the gate modulation by BG and TG, a 2D contour plot of σ_{4prob} as functions of V_{BG} and V_{TG} is then plotted in Fig. 2(b). Such 2D diagram shows parallel diagonal contours with constant current, and the slope of these contours line is approximately 1, indicating that the BG and TG exhibit the same capability to modulate the channel, since the oxidation layer capacitance of the back gate and top gate is nearly symmetrical ($C_{BG}/C_{TG} \approx 1$).

For SG structure, the field-effect (FE) mobility can be estim-

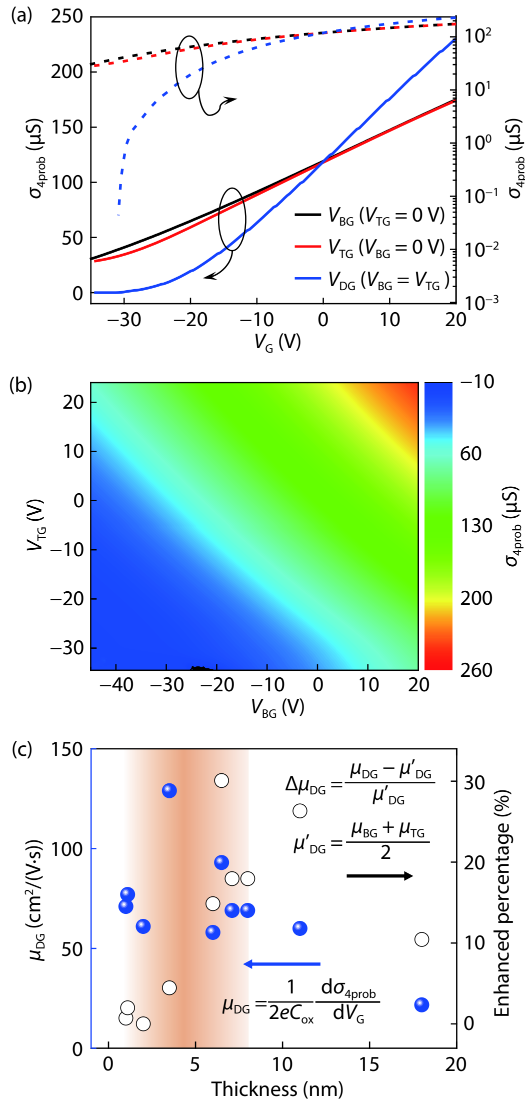

Fig. 2. (Color online) (a) Four-terminal conductivity σ_{4prob} as functions of BG, TG and DG voltages. Solid and dashed curves correspond to linear and logarithmic coordinates, respectively. (b) 2D contour plot of σ_{4prob} as functions of V_{BG} and V_{TG} at room temperature. (c) Mobility versus sheet thickness collected from 10 MoS_2 DG-FETs work under DG mode.

ated by $\mu = \frac{1}{eC_{ox}}\frac{d\sigma}{dV_G}$, where C_{ox} is the gate capacitance per unit area (40 nF/cm^2 for 200 nm of Al_2O_3), V_G is the gate voltage, and e is the elementary charge. While in the case of a symmetric DG structure and considering top and bottom surfaces of MoS_2 as parallel channels, we can estimate that the total conductivity $\sigma'_{DG} = \sigma_{BG} + \sigma_{TG}$. Since $C'_{ox\text{-}DG} \approx 2C_{ox}$, we expect that the quantity $\mu'_{DG} = (\mu_{BG} + \mu_{TG})/2$ will be equal to μ_{DG} estimated by the σ_{DG}–V_{DG} curve. However, it appears that directly measured μ_{DG} is generally larger than μ'_{DG}, which indicates the inadequacy of this parallel channel model. We then use $\Delta\mu_{DG} = (\mu_{DG} - \mu'_{DG})/\mu'_{DG}$ to quantify the mobility enhancement of dual gating, and plot in Fig. 2(c) $\Delta\mu_{DG}$ and μ_{DG} as functions of the channel thickness. It is noted that both device mobility and $\Delta\mu_{DG}$ reach a maximum with the MoS_2 thickness in the range of 2–6 nm, and such thickness-dependent μ_{DG} deviates from previously reported results with only BG[24, 26, 27], indicating a different carrier transport mechanism in our DG-FETs.

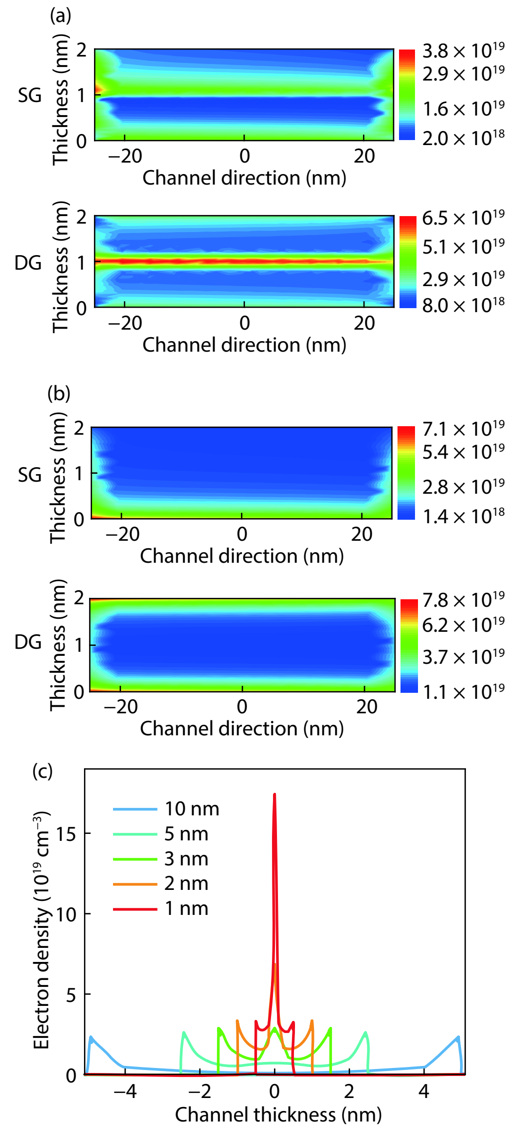

Fig. 3. (Color online) (a) With and (b) without considering quantum confinement effect, the simulation results of carrier redistribution of a 2-nm-thick MoS_2. The upper and lower panels show the simulation results from the SG (V_{BG} = 10 V) and DG (V_{BG} = V_{TG} = 10 V) device, respectively. (c) The electron density in the channel of the DG MoS_2 device versus channel thickness. The dielectric layer is 200 nm Al_2O_3 for all devices

Depending on the channel thickness, there is a competition of multiple mechanisms in our MoS_2 DG-FETs: 1) larger current carrying ability in thicker channels, but with considerable interlayer resistance[24]; 2) current redistribution due to the DG induced quantum confinement effect; 3) electrical transport exposed to extrinsic Coulomb scattering from high-k dielectrics (e.g. Al_2O_3, HfO_2) and interface for ultra-thin channels. Therefore, the experimental results exhibit their overall competitional effects. While the first and the third factors may have a negative effect on the mobility, we now focus on the quantum confinement effect, which may avoid the interfacial scattering and enhance the carrier mobility.

To ravel the impact from quantum confinement effect, the carrier density, and distribution of the DG-FETs are then simulated by using the van Dort model, the 1D Schrödinger equation, the density gradient model, and the modified local-density approximation (MLDA). The van Dort model com-

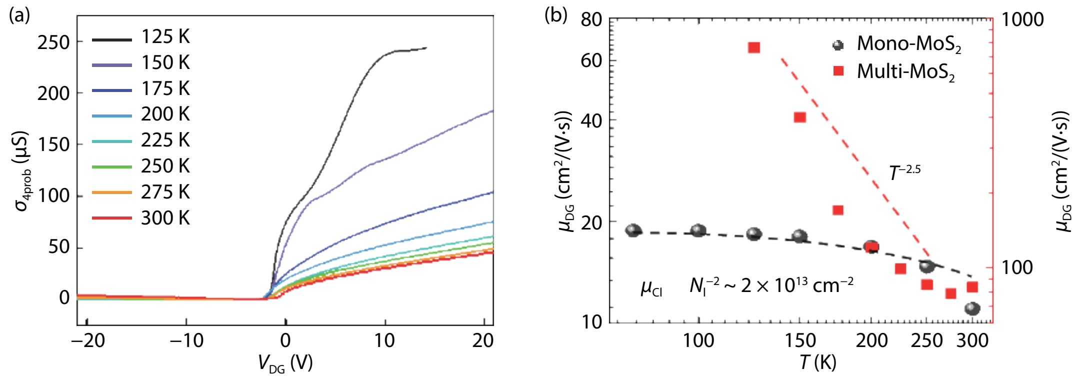

Fig. 4. (Color online) Temperature dependence electrical measurement. (a) The temperature-dependent σ as a function of V_{DG} of a four-probe device. MoS_2 is ~5 nm thick with 200 nm Al_2O_3 of both TG and BG dielectrics. (b) The temperature-dependent mobility extracted from monolayer MoS_2 (black dot) and multi-layer MoS_2 DG-FET (red square). Monolayer MoS_2 DG-FET is 15 nm HfO_2 of both TG and BG dielectrics.

putes the impact of electric field normal to the channel interface on the carrier density modification due to the quantization. Based on the energy band structures in the channel, the 1D Schrödinger equation was solved self-consistently with the Poisson equation. The eigenvalues and wave functions for electrons and holes were obtained with consideration of multi valleys in conduction and valence bands. The density gradient model added the quantum correction to the carrier distribution at interfaces in the device by introducing the reciprocal thermal energy, mass-driving term, and the smoothed potential[28]. In this model, the bandgap narrowing effect and apparent band-edge shifts caused by multistate configurations were involved. The MLDA model calculates the distribution of confined carriers near the dielectric/channel interface. In our simulation, the multi valley properties of conduction and valence bands were considered in MLDA model.

Figs. 3(a) and 3(b) compare the quantum-confinement impact on the simulated carrier redistribution in SG (V_{BG} = 10 V) and DG (V_{BG} = V_{TG} = 10 V) structures. In the DG structure, quantum confinement effect is rather prominent, it repulses carriers away from dielectric-MoS_2 interfaces and confines carriers inside the channel, which can suppress phonon and Coulomb scattering at interfaces and contribute to the mobility improvement. On the opposite, the carriers in the SG structure are pushed towards one side of MoS_2, amplifying the interface scattering. Fig. 3(c) shows the calculated carrier distribution in MoS_2 DG device with a series of channel thicknesses, by considering quantum confinement effect. It is noticed that the impact of quantum confinement effect attenuates with larger thickness but still exist in a 5 nm thick channel.

Thus, a complete scenario for thickness dependence of MoS_2 DG-FET can be: thicker MoS_2 carries current larger but with less quantum confinement effect, and there are also trade-offs including large interlayer resistance and screening effect than weakens the gate control. For practical applications of MoS_2 FETs, considering critical parameters including μ, SS and current on/off ratio, a layer thickness in the range of 2–6 nm would be ideal by achieving overall satisfying μ, SS and current on/off ratio[21], which is competitive comparing to best SOI[29].

We then investigate the temperature-dependent electrical properties of our MoS_2 DG-FETs. Fig. 4(a) shows the temperature-dependent transfer curve from a multilayer MoS_2 device (~ 5 nm). The channel current increases when temperature decreases, while the threshold voltage V_{TH} hardly shifts when lowering the temperature. In the 4-terminal device architecture, mobility extraction is more accurate, as shown in Fig. 4(b). The mobility in a multi-layer MoS_2 DG-FET is as high as 763 cm^2/(V·s) ($n \approx 10^{13}$ cm^{-2}) at 125 K (plotted by red point) and can be fitted by $T^{-\gamma}$ for T > 100 K with γ = 2.5, which is in good agreement with theoretically predicted value (γ between 1.52 and 2.6)[30, 31]. This indicates that our multilayer MoS_2 DG-FET is in the phonon-limited transport regime. While the temperature-dependent mobility of a monolayer MoS_2 device (grey points) shows typical CI limited regime, especially at low temperature. The CI limited mobility (μ_{CI}) can be well fitted by our calculation (plotted by gray dash) considering screening effect by surrounding dielectrics[32, 33] (15-nm-thick HfO_2 for this device) with $n \approx 10^{13}$ cm^{-2} and impurity density $N_I \approx 2 \times 10^{13}$ cm^{-2}. Such difference can also originate from the quantum confinement effect but a more detailed investigation is necessary to achieve an in-depth understanding in the future.

4. Conclusion

We reported a systematic investigation of carrier transport in MoS_2 DG-FETs with a variation of MoS_2 channel thickness. DG structure provides better electrostatic control for the MoS_2 FETs. Moreover, quantum confinement plays an important role in the charge transport, as for a certain thickness of MoS_2, confinement of the charge in the center of the channel under DG mode reduces the scattering and thus boosts the mobility compared to single gating of a similar thickness layer. The TCAD simulation considering quantum confinement reveals that the impact of quantum confinement effect attenuates with larger thickness but still exist in a 5 nm thick channel. Furthermore, the phonon-limited transport regime and CI limited regime were revealed in multi-layer MoS_2 DG-FETs and single layer MoS_2 by temperature-dependent transfer curves, respectively. Such device architecture together with similar results can be extended to other TMDCs based devices.

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