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Metal–insulator transition in few-layered GaTe transistors

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Abstract: Two-dimensional (2D) materials have triggered enormous interest thanks to their interesting properties and potential applications, ranging from nanoelectronics to energy catalysis and biomedicals. In addition to other widely investigated 2D materials, GaTe, a layered material with a direct band gap of ~1.7 eV, is of importance for applications such as optoelectronics. However, detailed information on the transport properties of GaTe is yet to be explored, especially at low temperatures. Here, we report on electrical transport measurements on few-layered GaTe field effect transistors (FETs) encapsulated by h-BN at different temperatures. We find that by tuning the carrier density, ambipolar transport was realized in GaTe devices, and an electrical-field-induced metal to insulator transition (MIT) was observed when it was hole doped. The mobilities of GaTe devices show a clear dependence on temperature and increase with the decrease of temperature, reaching ~1200 $cm^2V^{-1}s^{-1}$ at 3 K. Our findings may inspire further electronic studies in devices based on GaTe.

Key words: metal-insulator transition; gate tunable; GaTe; field effect transistors

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1. Introduction

Since the discovery of graphene[1, 2], two-dimensional (2D) semiconductors, including transition metal dichalcogenides (TMDCs)[1, 3], black phosphorous (BP)[4] and 2D ferromagnetic semiconductors[5], have provoked tremendous attention benefiting from their intrinsic physical properties and unique electronic structures[6], especially the versatality to construct van der Waals heterostructures. It has thus triggered new physical phenomena, such as the valley Hall effect[7], electrical control of magnetism[5, 8, 9], metal–insulator transition (MIT)[10–18], Mott-insulator and superconductivity in twisted bilayer graphene with magic angle[19].

Recently, telluride gallium (GaTe) has attracted increasing attentions. As a 2D layered semiconductor with a direct band gap, GaTe shows excellent photoelectric properties[20–22], the phototransistors fabricated from GaTe exhibit high photoresponsibility of 10^4 A/W, which is far beyond that of most other 2D layered materials. Flexible GaTe photodetectors have also been obtained with a high photoresponse and an excellent linear input–output relationship[23]. In addition, low lattice symmetry of structure endows GaTe unique anisotropic properties that can be utilized to fabricate anisotropic devices with gate-tunable giant anisotropic resistance[24, 25]. However, detailed measurements on the transport properties of GaTe are still missing. More investigations are needed to gain a better comprehension of GaTe, as well as to fabricate functional devices based on it.

In this work, we report measurements on the transport properties of GaTe at different temperatures. It is known that GaTe is easily oxidized in air. Therefore, to attenuate damages from the air environment, h-BN was employed to fully encapsulate GaTe by the dry transfer method performed in a glove box. The results show that by tuning the carrier density, the GaTe devices exhibit ambipolar transport property, which persists down to low temperatures. As temperature decreases, our devices display a remarkable increase in the field-effect mobilities on the hole side: from ~40 $cm^2V^{-1}s^{-1}$ at 300 K to ~1200 $cm^2V^{-1}s^{-1}$ at 3 K, respectively. Moreover, for gate voltage approaching −100 V, all devices studied show a metallic behavior over the entire T-range. These studies provide us with a measure to understand the transport properties of thin flakes of GaTe, which may enable the design of future electronic and optoelectronic devices based on it.

2. Method

2.1. Crystal growth and characterization

Bulk crystals were grown via self-flux method[26]. Ingredient powders with high purity (99.99%) were mixed with stoichiometric ratio of Ga : Te = 1 : 1, the mixture was kept at 880 °C for 3 h and then was cooled to 700 °C at a rate of 1.5 °C per minute followed by a natural cooling process. The bulk crystal formed at the bottom of crucible after cooling. XRD results indicate that the self-flux process yields high quality GaTe crystals.

2.2. Exfoliation of GaTe and fabrication of few-layered GaTe transistors

Thin flakes of GaTe were obtained through a mechanical exfoliation method. Bottom h-BN was directly exfoliated onto the substrate. Selected GaTe flakes and top h-BN were stacked in sequence by dry transfer procedure[27]. All of the exfoliation and transfer process were finished in a glove box to avoid any degradation caused by oxygen or water. Atomic

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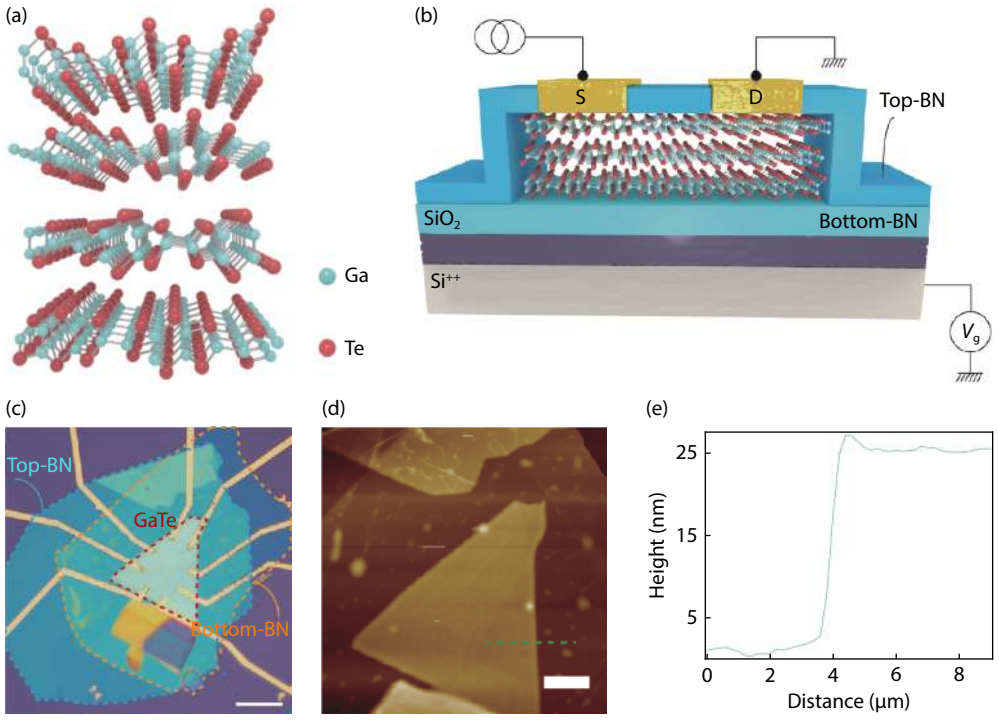

Fig. 1. (Color online) Characterizations of GaTe and a typical BN/GaTe/BN device. (a) Schematic of GaTe layered lattice, with the interlayer spacing of ~0.8 nm. (b) Schematic illustration of the device. (c) Optical micrograph of the device, the scale bar is 10 μm. (d) AFM morphology image of the device with a height profile plotted in (e), plotted along the green dashed line in (d).

force microscope was used to confirm the height and surface roughness of the samples which were transferred onto Si substrates coated with 300 nm SiO_2 layers. Reactive ion etching was performed to etch the top h-BN making the GaTe flake partially exposed as patterned for electrode contact. Devices with Cr/Au (5 nm/35 nm) electrodes were fabricated via standard electron beam lithography (EBL) and electron beam evaporation procedures, and then annealed in Ar : H_2 (10 : 1) atmosphere at 320 °C for 30 min.

2.3. Measurements on electrical transport

Electrical measurements were performed by micro-probe station and physical properties measurement system (PPMS) with Keithley 2400 source meters and digital lock-in amplifiers Stanford Research Systems SR830.

3. Results and discussion

As a layered material, the in-plane interaction of GaTe is covalent bondings while van der Waals force keeps the layers together along the *c*-axis, and the interlayer spacing is ~0.8 nm. Fig. 1(a) shows the schematic of GaTe crystal structure which is monoclinic lattice with low symmetry. Devices of thin flakes of GaTe were fabricated by the van der Waals stacking process. A configuration of such a device is depicted in Fig. 1(b), where few-layered GaTe flakes were sandwiched by two hexagonal boron nitride (h-BN) layers with a thickness of about 20 nm.

Due to its insulating and inert properties, h-BN serves as a proper dielectric layer and provides preservation of GaTe for its intrinsic properties. Layered h-BN can also provide an atomically flat substrate which is conducive to improving the performance of the device. We have performed systematic measurements on multiple devices and most of them exhibit similar behaviours. We will mainly discuss the representative device here, an optical micrograph is shown in Fig. 1(c), thin flake of GaTe is highlighted with red dashed line. Fig. 1(d) shows the atomic force migraph (AFM) scan, corresponding to the heterostructure in Fig. 1(c). It can be seen that the surface of the sample obtained by dry transfer is quite clean and flat. GaTe flake in this device is ~24.5 nm (Fig. 1(e)).

Fig. 2(a) displays the transfer characteristics of the device at T = 300 K; i.e., the source-drain current I_{ds} dependence on the gate voltage V_g in the range of ±100 V. A typical p-type FET behaviour can be observed which is similar with other reports, at the hole side, an "ON/OFF" ratio of ~10^4 and a subthreshold swing (SS) of ~356 mV/dec can be extracted from the curve. Further improvement for the SS might be achieved by employing graphite and h-BN as the gate electrode and dielectric layer, respectively. Surprisingly, when taking a closer look at the transfer curves in the range of V_g > 70 V, we can see the device also slightly turns on which is more obvious when plotted in log scale (shown in Fig. 2(b)), which is the hallmark of a bipolar behaviour. To better characterize the performance of the device, we performed output tests. As can be seen in Fig. 2(c), the device turns on as V_g < −20 V and linear I_{ds}–V_{ds} curves at different fixed V_g indicate that Ohmic contacts have been achieved on the hole side. For the electron side, the device turns on as V_g > 80 V, which further indicates that ambipolar transport is realized, suggesting GaTe will be a good candidate for being used in multi-functional devices such as p–n juctions and tunnel diodes. In contrast, the I_{ds}–V_{ds} curves on the electron side largely deviate from linear behaviour and the "ON" current is relatively weak. Further enhancement of the transport properties on the electron side may be realized by trying high-κ dielectric layer[13] or electric-double layer (EDL)[28].

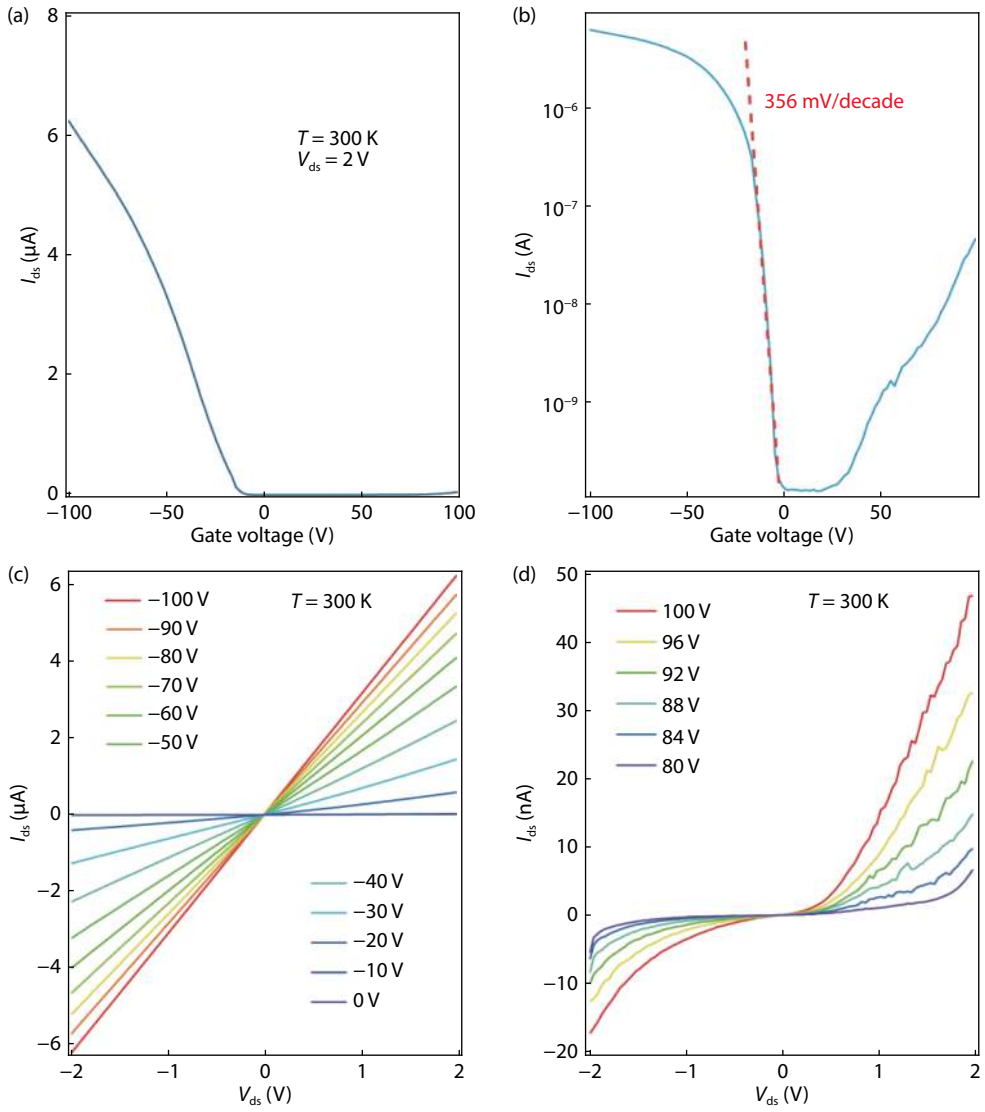

Fig. 2. (Color online) Electrical transport properties of BN/GaTe/BN devices at room temperature. (a) Field effect curve at V_{ds} = 2 V of the device. (b) The same data plotted in a log scale. (c) I_{ds}–V_{ds} curves on the hole side at fixed gate voltages. (d) I_{ds}–V_{ds} curves on the electron side at fixed gate voltages.

In Fig. 3, we display the transport properties of the device at different temperatures. Fig. 3(a) shows the color map of I_{ds}–V_{ds} curves as a function of gate voltage at different temperatures. The distinct behaviour of a bipolar FET can be observed at all temperatures suggesting the ambipolar transport property is quite robust while the gap becomes a little larger on lowering the temperature. As can be seen in Fig. 3(b), the I_{ds}–V_{ds} curve remains linear at 50 K while slightly deviate from linear below 50 K. Furthermore, it is of a surprise to see that the "ON" current becomes much higher at low temperature. However, similar increasement of current was not observed on the electron side, see Fig. 3(c).

We now examine the transport characteristics of few-layered GaTe device at various temperatures in more detail. Fig. 4(a) presents the conductivity (σ) plotted in the unit of quantum conductance (e^2/h). Clear metal-insulator transition (MIT) behavior can be seen because the device has metallic ground state with a residual resistance at hole doping (V_g = –40 V, for example), while it enters insulating regime when V_g approaches to 0 V. As shown in Fig. 4(b), with increased hole doping, the output curves of the device display a crossover from an insulating regime at higher gate voltage (V_g > –30 V), where I_{ds} increases with the temperature increasing, to a metallic regime at lower gate voltage (V_g < –30 V), where I_{ds} increases as the temperature decreases. Similar behaviour has been observed in multiple few-layered GaTe devices. This MIT phenomenon was observed for the first time in GaTe flakes, and our results are consistent with previous studies on WSe_2, MoS_2, WS_2[13, 29, 30].

To further understand this, we plot the field-effect mobility in the metallic regime (V_g = –40 V) as a function of temperature using the expression $\mu = \frac{dI_{ds}}{dV_{bg}} \times \frac{L}{WC_{bg}V_{ds}}$[31], where L is the channel length, W is the channel width, $C_{bg} = \frac{\varepsilon_0}{(d_1/\varepsilon_1)+(d_2/\varepsilon_2)}$ is the capacitance per unit area, and d_1, d_2 are the thicknesses of h-BN dielectric and SiO_2 dielectric, respectively. As shown in Fig. 4(c), as temperature decreases, our devices display a remarkable increase in field-effect mobility: from ~40 $cm^2V^{-1}s^{-1}$ at 300 K to ~1200 $cm^2V^{-1}s^{-1}$ at 3 K. In the temperature range of 100–250 K, the field-effect mobility can be well fitted by a power law $\mu \sim T^{-\gamma}$ with the ex-

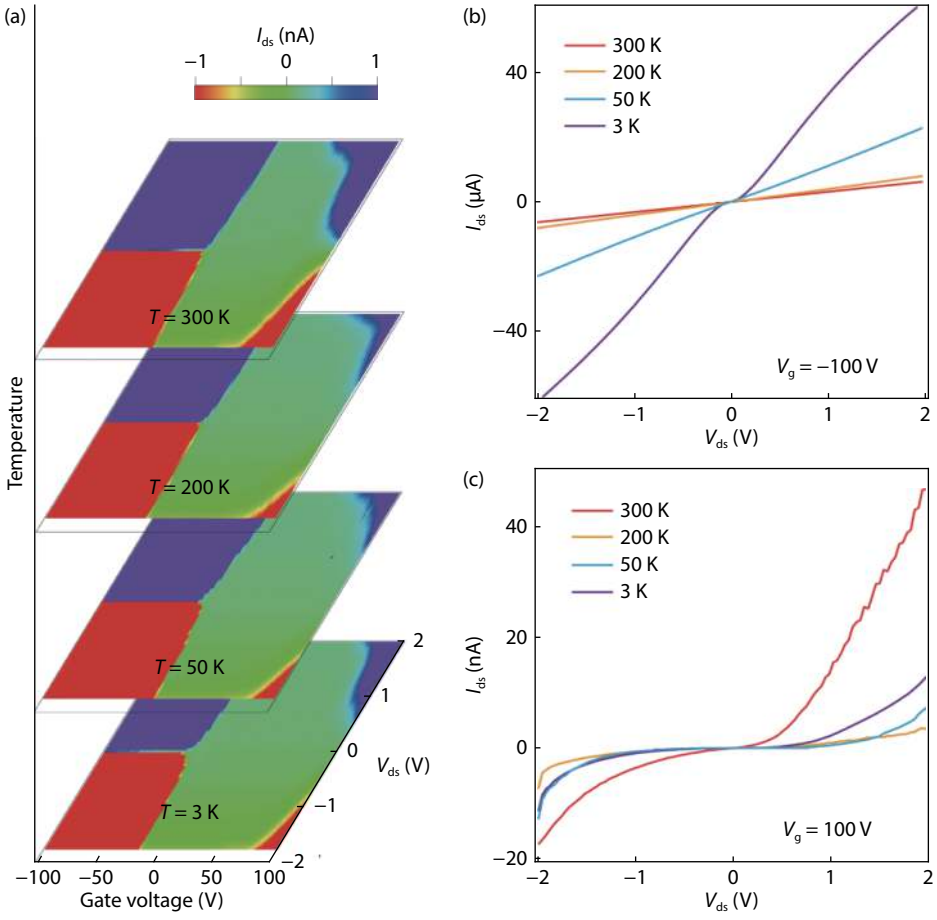

Fig. 3. (Color online) Transport properties of BN/GaTe/BN devices at different temperatures. (a) Color map of *I*–*V* curves as a function of gate voltage at different temperatures. To enhance the visibility, color scales are set to cutoffs at ±1 nA. (b, c) Line cuts in (a), with output curves on hole and electron sides, respectively.

ponent *γ* around 0.86 (black solid line). This value is comparable to single-layer WS_2 (0.73)[32] and monolayer MoS_2 (0.78)[13]. Moreover, the field-effect mobilities of our devices keep increasing rapidly below 100 K with an almost unsaturated state. This suggests that the domination of phonon scattering remains in temperatures down to ~10 K, which can be attributed to the atomically flat interface and suppressed impurity scattering provided by the h-BN encapsulation[33].

4. Conclusion

Fabricating few-layered GaTe tansistors encapsulated in h-BN offers more opportunities for intrinsic properties research with GaTe. Transport measurements of GaTe FETs have proven that GaTe could serve as a platform for electronic systems thanks to its formidable ability in carrier modulation. Metal-insulator transition has been achieved in thin flakes of GaTe with a Si back gate. In addition, ambipolar behaviour was also observed in our devices making it promising for the implementation of nanoelectronic systems that envolves semiconducting channels. Our findings manifest the potential of GaTe for future functional devices based on it.

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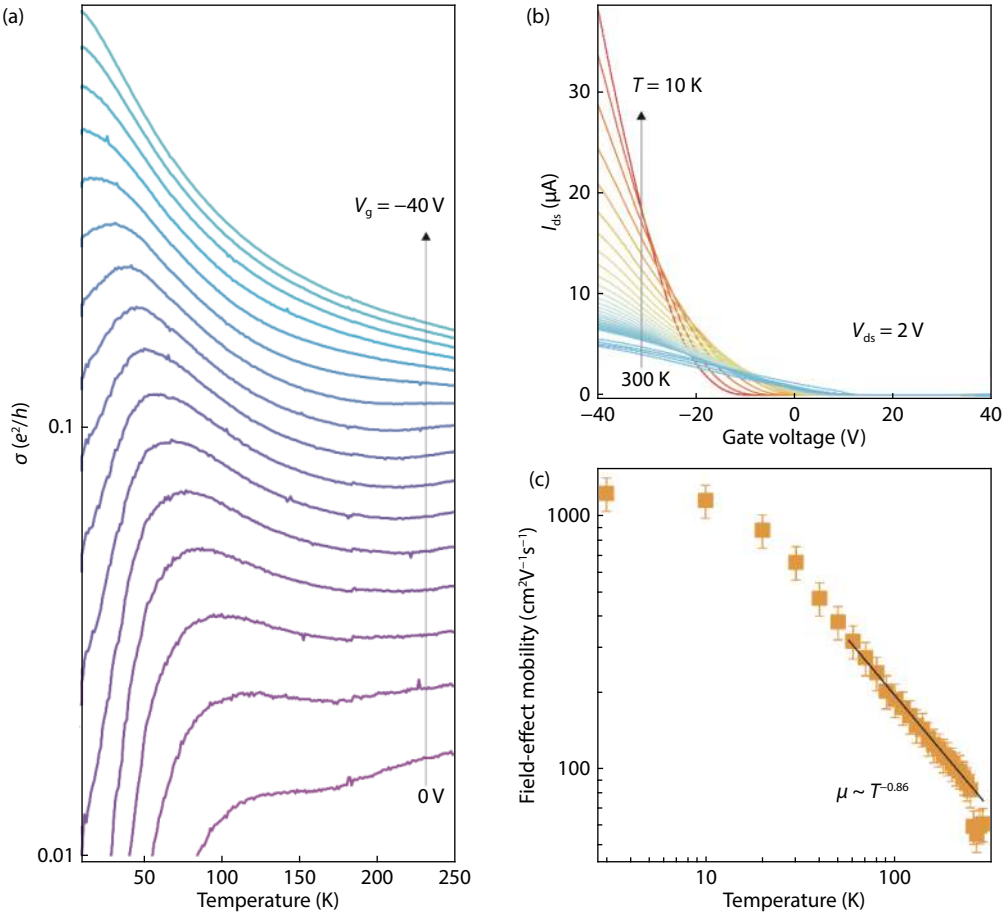

Fig. 4. (Color online) Temperature-dependent transport characteristics in few-layered GaTe device with a constant voltage V_{ds} = 2 V. (a) *T*-dependence of conductivity σ for different gate voltages. (b) I_{ds}–V_g at different temperatures, I_{ds} increases when the temperature decreases at high negative gate voltage V_g < −30 V. (c) Field-effect mobility as a function of temperature. The solid black line is best fitted to the power law in the range of 100–250 K.

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