REVIEWS

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Contact engineering for two-dimensional semiconductors

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Abstract: Two-dimensional (2D) layered materials, including graphene, black phosphorus (BP) and transition metal dichalcogenide (TMD) such as molybdenum disulfide (MoS_2), tungsten diselenide (WSe_2), have attracted increasing attention for the application in electronic and optoelectronic devices. Contacts, which are the communication links between these 2D materials and external circuitry, have significant effects on the performance of electronic and optoelectronic devices. However, the performance of devices based on 2D semiconductors (SCs) is often limited by the contacts. Here, we provide a comprehensive overview of the basic physics and role of contacts in 2D SCs, elucidating Schottky barrier nature and Fermi level pinning effect at metal/2D SCs contact interface. The progress of contact engineering, including traditional metals contacts and metallic 2D materials contacts, for improving the performance of 2D SCs based devices is presented. Traditional metal contacts, named 3D top and edge contacts, are discussed briefly. Meanwhile, methods of building 2D materials contacts (2D top contact and 2D edge contact) are discussed in detail, such as chemical vapor deposition (CVD) growth of 2D metallic material contacts, phase engineered metallic phase contacts and intercalation induced metallic state contacts. Finally, the challenges and opportunities of contact engineering for 2D SCs are outlined.

Key words: two-dimensional materials; contact engineering; Schottky barrier; Fermi level pinning; heterostructures

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1. Introduction

Silicon (Si) based technologies are the basis of complementary metal oxide semiconductor (CMOS) field effect transistor (FET) devices and they are the main driving force for the rapid growth of information technology[1, 2]. Based on Moore's law, higher speed and larger capacity will be obtained by miniaturization of the device dimensions in modern electronics. However, further scaling down the Si-based CMOS FET has encountered significant challenges from fundamental quantum mechanical limitation effects[1]. The discovery of novel materials to continue Moore's law and innovative CMOS technology is extremely urgent for future ultra-low power electronics and flexible devices[3, 4]. Under this background, atomically thin 2D materials, such as graphene[5–10], black phosphorus[11–15], boron nitride[16–20], and transition metal dichalcogenide[21–31], have attracted widespread attention thanks to their diverse optical and electrical properties. Taking advantage of the atomically thin nature of 2D materials, further scaling down the device dimensions without invoking detrimental short channel effects in 2D SCs based CMOS FETs is possible[32, 33]. In addition, the attractive features of 2D materials enable us to study the mechanism of tunneling and avalanche effect[34–36] and thermionic emission phenomenon[37] at atomic dimension, which is the key to developing nanoscale transistors[38], high breakdown voltages transistors[39], neuromorphic chips[40] and so on.

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Contact resistance is critical for achieving high performance and low power consumption in Si-based CMOS FET or advanced 2D SCs based integrated circuits. Contacts are the communication links between these 2D SCs and external circuitry. The properties of the interface between metal–2D SCs govern the performance of these devices, including drain current[41], carrier mobility[42], photoresponse[43], signal-to-noise ratio[44], power dissipation[45] and so on. Compared to the concept of conventional Si based metal–semiconductor contact, many bottlenecks can be broken down because the 2D SCs are thinner than the depletion and channel length. They also show advantageous transistor performance. However, the main issue is still the large contact resistance at the interface between the metal electrode and the 2D SCs. According to $R_c = h/(2e^2k_f) = 0.026/(n_{2D})^{1/2}$, the typical contact resistance to monolayer MoS_2 is about three orders of magnitude larger than that from the quantum limit at a charge carrier density of 10^{13} cm^{-1}[46], where n_{2D} is charge carrier density, h, k_f and e is Planck's constant, Fermi wavevector and electron charge, respectively. Therefore, there is plenty room to make high-quality contacts by in-depth study the detailed physics of contacts between metal and 2D SCs.

In this review, the state-of-the-art studies of contact engineering of 2D SCs are summarized. We first introduce the background of 2D materials. Next, we discuss the contact geometry and the nature of metal-2D SCs contact and describe the Fermi level pinning and Schottky barrier of metal-2D SCs briefly. Then, conventional metal contacts and metallic 2D materials contacts are discussed, where the advantages and disadvantages of each method are presented and illustrated by some examples. Especially, using metallic 2D materials as con-

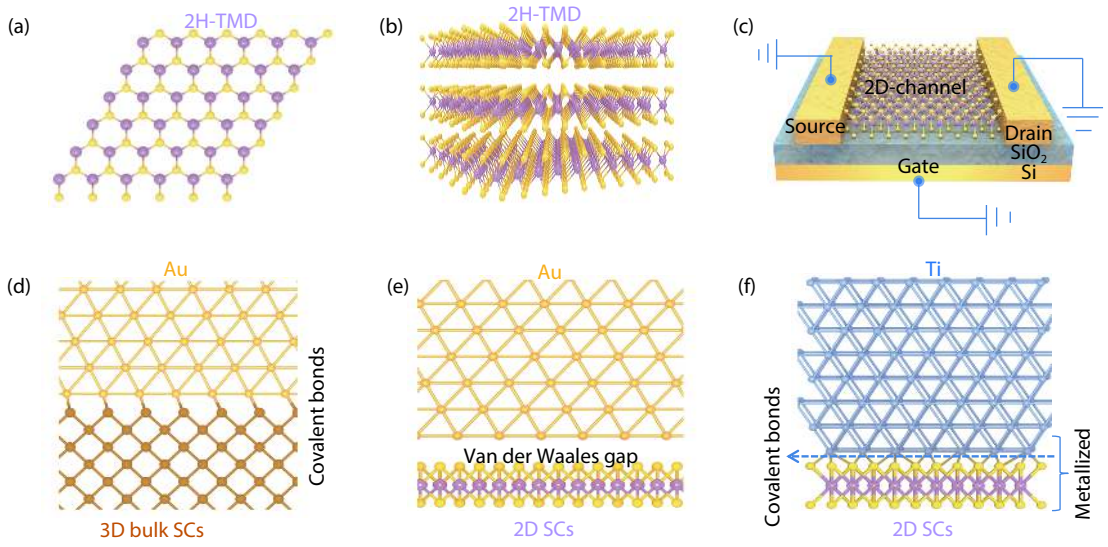

Fig. 1. (Color online) Atomic structure of representative 2D semiconductor materials and phase engineered contacts. (a, b) Top and side view of 2H stacked structure of 2D semiconductor. (c) Device model of 2D SCs based device. (d–f) Different types of metal–semiconductor junction with contact interface.

tacts is discussed in details in this review. Finally, the challenges and under-explored aspects of the contact engineering of 2D SCs are proposed.

2. Development of 2D SCs

Layered materials, which have a strong covalent bonding within the layer and weak vdW interaction between the layers, have been widely studied thanks to their fascinating properties[47–49]. Early research has focused on graphene because of its remarkable electrical and optical properties, such as high carrier mobility and optical transparency[5–10]. Considerable efforts were then made to develop other layered materials, such as transition metal dichalcogenides (TMDs)[25, 50, 51] and single element semiconductor black phosphorus (BP)[11–15]. Among these layered materials, 2D SCs have received scientific interest because of their finite bandgaps ($E_g \approx 1$–2 eV)[52–54]. 2D SCs have a general chemical formula MX_2, where M represents the transition metal (e.g., Mo, W, Re or Ti) and X is chalcogen atom (e.g., S, Se or Te)[31, 55, 56]. Figs. 1(a) and 1(b) show the top view and side view of trigonal prismatic 2H hexagonal structure for Mo or W based dichalcogenides, respectively, where the transition metal Mo or W within the two layers of sulfur forms a "sandwich-like" structure. In bulk 2D SCs, the materials have indirect bandgaps within the range of 0.9–1.6 eV[52]. However, when bulk group VIB 2D SCs are thinned down to a monolayer, an indirect to direct transition will occur and the bandgaps will be increased to 1.6–2.0 eV[53] thanks to quantum confinement effects. For example, bulk MoS_2 has indirect bandgap of about 1.2 eV, while the monolayer counterpart has direct bandgap of about 1.8 eV[54]. Although graphene has distinctive electrical and optical properties, the absence of sizable bandgap limits its application in many electronic devices. In contrast, 2D SCs with tunable bandgaps have a promising outlook in fabricating electronics. Many methods have been used to prepare single and multi-layer 2D materials, including mechanical, chemical and electrochemical methods, which has been summarized by previous works[23]. Since this review focuses on the contact engineering for 2D SCs, the details of these preparation methods are not discussed here.

3. Contact geometry and Schottky barrier of a metal-2D SC contact

3.1. Contact geometry

The field effect transistor (FET) is the most fundamental and common unit for electronic devices used in fundamental research and industry, as shown in Fig. 1(c). Heavily doped Si is used as the conductive substrate, where the back gated voltage is applied. The thermally oxidized SiO_2 on Si substrate with thickness in the range of 90–300 nm is a dielectric layer and the 2D SCs can either be mechanically exfoliated or CVD grown onto the substrate. As the 3D top contact, the surface of bulk (3D) SCs tends to form covalent bonds with metals, shown in Fig. 1(d). However, for the metal-2D SC contact, it is difficult to form covalent bonds on the surface of 2D SCs. There will be a van der Waals gap between the interface of the metal (such as Au) and 2D SCs[57], as shown in Fig. 1(e). Allain *et al.* pointed out that this 3D top contact with van der Waals gap interface is an additional 'tunnel barrier' for carrier injection before the inherent Schottky barrier (SB)[58], which will result in a higher contact resistance. However, although an additional resistance may be caused by the non-bonding vdW gap, its Schottky tunnel barrier width (λ_{SB}) is too small (0.1 to 0.15 nm) to affect the carrier transport and can largely be neglected[59, 60]. In fact, owing to the existence of vdW gap, a cleaner metal-2D SCs interface can be formed and the crystal lattice of 2D SCs underneath the contact will be maintained in an unperturbed state, yielding to lower contact resistance and higher carrier mobility[61]. Another alternative method is to select a matched contact metal, which will be hybridized with the atoms of 2D SCs through covalent bonding. According to the density functional theory (DFT) calculation, covalent bonds can be formed at the interface between the 2D SCs and some specific metals, such as Ni for graphene[62], Ti for MoS_2[63]. In the case of monolayer MoS_2, the nonlocalized overlap states will be intro-

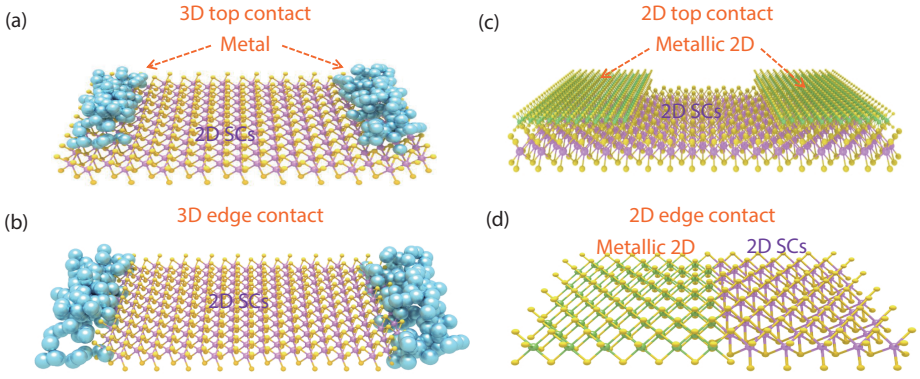

Fig. 2. (Color online) (a, b) 3D top contact and 3D edge contact configuration of metal-2D SCs contact. (c, d) 2D top contact and 2D edge contact of metallic 2D-SCs contact geometries.

duced in the bandgap of MoS_2 by Ti contact, causing a totally metallized state of monolayer MoS_2[57], as shown in Fig. 1(f). At this situation, the contact resistance decreases significantly. It should be noted that covalent bonding at the interface of metal-2D SCs may be out of work for multilayer 2D SCs because only the top layer can be hybridized, which will increase the contact resistance. Furthermore, Fermi level pinning effect has to be taken into account if the metal was hybridized with 2D SCs through covalent bonding[63] because the Schottky barrier height (Φ_{SB}) can be changed significantly by such effects.

Although 3D top contact is commonly used between metal electrode and 2D SCs (Fig. 2(a)), considering the disadvantages of such contact, a 3D edge contact is proposed to overcome the Fermi level pinning effect at the interface (Fig. 2(b)). Both experiments and DFT calculation have shown the numerous advantageous of 3D edge contacts[64]. However, it is difficult to form a pure 3D edge contact by standard electron-beam lithography technique because of the atomically thin nature of 2D materials, where encapsulation of the SCs by hBN or thin oxide is needed[65–69]. Apart from traditional metal contact, contacting 2D SCs using other 2D metallic materials is an elegant and convenient approach to decrease contact resistance and Schottky barrier. Schematic diagrams of 2D top contact and 2D edge contact are shown in Figs. 2(c) and 2(d), respectively. Three fundamental methods—CVD growth, phase engineering and intercalation treatment—are adopted to achieve 2D metallic contacts. High quality vertical and lateral heterostructures, such as VS_2-MoS_2, have been synthesized by the two step CVD method[70–75]. These authors found that when compared to Ni/Au contact, the carrier mobility was improved at least four times and the Φ_{SB} was reduced from 163 to 30 meV by 2D metallic VS_2 contact[75]. Similarly, heteroepitaxial stacking of monolayer metallic 1T-WTe_2 and SC 2H-WSe_2 was achieved by two step CVD growth[76]. A distinctively low contact barrier below 100 meV was established across a clean epitaxial vdW gap. Furthermore, other 2D metallic-SCs heterostructures, such as vertical $NbTe_2$-WSe_2 and lateral graphene–MoS_2 heterostructures, are synthesized by two step CVD method, where the performance of the FETs is improved greatly by 2D metallic materials contact[77]. It is also possible to achieve a metallic state via direct substitutional doping, such as Nb doping induced metallic state in monolayer WS_2, which can serve as a metallic contact[78, 79]. Aside from the CVD growth method, phase engineering is an effective way to transform the 2D SC into a metallic phase. By treating 2D SCs (e.g., monolayer or few layer MoS_2) with n-butyl lithium, an uncovered region could be converted from 2H SC to 1T metallic phase[80]. In addition, Ar plasma or laser induced 2H SC to 1T metallic phase transition has also been reported by Zhu *et al.* and Cho *et al.*[80, 81]. The phase transition area of 2H–1T can be selected by the patterning process and the performance of these devices is substantially improved. Intercalation is also a promising method to turn the 2D SC to metallic state, which has seldom been explored to integrate 2D materials[82]. Combining with lithography, a spatially and size controlled metallic state could be realized by Co intercalation SnS_2.

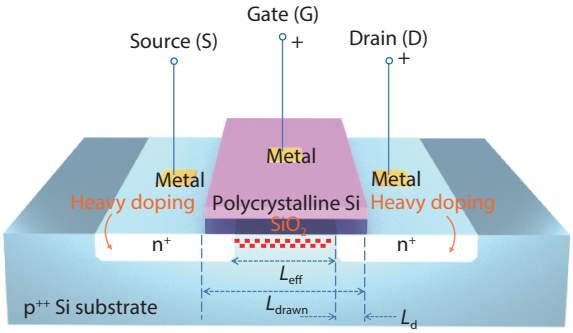

Fig. 3. (Color online) Schematic diagram of a conventional Si-based NMOS FET.

3.2. Schottky barrier of a metal-2D SC contact

In traditional Si-based CMOS integrated circuits, ohmic contacts are realized by heavy ion diffusion or implantation in body Si substrate. A simplified schematic diagram of an n-type MOS (NMOS) FET is shown in Fig. 3. The NMOS FET is fabricated on the p-type Si substrate, where the thickness of body Si is less than 1 mm generally. The L_{eff} and t_{ox} are the effective channel length and thickness of oxide, and the typical value of which are about 0.15 μm and 50 Å, respectively[1, 2]. The driving force of the development of CMOS integrated circuits is to scale down the L_{eff} and t_{ox} continuously. Source (S) and drain (D) are formed by heavy electron doping, also known as the n^+ region. Heavily doped polycrystalline silicon is regarded as a gate electrode. The contact between the metal and the heavily doped region (source and drain) is called an ohmic contact. For conventional CMOS circuitry, an ohmic contact is essential to achieve high performance devices for either n or p type transports. The main indicat-

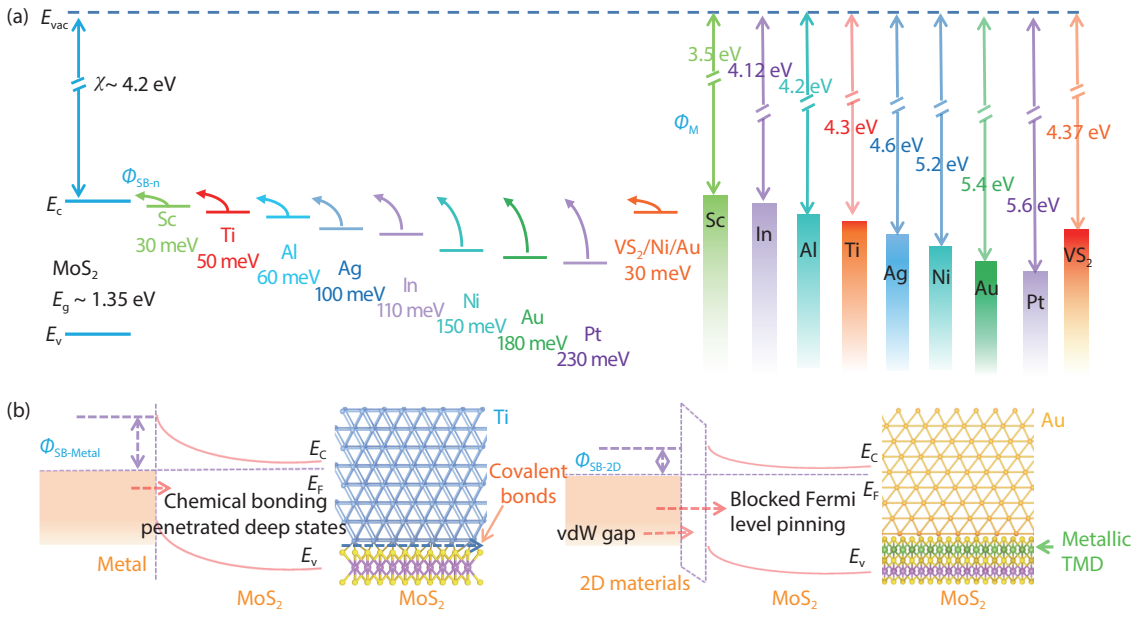

Fig. 4. (Color online) (a) Schematic diagram of various metal–MoS_2 band alignments along with work function of metal (Φ_M). The Fermi level of metal is lined up close to conduction band of MoS_2. The left-hand part in Fig. 4(a) is the actual Φ_{SB} extracted from experiment, which is different from the theoretical value calculated by the difference of Φ_M (right-hand part in Fig. 4(a)) and electron affinity (χ) of MoS_2. For example, theoretical values of Φ_{SB} for Sc–MoS_2 and Pt–MoS_2 contact are about –0.7 and 1.4 eV, respectively. However, the actual Φ_{SB} obtained from experiment is only 30 and 230 meV, indicating that there is a strong Fermi level pinning effect at the interface of metal and 2D SCs. (b) Energy band diagrams of MoS_2 with and without 2D metallic materials.

or of an ohmic contact is the specific contact resistance (R_c), which can be defined by[1, 2]

$$R_c \equiv \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \quad (\Omega \cdot \mathrm{cm}^2), \tag{1}$$

where J and V is current density and external bias voltage, respectively. For metal-SCs contact with low doping concentration of SCs, the thermionic emission current dominates. The characteristic of J–V can be represented as[1, 2]

$$J = J_s\left[\exp\left(\frac{qV}{kT}\right) - 1\right], \tag{2}$$

$$J_s = A^* T^2 \exp\left(\frac{-q\Phi_{Bn}}{kT}\right), \tag{3}$$

where J_s, A^*, T, k and Φ_{Bn} is saturation current density, effective Richardson constant, absolute temperature, Boltzmann constant and barrier height, respectively. Combining the Eq. (1), R_c can be derived by[1, 2]

$$R_c = \frac{k}{qTA^*}\exp\left(\frac{q\Phi_{Bn}}{kT}\right). \tag{4}$$

From Eq. (4), it can be found that R_c is proportion to Φ_{Bn}, a smaller R_c will be achieved if using lower Φ_{Bn} of metal-SCs contact. In contrast, if metal is contacted with heavily doped SCs, then the barrier width will be extremely narrow. In this situation, the tunneling current is dominant and can be estimated as[1, 2]

$$I \sim \exp\left[-\frac{C_2(\Phi_{Bn} - V)}{\sqrt{N_D}}\right], \tag{5}$$

$$C_2 = 4\sqrt{m_n \varepsilon_s}/\hbar, \tag{6}$$

where N_D, m_n, ε_s and $\hbar$ is concentration of donor, effective mass, dielectric constant of silicon and reduced Plank constant, respectively. R_c can be expressed by[1, 2]

$$R_c \approx \exp\frac{C_2\Phi_{Bn}}{\sqrt{N_D}} = \exp\frac{4\Phi_{Bn}\sqrt{m_n\varepsilon_s}}{\sqrt{N_D}}. \tag{7}$$

From Eq. (7), a small R_c can be realized by high doping concentration. As aforementioned, in conventional Si-based CMOS circuits, ohmic contacts are realized by heavy doping. However, when Si is substituted by 2D SCs, such controllable and sustainable doping strategies are not applicable to the 2D SCs based FET because of their fragility. Most contacts between metal and 2D SCs are Schottky contacts, which will increase contact resistance and limit the carrier injection. Therefore, reducing the Φ_{SB} of metal and 2D SCs contact is an effective way to improve carrier injection efficiency.

Fig. 4(a) shows a schematic diagram of several metal-MoS_2 band alignments along with work function of metal (Φ_M)[46, 49, 57, 63, 64]. The electron affinity (χ) of MoS_2 can be given by the energy difference of conduction band E_c and the vacuum level E_{vac}. Schottky barrier height, which is a tunnel barrier for carrier injection to cross the junction, is one of the most important parameters for the metal/SCs contact because it can fundamentally determine charge transport efficiency and impact device performance. If low Φ_M metal is aligned with the Fermi level (E_F) close to the conduction band, then electron injection will be facilitated. Otherwise, if high Φ_M metal aligned with E_F close to valence band, then hole injection will be promoted. In an ideal metal-2D SCs interface, Φ_{SB} is characterized by the Schottky–Mott rule, which is governed by electrostatics that involve energy-level align-

ments[83, 84].

$$\Phi_{SB\text{-}n} = \Phi_M - \chi_S, \quad (8)$$

$$\Phi_{SB\text{-}p} = E_g + \chi_S - \Phi_M, \quad (9)$$

where $\Phi_{SB\text{-}n}$ and $\Phi_{SB\text{-}p}$ are Schottky barrier heights for electrons and holes, respectively. E_g are bandgaps of the 2D SCs. Ideally, all of the parameters are followed by a Schottky–Mott rule and Φ_{SB} is linearly dependent on the Φ_M with a slope of unity. However, in fact, an ideal metal–2D SCs contact rarely forms and the Φ_{SB} is often incorrect estimated by Schottky–Mott mode, which was first noted by Bardeen in 1947[85]. According to the Bardeen limit, Φ_{SB} is usually independent on Φ_M, which lies between the Schottky and Bardeen limit. The Fermi level of metal is pinned to a nearly fixed position within the bandgap of SCs. For a given SC, the actual Φ_{SB} is given by Eq. (10) and the strength of Fermi-level pinning can be characterized by the interface S parameter (Eq. (11))[83]:

$$\Phi_{SB\text{-}n} = (S\Phi_M - \chi_S) + (1 - S)\Phi_{IS}, \quad (10)$$

$$S = d\Phi_{SB\text{-}n}/d\Phi_M, \quad (11)$$

where Φ_{IS} and S are the interface state energy of SC and Schottky pinning factor, respectively. If $S = 0$, then Φ_{SB} is independent of metal Φ_M, which indicates the strong pinning effect at the metal–SC interface. If $S = 1$, then Φ_{SB} is determined by Eqs. (1) and (2), and the Schottky–Mott limit is achieved. In the case of MoS_2 and Ti contact, the theoretical value of Φ_{SB} is about 0.1 eV according to Eq. (8). The actual Φ_{SB} from experiment is about 50 meV[86], which is lower than that from the theoretical calculation. As shown in the left-hand part of the band alignments of various metal–MoS_2 in Fig. 4(a), the Fermi level of metals (e.g., Sc, Ti, Ag and Pt etc.) locates in the bandgap of MoS_2 near the conduction band[86]. It is worth mentioning that the extracted Φ_{SB} of 2D metallic VS_2 contacted MoS_2 device is only 30 meV, which is much lower than that from Ni–MoS_2 contact (170 meV)[75]. As the interlayer between the metal and MoS_2, the surface of the MoS_2 was protected by VS_2 and the Fermi level pinning effect can be avoided. The energy band diagrams of MoS_2 without and with 2D metallic materials are shown in Fig. 4(b), where the Φ_{SB} was reduced in 2D metallic-SCs contact. The origin of the Fermi level pinning may be attributed to the charge redistribution at the interface of metal–2D SCs contact or the interaction between the contact metal and the chalcogen component[49, 57]. There is at present no consensus of the origin of Fermi level pinning and the origin has been discussed elsewhere[49, 57].

4. Conventional metal contacts and 2D metallic material contacts

In this part, we first discuss the strategies of conventional metal contacts (3D top contact and 3D edge contact) to decrease the contact resistance and improve carrier injection efficiency, including selecting matched contact metal, designing contact geometry, introducing special metal interlayer and metal transfer approaches. Next, strategies to introduce 2D metallic materials contacts (2D top contact and 2D edge contact) are discussed in detail, such as CVD growth of 2D metallic materials as contact, phase engineering of 2D SCs to metallic phase as contact. Finally, we discuss an intercalation strategy to induce metallic state.

4.1. Conventional metal contacts

4.1.1. Select matched contact metal

Due to the lack of controllable and sustainable doping strategies for 2D SCs FET, the contact quality and resistance are determined by the contact metal. Therefore, a proper understanding and choice of source/drain contacts metals is essential to improve the performance of 2D SCs-based FETs. Das *et al.* presented a thorough experimental study of contacts to MoS_2 by using different Φ_M metals such as Sc (Φ_M = 3.5 eV), Ti (Φ_M = 4.3 eV), Ni (Φ_M = 5.3 eV) and Pt (Φ_M = 5.6 eV)[86]. Figs. 5(a) and 5(b) show the prototype back gated MoS_2 transistor and the corresponding SEM image. The AFM and optical images are shown in Fig. 5(c) and the inset figure, where the thickness of mechanical exfoliated MoS_2 flake is about 3 nm. Assuming that an ideal interface has been formed by MoS_2–metal, the Φ_{SB} will be determined by Schottky–Mott rule. The expected Fermi level of metal with the electronic bands of MoS_2 is shown in Fig. 5(d), where only the difference of the electron affinity of MoS_2 and the Φ_M of the corresponding metal is considered. The electron injection to conduction band should occur for low Φ_M metal of Sc and Ti, while high Φ_M metal Ni and Pt provide access to hole injection to valence band. In other words, n-type FET characteristics should be obtained by Sc and Ti contact, while p-type FET transfer curves can be observed. However, from the experimental transfer curves (Fig. 5(e)) it can be seen that all of the metal contacts present n-type FET characteristics, indicating that the Fermi levels of all the metals are lined-up close to conduction band of MoS_2. The actual Fermi level of metal with the electronic bands of MoS_2 is shown in the inset of Fig. 5(e). In addition, the on-state current is decreased from Sc to Pt contact at positive V_{gs}, indicating different carrier injection efficiency for various contact metals.

Fig. 5(f) shows the temperature-dependent transfer curves with Ni contact, which was used to create the Arrhenius plot in Fig. 5(g). The actual Φ_{SB} can be revealed by the Arrhenius plot if the flat band voltage V_{FB} is identified, and the V_{FB} has been marked in Fig. 5(g). Note that the contributions of thermionic emission and thermally assisted tunneling are identified at different V_{gs} in Fig. 5(d). Based on the conventional thermionic emission theory, the slope of the curves in high-temperature region is presented. The Φ_{SB} is extracted by equation[86]:

$$I_{ds} = AT^2 \exp[(q\Phi_{SB}) / (k_B T)]\{1 - \exp[(qV_{ds}) / (k_B T)]\}, \quad (12)$$

where I_{ds}, A, k_B, q, T and V_{ds} are the current through the device, Richardson's constant, Boltzmann constant, electronic charge, temperature and source to drain bias, respectively. From Fig. 5(h), the extracted Φ_{SB} of Ni-contacted MoS_2 is 150 meV, much lower than that calculated from Schottky–Mott rule. Fig. 5(i) shows the extracted Φ_{SB} from different metals with MoS_2 as a function of their corresponding Φ_M. The Φ_{SB} is 30, 50, 150, and 230 meV for Sc, Ti, Ni, and Pt, respectively. The slope extracted by $d\Phi_{SB}/d\Phi_M$ (interface

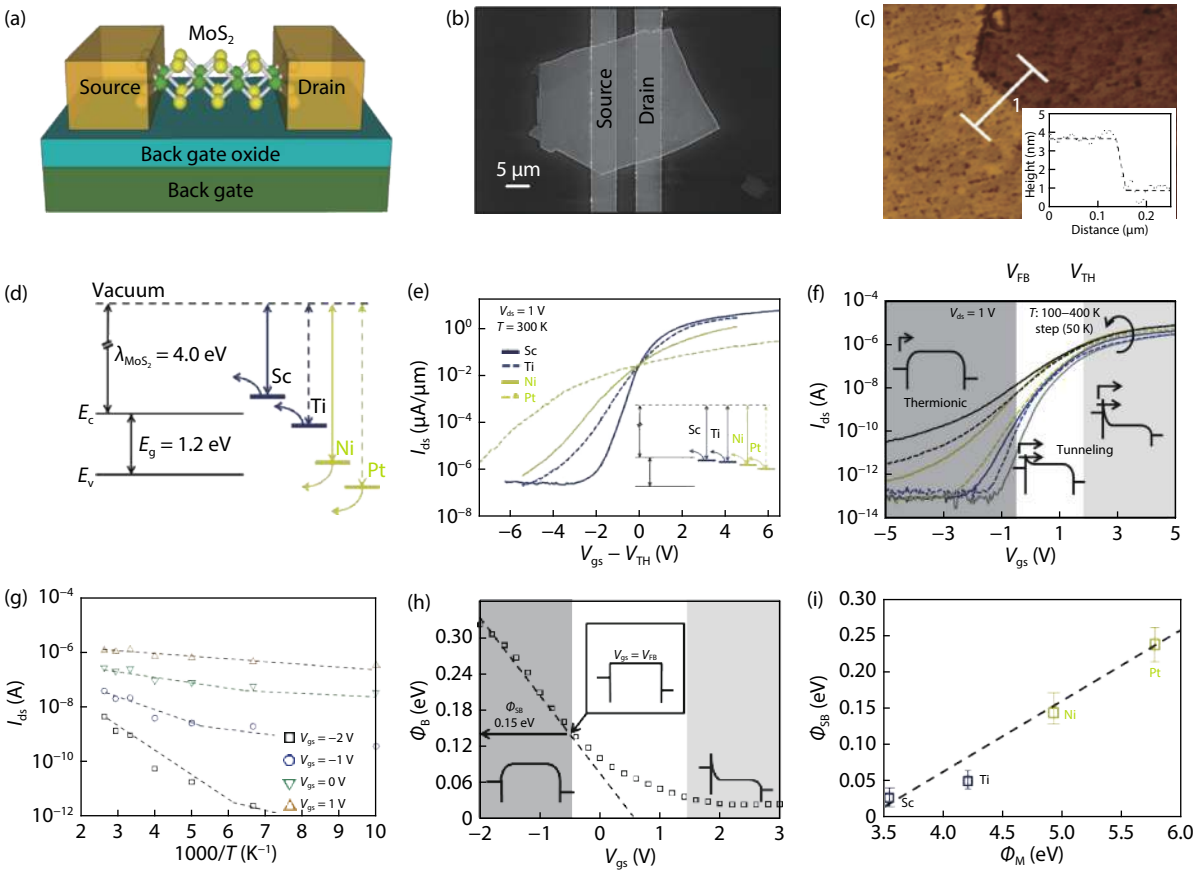

Fig. 5. (Color online) Metal contact investigation of MoS_2 device. (a) Schematic diagram of back gated MoS_2 transistor. (b, c) SEM and AFM images of device with MoS_2 thickness of 3 nm. (d) The expected position of the metal Fermi level across the band of MoS_2, where the Φ_{SB} was decided by the Schottky–Mott rule. (e) Transfer characteristics of MoS_2 device with different contact metal. The inset is the actual position of Fermi level of from experimental date. (f) Temperature-dependent transfer curves with Ni contact, where the contribution of thermionic emission and thermally assisted tunneling are marked. (g) Arrhenius-type plot from (a). (h) Extracted actual Φ_{SB} for Ni-contacted MoS_2 device. (i) The relationship of Φ_{SB} with metal work function[86]. Copyright 2013, American Chemical Society.

parameter S) is about 0.1, which indicates strong Fermi level pinning effects at the metal–MoS_2 interface and the Fermi levels of metal are pinned close to the conduction band in the bandgap of MoS_2. It also explains why all of the metal contacts present n-type characteristics, even when using the large Φ_M metal. The carrier mobility of MoS_2 with thickness of 10 nm is 184, 125, 36, and 21 $cm^2/(V{\cdot}s)$ for Sc, Ti, Ni and Pt contact. However, the mobility is less than 20 $cm^2/(V{\cdot}s)$ for Sc contact when the thickness of MoS_2 is reduced to 3 nm. The results indicate that the performance of monolayer or few layer MoS_2 FET can be further improved more effectively, except for the selection of the matched contact metal.

4.1.2. Introducing a special interlayer metal

Although the performance of 2D SCs FET can be improved by proper contact metal, the Fermi level pinning effect at the interface still limits the development of 2D SCs FETs. Creating van-der-Waals-type bonding between three-dimensional metal and 2D SCs is an ingenious method to improve the performance of 2D SCs FET. In a van-der-Waals-type contact, the contact resistance and Φ_{SB} can be decreased substantially. Furthermore, the Fermi level pinning effect at the metal–2D SCs interface can effectively be avoided[87]. Recently, Wang reported the realization of ultraclean van der Waals contacts between metal indium (In) and monolayer MoS_2, where the 10 nm In capped by 100 nm protection layer of Au was deposited by standard laboratory electron-beam evaporator under normal vacuum (< 10^{-6} Torr)[87]. The contact resistance of In/Au electrodes is only about 3000 and 800 $\Omega{\cdot}\mu m$ for monolayer and few layer MoS_2, which is the lowest value obtained among metal electrodes evaporated onto MoS_2. In addition, the carrier mobility reaches about 167 $cm^2/(V{\cdot}s)$ for monolayer MoS_2 based back-gated FET.

Fig. 6(a) shows a schematic of the In/Au contacted MoS_2 FET device. Cross-sectional annular dark field (ADF) scanning transmission electron microscopy (STEM) was used to verify the interface between In/Au–MoS_2. Fig. 6(b) shows ADF and bright-field STEM images. The atomic resolution cross-sectional image of In/Au and MoS_2 indicates that monolayer MoS_2 is atomically sharp with no detectable evidence of reaction with In/Au. In addition, there is no observed damage on MoS_2, indicating that In is gently deposited on the surface of MoS_2. These results demonstrate the presence of a high-quality contact interface through the formation of van-der-Waals-type bonding of MoS_2 and In layer. To investigate the performance of In/Au contacted MoS_2 FET, contact resistance and FET properties are measured. Figs. 6(c) and 6(d) show the measured contact resistance of CVD growth monolayer (0.7 nm) and mechanically exfoliated few-layer (8 nm) MoS_2 FETs us-

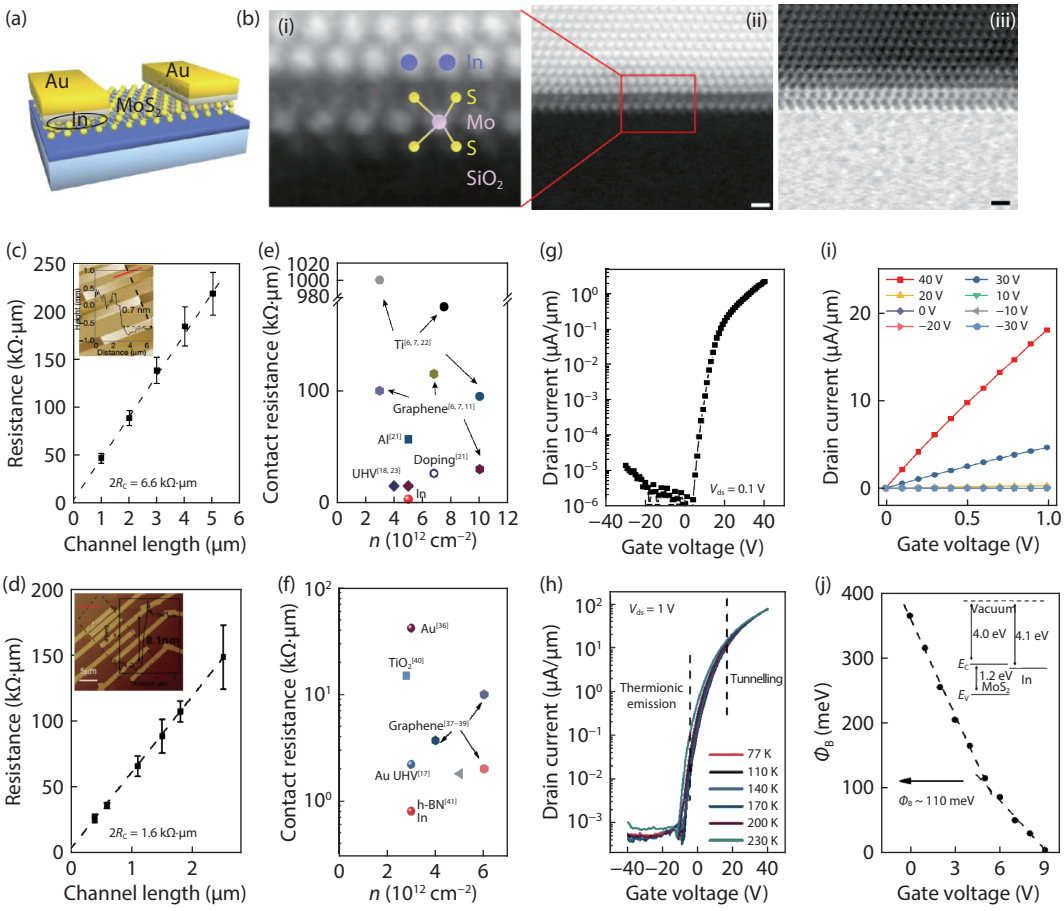

Fig. 6. (Color online) In contacted MoS_2 transistors. (a) Device mode of MoS_2 based back-gated device. The electrodes consist of 10 nm In layer capped with 100 nm Au. (b) Cross-sectional annular dark field (ADF) scanning transmission electron microscopy (STEM) of interface of In-MoS_2. (c, d) Extracted contact resistance using transmission line method for MoS_2 with thickness of 0.7 and 8.1 nm, respectively. (e, f) Comparison of contact resistance *versus* carrier concentration with different contact materials from literatures. (g, h) Transfer characteristics of device with monolayer MoS_2 and temperature-dependent transfer curves for 8 nm MoS_2 device. (i) Output curves with linear relationship indicates ohmic contact. (j) Extracted Φ_{SB} with value of 110 meV, indicates the ideal contact between the interface of In and MoS_2, which is nearly the same as the value decided by the Schottky–Mott rule. The inset is the energy band diagram of MoS_2 and In[87]. Copyright 2019, Nature Publishing Group.

ing transmission line method (TLM). The contact resistance is 3.3 ± 0.3 kΩ·μm (at $n = 5.0 \times 10^{12}$ cm^{-2}) and 800 ± 200 Ω·μm (at $n = 3.1 \times 10^{12}$ cm^{-2}), respectively. Figs. 6(e) and 6(f) compare the contact resistance from the literature, indicating that the contact resistances achieved in this work are the lowest among all carrier concentrations. Figs. 6(g) and 6(h) present the room temperature and temperature-dependent transfer characteristics of monolayer and few-layer MoS_2 FETs, respectively. A mobility of about 170 cm^2/(V·s) can be achieved by using In/Au electrodes with monolayer MoS_2 FET. Fig. 6(i) shows the output curves of monolayer MoS_2 FET, where the linear output characteristics indicate the absence of a contact barrier and ohmic contact. The Φ_{SB} extracted from few-layer MoS_2 in Fig. 6(j) is about 110 meV, which is consistent with the difference between work function of the metal and the conduction-band energy level of MoS_2. Furthermore, the achieved ideal contact demonstrates that the Fermi level pinning effect is absent at this interface. In conclusion, this work provides a simple method to make ultraclean van der Waals contacts with standard industrial technology.

4.1.3. Transfer metal electrode

Another approach to improve the performance of 2D SCs FET is to transfer the electrode to the surface of 2D SCs, which has recently been reported by Duan *et al.*[60]. Similar to the results of In/Au contacted MoS_2, a van der Waals contact without chemical disorder and Fermi level pinning between metal and MoS_2 can be created by transferring metal films (silver or platinum) on MoS_2. Ag or Pt contacted MoS_2 two-terminal FETs can achieve an electron and hole mobility of 260 and 175 cm^2/(V·s) at room temperature. Figs. 7(a)–7(c) show the cross-sectional atomic structure and optical image of transferred Au electrode on top of MoS_2. After peeling off the transferred metal electrode, the surface of MoS_2 retains its original shape. This indicates that the MoS_2 was not damaged during physical integration and the interface of metal-MoS_2 does not form a direct chemical bonding. A cross-sectional TEM image of transferred Au contacted MoS_2 is shown in Fig. 7(g), where the atomically sharp and clean metal-semiconductor interfaces can be observed. However, the surface of MoS_2 was damaged by electron-beam-deposited Au electrode, as shown in Figs. 7(d), 7(f), and 7(h), which suggests direct chemical bonding and strong metal–semiconductor interaction in deposition process.

Fig. 7(i) shows the transfer characteristics of MoS_2 with electron-beam-deposited metal electrode. All of the devices present n-type behavior irrespective of metals with high or

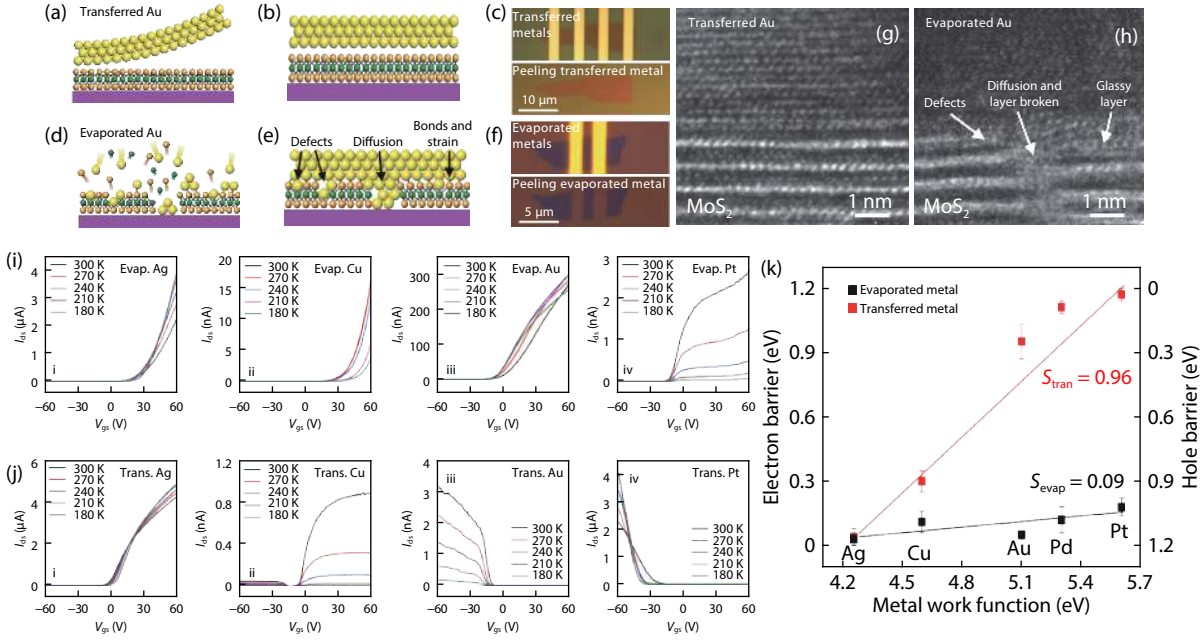

Fig. 7. (Color online) Transferred metal electrode contacted MoS_2 FET. (a–c) Cross-sectional atomic mode and optical images of MoS_2 device with transferred Au and the transferred Au mechanically released. (d–f) Cross-sectional schematics and optical images of MoS_2 device with traditional electron-beam-deposited Au and the deposited Au mechanically released. (g, h) Cross-sectional schematics and TEM images of transferred and evaporated Au. (i, j) Transfer curves of MoS_2 devices with different transferred and deposited metals. (k) Experimentally extracted Φ_{SB} for different transferred and evaporated metals[60]. Copyright 2018, Nature Publishing Group.

low Φ_M, which is consistent with previous studies[21, 49]. This can be assigned to the strong Fermi level pining near the conduction band of MoS_2. In contrast, for transferred metal electrodes, the carrier type can be tailored from electrons to holes by changing the Φ_M of contact metal, as shown in Fig. 7(j). The Φ_{SB} extracted from experiment as function of Φ_M for different transferred and evaporated metals are presented in Fig. 7(k). For transfer electrode contacted MoS_2 FET, the Φ_{SB} is strongly dependent on the metal Φ_M with a slope of 0.96 (S = 0.96), approaching thee Schottky–Mott limit. In contrast, the slope is only 0.09 (S = 0.09) for transitional electron-beam-deposited metal contact, which indicates the strong pinning effect at the metal–MoS_2 interface. The electron mobility of Ag transfer contacted MoS_2 FET is 260 $cm^2/(V·s)$ while the hole mobility of Pt transfer contacted is 175 $cm^2/(V·s)$. This work provides a general, low-energy metal integration approach to achieve high performance of 2D FET.

4.1.4. Metal edge contact

Considering the aforementioned limits of a 3D top contact, 3D edge contact has proven to be highly advantageous when compared with a 3D top contact in terms of carrier injection efficiency[86–90]. A 3D top contact has a wide tunnel barrier for its unfavorable out-of-plane carrier transport interface with low degree of covalency, while 3D edge contact has a more favorable in-plane carrier transport interface and smaller tunnel barrier. Though 3D edge contact has many benefits, it is difficult to realize pure edge contact by standard lithographic techniques. Recently, Wang *et al.* achieved the pure edge contact by capping insulting layer h-BN on the surface of graphene before metal deposition[65]. The insulating capping layer prevents the top surface of graphene from the direct contact with metal. The obtained contact resistance is as low as 100 Ω·μm and room temperature mobility reaches the theoretical phonon scattering limit[65]. Similarly, based on this method, h-BN encapsulated MoS_2 device with graphene edge contact was achieved by Cui *et al.*, as shown in Fig. 8(a)[66]. This method uses graphene as the bridge between MoS_2 and metal. Figs. 8(b)–8(d) show the temperature-dependent output curves, contact resistance and temperature-dependent Hall mobility, respectively. The linear output curves in Fig. 8(b) indicate the ohmic contact of this device. The record-high Hall mobility of 34 000 $cm^2/(V·s)$ was achieved at low temperature, and 120 $cm^2/(V·s)$ at room temperature, indicating the high contact quality.

Note that the edge contact in Fig. 8(a) is bridged by graphene and is not directly edge contacted with 2D SCs. Chai *et al.* fabricated the pure edge contacted MoS_2 device through pre-deposition Al_2O_3 by ALD or encapsulated h-BN on MoS_2[67]. Figs. 8(e) and 8(i) show the schematic illustration of preparation process called "passivation first, metallization second technique". Figs. 8(f)–8(h) show the electrical properties of the Al_2O_3 capped edge-contacted MoS_2 device, where the Schottky contact is obtained and the maximum mobility is about 9 $cm^2/(V·s)$. Figs. 8(j)–8(l) show output curves and transfer characteristic of the h-BN capped MoS_2 device. Its calculated contact resistance is about 314 kΩ and the mobility is only 1.2 $cm^2/(V·s)$ for the h-BN encapsulated device, which indicate that it may not be a truly ohmic contact even if the apparent linear dependence of current on drain voltage, as Das demonstrated in their report[86]. The results indicate that the edge contact quality between metal and MoS_2 using this "passivation first, metallization second technique" should be optimized in future.

4.2. Metallic 2D material contacts

Apart from conventional metal contact, integrating 2D

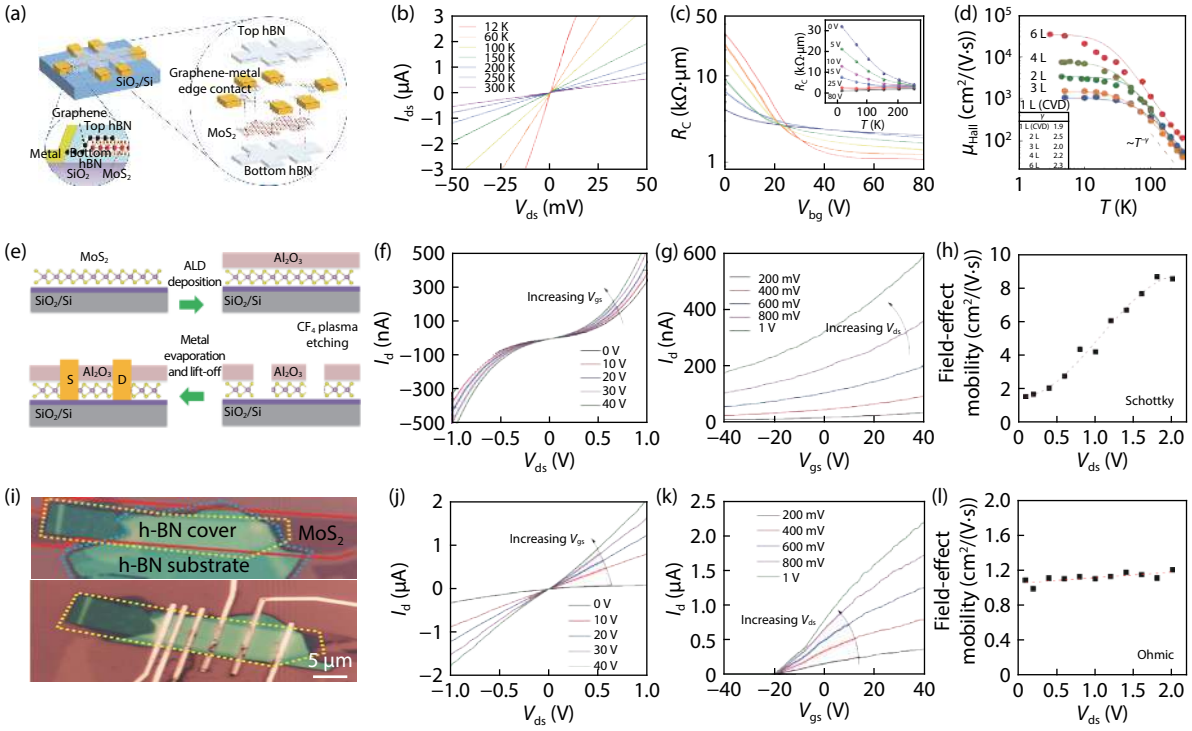

Fig. 8. (Color online) Edge contact investigation of MoS_2 device. (a) Schematic diagram of hBN encapsulated MoS_2 device with graphene edge contact. (b–d) Temperature dependent output curves, contact resistance and temperature dependent Hall mobility, respectively[66]. Copyright 2016, Nature Publishing Group (e) Schematic of Al_2O_3 capped edge contacted MoS_2 device. (f–h) Output curves, transfer characteristic and mobility with different drain voltage for Al_2O_3 capped MoS_2 device. (i) Schematic of h-BN capped edge contacted MoS_2 device. (j–l) Output curves, transfer characteristic and mobility with different drain voltage for hBN capped MoS_2 device[67]. Copyright 2016, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

metallic materials on SCs to form van der Waals contact is also an attractive way to eliminate Fermi level pinning effect and decrease the contact resistance. Furthermore, 2D metallic-SCs heterostructures have wide potential in future applications, such as high-performance transistors[25, 28], phototransistors[32, 38] and so on. In this part, we will discuss CVD growth of 2D metallic materials as contact, phase engineering of 2D SCs to metallic phase as contact, and intercalation method to induce 2D SCs into metallic state as contact. For the 2D top contact, the 2D metallic materials can be regarded as a protection and buffer layer. In the case of CVD growth 2D metallic materials as top contact, the out-of-plane van der Waals bonding will be formed between 2D SCs and metallic materials. The surface of 2D SCs will not be damaged by the deposited metal. A van der Waals type contact will facilitate the carrier injection across the interface, which was also demonstrated by In/Au contacted 2D SCs, as we discussed previously in Section 4.1.2. In addition, Fermi level pinning effect can be avoided and then the contact resistance can be reduced by such contact. However, compared to the 2D edge contact with metallic materials grown by CVD, there is a larger tunnel barrier in 2D top contact because of the van der Waals contact mode. Higher carrier injection efficiency can be achieved by in-plane covalent bonding between 2D SCs and metallic materials owing to the smaller tunnel barrier widths in a 2D edge contact.

Besides CVD growth method, phase engineering and intercalation can also introduce 2D metal–SCs in-plane heterostructure. The metallic state can be realized by point defects through laser or Ar plasma treatment, or introducing interlayer metal atoms through intercalation approaches, which is similar to the heavy doping technology in Si-based CMOS circuits. Therefore, this type of 2D SCs FET can be regarded as a simplified conventional Si-based NMOS FET. The difference is that doping technology in Si-based CMOS circuits is controllable and sustainable, while doping strategies for 2D SCs FET can only be applied to certain 2D SCs.

4.2.1. CVD growth 2D metallic materials as contact

The CVD method can produce many kinds of 2D metallic-SCs heterostructures with high yield, including the stacking orientation controlled vertical and seamless lateral 2D metallic-SCs heterostructures[71–75]. Therefore, CVD is regarded as one of the most promising methods to build 2D integrated circuits for future applications. To take one example, uses CVD growth 2D metallic materials as contact to decrease the contact resistance and enhance the performance of 2D SCs FET.

Recently, Lee *et al.* and Duan *et al.* achieved heteroepitaxial stacking of van der Waals monolayer 1T metallic-2H SC WSe_2 heterostructures, in which a distinctively low contact barrier was achieved across a clean epitaxial van der Waals gap[76, 77]. Fig. 9(a) shows a schematic illustration of a two-step CVD method growing metallic WTe_2-SC WSe_2 heterostructure, where the monolayer WSe_2 was synthesized first followed by the growth of metallic WTe_2. Fig. 9(b) shows the illustration of device schemes of WTe_2 (FET-1) and Ti/Au (FET-2) contact. The output current of WTe_2 contact WSe_2 FET is much larger than its counterpart from Ti/Au contact (Fig. 9(c)), which indicates high carrier injection efficiency with WTe_2 contact. The temperature-dependent sheet conduc-

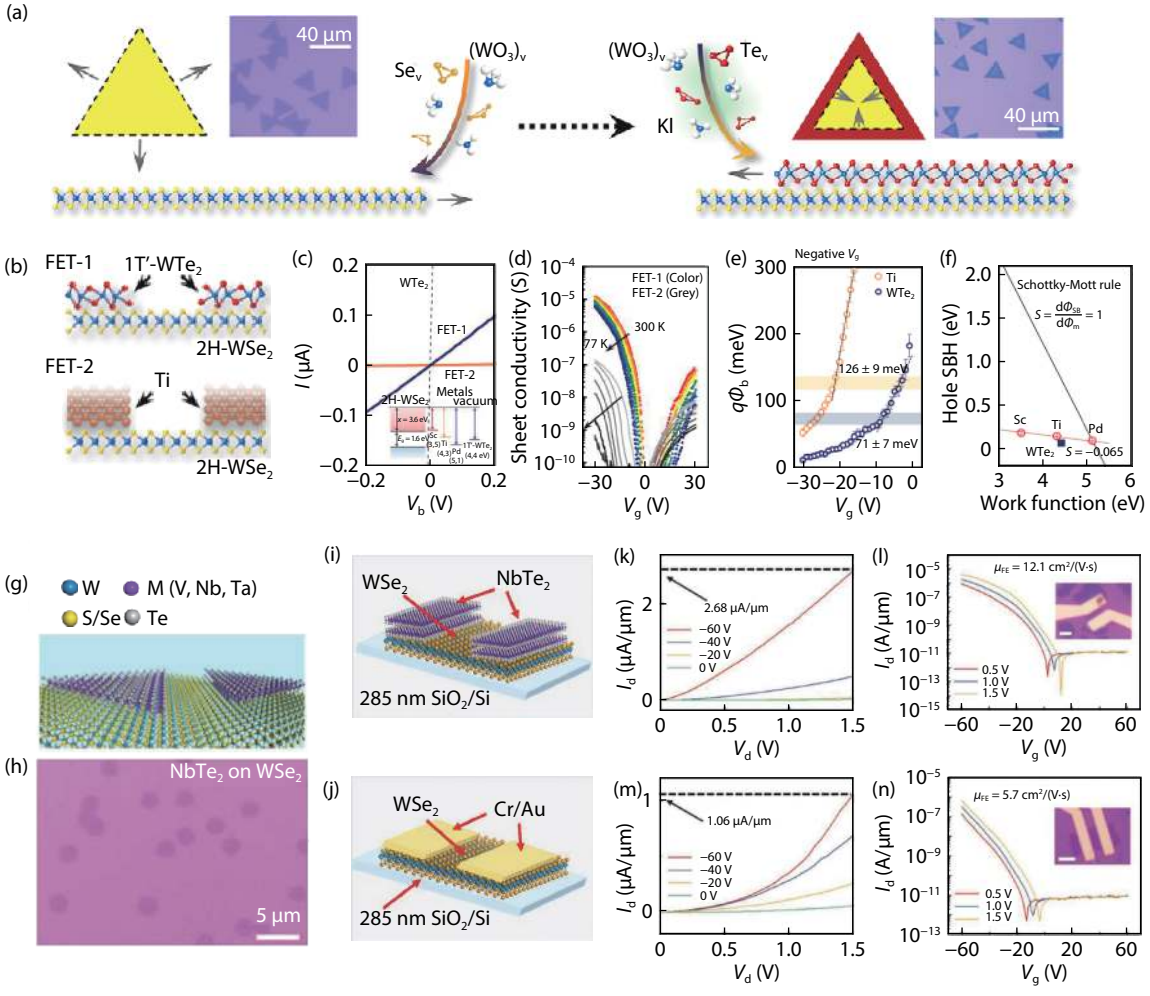

Fig. 9. (Color online) Contact engineering of vertical 2D metallic-2H WSe_2 heterostructure. (a) Sequential growth scheme of vertical WSe_2 and WT_2 heterostructure. The inset is the optical images of WSe_2 and WTe_2. (b) Device mode of WSe_2 with and without contact. (c, d) Output curves and temperature-dependent conductivity of WSe_2 device with WTe_2 and Ti contact. (e) Built-in potential energy versus back-gated voltage for Ti and WTe_2 contacted WSe_2 devices. (f) $Φ_{SB}$ height with the function of metal work function[76]. Copyright 2013, American Chemical Society. (g, h) Atomic structure of van der Waals epitaxy growth of 2D metallic-SCs heterostructure and optical image of $NbTe_2$-WSe_2 heterostructure. (i, j) Schematic model of WSe_2 device with $NbTe_2$ and Ti contact. (k–n) Current–voltage and transfer characteristics of WSe_2 device with and without $NbTe_2$ contact. The inset is optical images of fabricated devices[77]. Copyright 2019, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

tivity ($σ$) versus bake gate voltage (V_g) curves are shown in Fig. 9(d). The current on–off ratio of WTe_2 contact device is about 10^7, which is larger than that from Ti/Au contact WSe_2 FET (~ 10^5). In addition, the maximal hole mobility is about 20 cm^2/(V·s) for WTe_2 contact device, which is at least ten times higher than that of Ti/Au contact. Using thermionic emission model, $Φ_{SB}$ height extracted from Fig. 9(e) for WTe_2 contact device is about 70 meV while the $Φ_{SB}$ height is about 126 meV from Ti/Au contact. The reduced $Φ_{SB}$ demonstrates that the Fermi level pinning effect can be eliminated by the 2D metallic contact. The parameters of interface S is about 0.065 and 1 from the curves slope in Fig. 9(f). The performance of WSe_2 FET also can be improved by 1T metallic $NbTe_2$ contact, where the atomic structure, optical image of heterostructure and device models are shown in Figs. 9(g)–9(j). The on-state current is 2.68 $μ$A/$μ$m at V_{ds} = 1.5 V for $NbTe_2$ contacted WSe_2 FET, which is twice over the one in Cr/Au contact device (Figs. 9(k) and 9(m)). Correspondingly, the hole mobility of $NbTe_2$ contact device is at least two times higher than that for Cr/Au contact, as seen in Figs. 9(l) and 9(n). The performance improvement can be attributed to the unbroken surface of the WSe_2, where the Fermi level pinning effect at the interface is avoided.

Lateral 2D metallic-SCs heterostructures are also utilized to fabricate device with 2D metallic material contact. Figs. 10(a) and 10(e) show a schematic model of lateral graphene–MoS_2 heterostructures[91, 92]. A device model of lateral VS_2–MoS_2 heterostructures[75] is presented in Fig. 10(i). As the MoS_2 FET contacted with metallic graphene or VS_2, the mobility can be improved substantially when compared to the traditional metal contact. The electrical characterizations of graphene contacted MoS_2 FET are shown in Figs. 10(b)–10(d) and Figs. 10(f)–10(h). As reported by Zhang *et al.*, current on–off ratio of 10^7 and maximum field effect mobility of 24 cm^2/(V·s) was obtained, which is much higher than its counterparts from Au contact. A similar improvement is also achieved by Hong *et al.* in graphene contacted MoS_2 device, in which a high on–off ratio of about 10^9 and maximum field effect mobility of 8.5 cm^2/(V·s) were presented. Figs. 10(j)–10(l) show the output characteristics, $Φ_{SB}$ and contact resist-

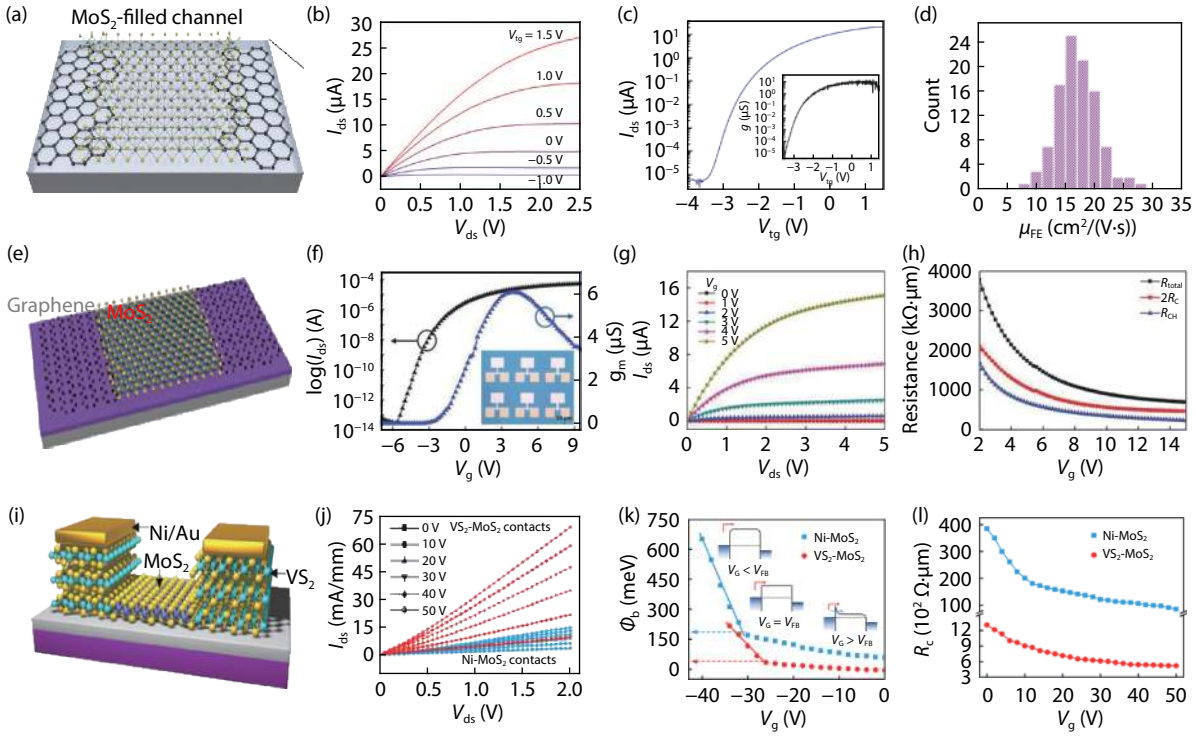

Fig. 10. (Color online) Contact engineering of lateral graphene–MoS_2 and VS_2–MoS_2 heterostructures. (a) Schematic diagram of MoS_2–graphene lateral heterostructure. (b, c) Transfer and output curves of graphene contacted MoS_2 device. (d) Statistics of obtained mobility from graphene contacted MoS_2 device[91]. Copyright 2016, Nature Publishing Group. (e) Schematic fabrication of the MoS_2–graphene lateral heterostructure. (f, g) Representative transfer and output curves of graphene contacted MoS_2 deice. (h) Total, contact and channel resistance of graphene contacted MoS_2 device[92]. Copyright 2016, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (i) Device schematic of VS_2 contacted MoS_2. (j) I_{ds}– V_{ds} curves of MoS_2 device with VS_2 and Ni contact. (k) Extracted Φ_{SB} of VS_2 and Ni contacted MoS_2 as a function of V_{bg}. (l) Contact resistance of Ni and VS_2 contacted MoS_2 devices[75]. Copyright 2018, American Chemical Society.

ances with different back gate voltage, respectively. The output current from the VS_2 contacted device is about six times higher than that from the Ni-contacted counterpart. As expected, the mobility was improved from 5.5 $cm^2/(V·s)$ for Ni/Au contact device to 35 $cm^2/(V·s)$ for VS_2 contacted device. The enhanced mobilities of the device can be attributed to the reduced Φ_{SB} and contact resistance[93–96]. As shown in Figs. 10(k) and 10(l), the Φ_{SB} is as small as 30 meV, getting one of the lowest Φ_{SB} in the previous reports, which is far less than that from Ni/Au contact (Φ_{SB} = 163 meV). The contact resistance in VS_2 contacted MoS_2 device is 520 Ω·μm at V_g = 50 V, which is ten times smaller than that of Ni–MoS_2 contacts (8640 Ω·μm).

4.2.2. Phase engineering 2D semiconductor into metallic phase

Compared to CVD grown 2D metallic-SCs heterostructures, the phase engineering method is more specific. On the one hand, it can only be applied to 2D SCs that have two or more stable or metastable phases; while on the other hand, the phase transition region can be patterned selectively. For example, the stable phase on MoS_2 is trigonal prismatic (H) coordination and a semiconductor while the MoS_2 with octahedral (T) coordination is a metastable phase with metallic nature[53, 96, 97]. The achieved metallic T phase can be worked as atomically seamless ohmic contact for 2D SCs device.

Electron donation induced phase transition—such as n-butyl lithium treatment[80], chalcogen vacancies induced by laser irradiation[80] or by Ar plasma treatment[81]—is one of the most widely used phase engineering methods to transform 2D SCs into metallic state. During these processes, the exposed area can be converted to metallic 1T phase while the covered region remains 2H SC phase. Fig. 11(a) shows an electrostatic force microscopy phase image of monolayer MoS_2 treated by n-butyl lithium, where the exposed regions are converted to 1T metallic phase while the protected regions remain 2H SC phase, forming a 1T–2H–1T lateral heterostructure. Figs. 11(b)–11(d) present the device performance of 1T metallic MoS_2 contacted 2H MoS_2 device. Compared to Au contacted MoS_2 device, the contact resistance reduced from 1.1 to 200 kΩ·μm and its ohmic contact was achieved by 1T MoS_2 contacted. In addition, the mobility was improved from 19 to 46 $cm^2/(V·s)$ and the subthreshold swing values of 1T-MoS_2 contacted FETs are much smaller than that of Au contacted. Similarly, through laser-irradiation, the mobility of 1T′ $MoTe_2$ contacted 2H channel $MoTe_2$ device was improved from about 1 to 50 $cm^2/(V·s)$ (Fig. 11(h)) and the Φ_{SB} was reduced from 200 to 10 meV compared to the counterpart of metal contacted 2H $MoTe_2$ device. A schematic illustration and the transistor model are shown in Figs. 11(e) and 11(f). Furthermore, Ar plasma induced 2H–1T phase transition of MoS_2 also reported by Zhu *et al.* A schematic diagram of plasma-treated process is shown in Fig. 11(i). The schematic modes of three types of devices are shown in Fig. 11(j) and the output and transfer characteristics of back gated monolayer MoS_2 device are shown in Figs. 11(k) and 11(l). Although the contact is a mixture of 2H and 1T phase, the contact resist-

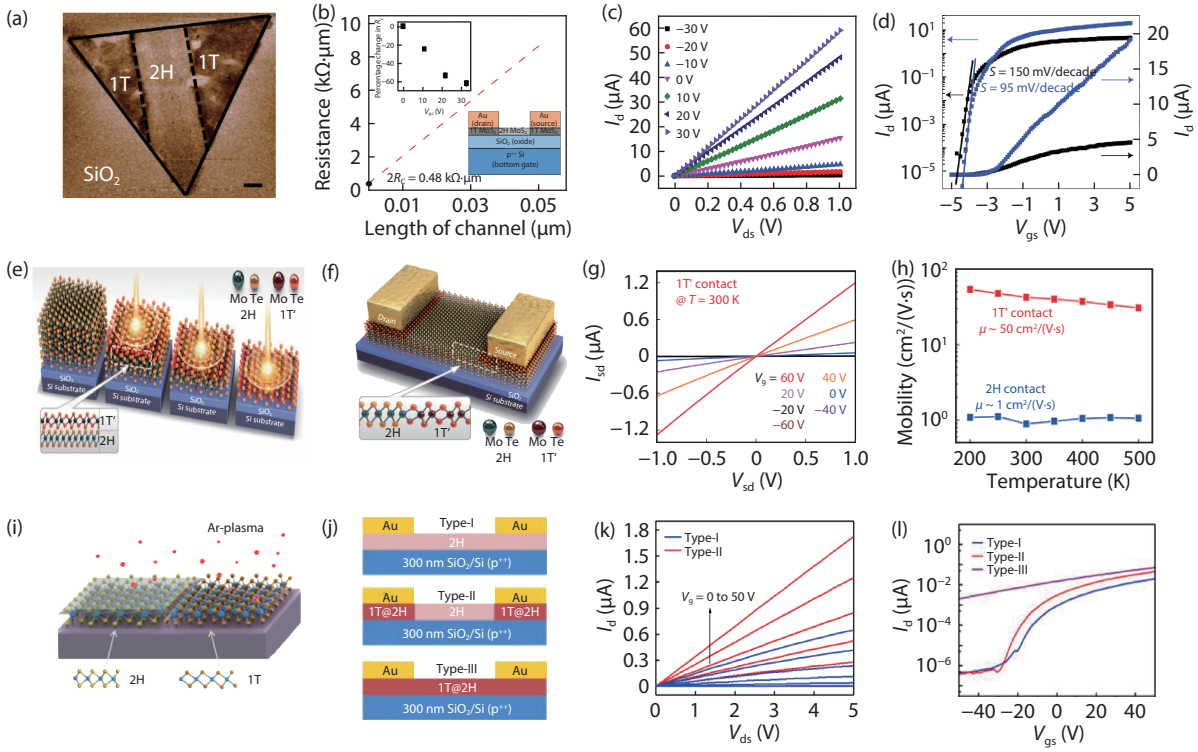

Fig. 11. (Color online) Electron donation, laser or Ar plasma induced metallic phase as contact. (a) Electrostatic force microscopy phase image of 1T–2H–1T lateral MoS_2 heterostructure. (b–d) Resistance, output and transfer curves of 2H phase MoS_2 with metallic 1T phase MoS_2 contact. The inset is the device model of MoS_2 device with Au and 1T metallic MoS_2 contact[80]. Copyright 2014, Nature Publishing Group. Laser induced phase transition of metallic 1T′-$MoTe_2$. (e) Atomic structure and laser treated process. (f) Device schematic with metallic 1T′-$MoTe_2$ contact. (g) Output characteristic of $MoTe_2$ device with 1T′-$MoTe_2$ contact. (h) Field-effect mobility as a function of temperature of $MoTe_2$ device with Au and metallic $MoTe_2$ contact$_2$ contact[80]. Copyright 2015, American Association for the Advancement of Science (AAAS). (i) Atomic structure and schematic representation of plasma-treated process. (j) Device models with Au or 1T/2H phase MoS_2 contact. (k, l) Output and transfer curves with different Au and 1T/2H phase MoS_2 contact[81]. Copyright 2017, American Chemical Society.

ance can still be reduced, which was demonstrated by the increased output current in Fig. 11(k).

4.2.3. Intercalation induced metallic state

Intercalation is a convenient and promising method to tune the properties of van der Waals materials[82]. Figs. 12(a) and 12(b) show the schematics of the atomic structure of bilayer pristine SnS_2 with a van der Waals gap and Co, Cu intercalated SnS_2, respectively. The n-type SnS_2 was converted to p-type semiconductor and a highly conductive metal by Cu and Co intercalation, respectively. Figs. 12(c)–12(f) show optical images of CVD-grown SnS_2, Cu–SnS_2, Co–SnS_2 and spatially controlled intercalation of SnS_2, respectively, where the morphologies stay the same after intercalation while the colors of Cu–SnS_2 and Co–SnS_2 become more opaque and turn dark blue and violet-red. Temperature-dependent resistance measurement was performed to verify the electrical characteristic of intercalated SnS_2 (Fig. 12(g)). One can see that the resistance of Co–SnS_2 is almost independent of temperature and gives a metallic behavior, while Cu–SnS_2 presents typical semiconducting behavior. Fig. 12(h) shows the typical transfer curve of Cu–SnS_2 FET, showing the p-type behavior. To verify whether the performance of metallic Co–SnS_2 contacted device can be improved, Co–SnS_2 contacted SnS_2, Cu–SnS_2 and p–n junction FETs are fabricated. The output curves are shown in Figs. 12(i) and 12(j), respectively. It can be seen that the current of all of the Co–SnS_2 contacted devices is improved compared to the Ti/Au contacted SnS_2 FET, which indicates the good contact quality formed by metallic Co–SnS_2.

5. Summary and outlook

In summary, in this review we have discussed the fundamental aspects related to contacts of 2D materials devices, including contact geometry and Schottky barrier. We also presented the progress of contact engineering strategies to improve the contact quality. In the conventional metal contact part, we show that the performance of 2D SCs FET can be improved by the right choice of top contact metal. However, the Fermi level pinning effect at the interface cannot be avoided, resulting in Schottky contact between top metal and 2D SCs. Fortunately, an ohmic contact can be realized and the Fermi level pinning effect can be eliminated by van-der-Waals-type bonding or gap through introduction of an In interlayer or metal electrode transfer method. A 3D edge contact was also emphasized and developed because it is advantageous over 3D top contact in terms of carrier injection efficiency, even if the pure edge contact technology is in the initial stage. However, the fabrication process of these 3D top contact or edge contact method is still complicated and faces the difficulties of scalable production.

Compared to traditional metal contact, a van-der-Waals-type metallic contact can easily be achieved by 2D metallic materials grown through CVD method. The performance of 2D SCs FET has improved substantially owing to the elimination of Fermi level pinning effect and reduction of Φ_{SB} and con-

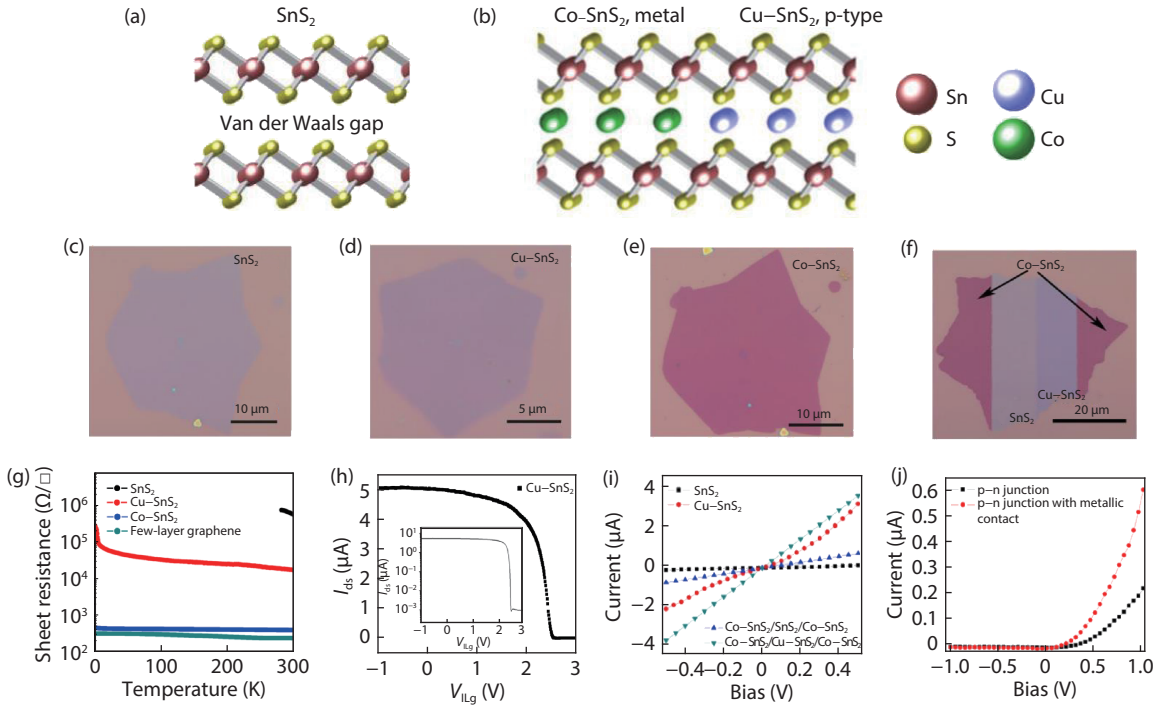

Fig. 12. (Color online) Intercalation induced phase transition of SnS_2. (a) and (b) Atomic structures of pristine SnS_2, Cu and Co intercalated SnS_2. (c–f) Optical images of pure SnS_2, Cu, Co and Cu–Co intercalated SnS_2. (g) Temperature-dependent resistance of SnS_2, Cu–SnS_2, Co–SnS_2 and few layer graphene, where the Cu–SnS_2 presents semiconductor behavior while the Co–SnS_2 behaves as a metal like graphene. (h) Transfer curves of Cu–SnS_2 with p-type characteristic. (i) *I*–*V* curves of Co–SnS_2 contacted SnS_2 and Cu–SnS_2 devices. (j) SnS_2/Cu–SnS_2 junction with and without metallic Co–SnS_2 contact[82]. Copyright 2018, Nature Publishing Group.

tact resistance. But the properties of 2D SCs may be degraded after the growth of 2D metallic materials because the defects and impurities may be introduced in 2D SC's lattice and surface at high temperature. This disadvantage can be avoided by phase engineering or intercalation methods. The phase engineering method is an effective way to achieve ohmic contact for 2D SCs FET. The problem of this method is that the induced T phase is unstable and may return to the H phase as time goes on or at temperatures above 100 °C. In contrast, transition metal intercalation induced metallic state is very stable, which makes it a promising post-growth treatment method to fabricate spatially controlled atomically seamless in-plane 2D metallic-SCs heterostructure. The limitation of the intercalation method is that it cannot be applied to all the 2D materials and the interfaces of the resulted heterostructures have not been well characterized. If the intercalation method can be further developed and applied to those 2D SCs with strong interlayer van der Waals coupling, for example double layer MoS_2 or WS_2, then it will be a tremendous advance and will facilitate the application of this method to 2D SCs based transistors.

Although great progress has been achieved in the field of contact engineering for 2D SCs, there are still some challenges to solve. First, the origin of Fermi level pinning effect is still in debate. Some possible mechanisms, such as charge redistribution induced interface dipoles at interface of metal and 2D SCs or contact metal and chalcogen interaction caused orbital overlap are believed to be responsible for the Fermi level pinning effect[97–100]. Accurate experiments should be developed to analyze the contact interface of metal and 2D SCs, which is important for our understanding of Fermi level pinning effect and Schottky barrier. Therefore, more efforts are needed to uncover and resolve this detrimental effect.

Second, phase engineering or intercalation method induced 2H–1T in-plane heterostructure has previously been reported but, up to now, the barrier at 2H–1T boundary has not been systematically studied. It is necessary to propose a method to predict or calculate the boundary barrier, which will guide us to fabricate high quality heterostructure with ignored tunneling width for carrier injection across the boundary.

Third, it is well known that 2D materials with excellent optical and electrical properties are promising alternatives of Si in future applications in CMOS integrated circuits, and the device dimensions can be further scaled down owing to the atomically thin nature. However, up to now, all the contact engineering strategies reported are limited to a few 2D materials. There are no universal and scalable strategies that can be applied to a highly scaled device in a manufactural way. Before the practical application of contact engineering strategies in modern circuits, wafer scale single crystal with thickness controlled 2D SCs must be made. CVD is one of the most promising methods to get wafer-scale 2D materials, but well crystallinity, repeatability and controllability are still hard to obtain. In addition, an accurate and suitable method should be exploited to precisely control the nucleation position of heterostructures. Very recently, Duan *et al.* provided a general scalable synthesis method to precisely control the nucleation position and growth process of 2D metallic-SCs heterostructures[101]. As shown in Figs. 13(a) and 13(b), periodic defect arrays have been patterned on 2D SCs (MoS_2, WSe_2

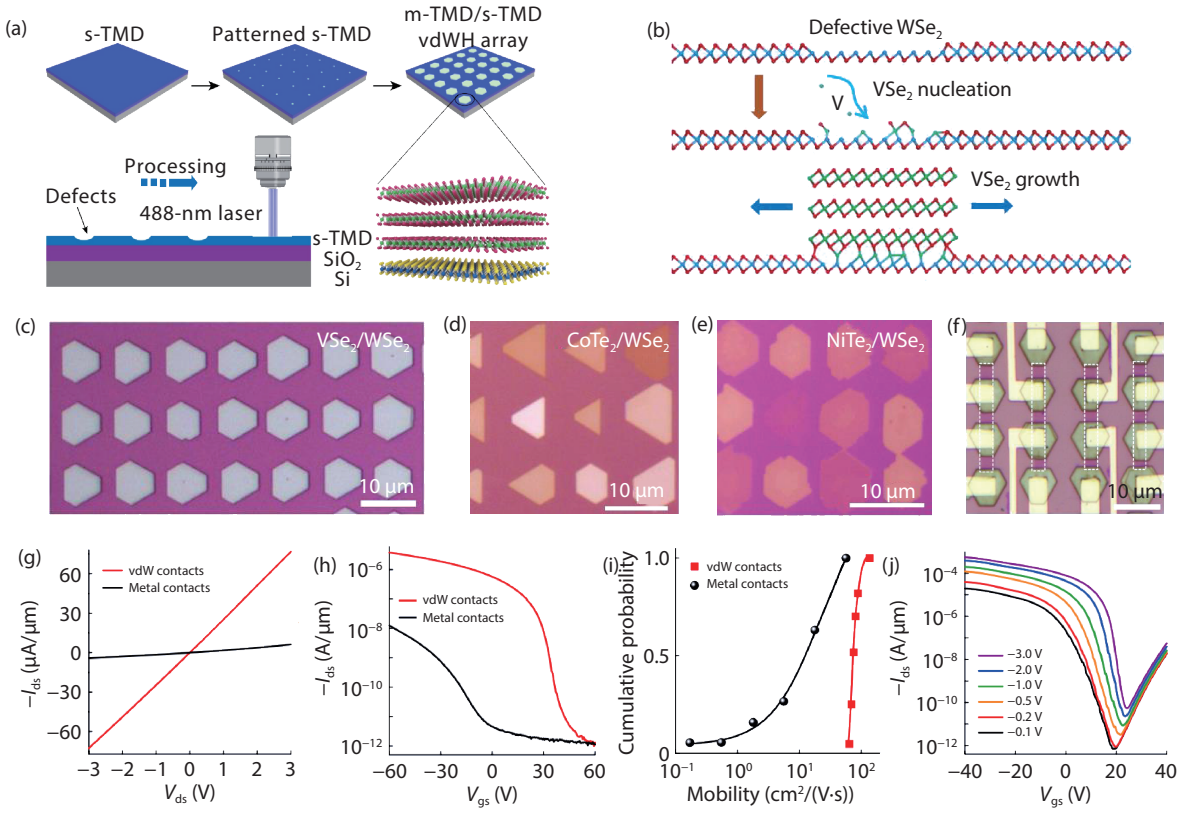

Fig. 13. (Color online) General scalable synthesis of precisely controlled nucleation position and growth process of 2D metallic-SCs heterostructures. (a) Schematic process of selectively patterned periodic defect arrays of 2D SCs (MoS_2, WSe_2 and WS_2) to grow 2D metallic materials (VSe_2, VS_2, $CoTe_2$, $NiTe_2$ and $NbTe_2$). (b) Schematic diagram of VSe_2 growth on patterned sites of WSe_2. (c–e) Optical images of periodical arrays of 2D metallic materials on WSe_2. (f) Optical image of VSe_2 contacted WSe_2 FET periodical arrays. (g–j) Electrical characterizations of the VSe_2 contacted WSe_2 FET[101]. Copyright 2020, Nature Publishing Group.

and WS_2) by 488 nm laser, where the 2D metallic materials (VSe_2, VS_2, $CoTe_2$, $NiTe_2$ and $NbTe_2$) are nucleated at such sites. Figs. 13(c)–13(e) show the optical images of periodic arrays of 2D metallic-WSe_2 heterostructures, where thick 2D metallic materials are grown on the pre-patterned sites periodically. An optical image and the electrical properties of 2D metallic VS_2 contacted WSe_2 FETs are shown in Figs. 13(f)–13(g). It can be seen that the performance of a WSe_2 FET is improved greatly by VSe_2 contact, indicating the feasibility of this scalable method. Finally, other controllable and sustainable contact engineering strategies should be exploited, such as exploiting a general scalable synthesis method to grow atomically thin in-plane 2D metallic-SCs heterostructures, looking for a general phase engineering method, improving the universality of intercalation method or developing transplantable 2D metallic arrays to fabricate 2D metallic-SCs heterostrutures accurately. It should be emphasized that wafer scale single crystal with thickness controlled 2D SCs must be realized before practical application in modern integrated circuits. The application of 2D materials to modern integrated circuits is still in its infancy, therefore it is necessary to develop a reliable, reproducible, and robust method to get 2D integrated circuits in the future.

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