NEWS AND VIEWS

Journal of Semiconductors
(2020) 41, 070402
doi: 10.1088/1674-4926/41/7/070402

Controlling spins in silicon quantum dots

Haiou Li, Xin Zhang, and Guoping Guo†

CAS Key Laboratory of Quantum Information, University of Science and Technology of China, Hefei 230026, China

Citation: H O Li, X Zhang, and G P Guo, Controlling spins in silicon quantum dots[J]. *J. Semicond.*, 2020, 41(7), 070402. http://doi.org/10.1088/1674-4926/41/7/070402

Spins in silicon (Si) quantum dots (QDs), as a new type of solid state qubits, is expected to be a competitive contender in the long run of scalable quantum computation[1]. Quantum computation is believed to be the next-generation computing technology to solve the problems that no classical computer can feasibly tackle. In the last decade, several physical platforms have shown their potential to be the choice for scalable quantum computation, such as superconducting circuits, ion traps, and spins in Si QDs. Among them, the spin in Si QDs is most compatible to modern semiconductor technology, with a promise to scale up to billions of qubits like classical processers that hold jillions of transistors.

Despite its significant impact on classical computation, silicon is still a new material for quantum computation. As early as the beginning of the 21st century, electron spins in gate defined GaAs/AlGaAs QDs were investigated[2]. However, the strong hyperfine interaction in this material impedes the development of a qubit with long coherence time, a time that the spin could preserve its quantum superposition states. In contrast, with existence of an abundant spin-zero isotope, silicon is a 'semiconductor vacuum' in which an electron spin can obtain exceptionally long coherence times, even though there are two main challenges to control spins in silicon: one is the relatively large effective mass of the electron in silicon, and the other is the interaction between spin and valley degree of freedom in Si QDs[3].

The large effective mass requires tighter electron confinement and decreases the transparency of tunnel barriers, and to tackle this problem, researchers suffered a long time and eventually invented the so-called overlapping gate architecture. As shown in Fig. 1(a), on the surface of a Si/SiGe heterostructure or a Si metal–oxide–semiconductor (MOS), metal electrodes are overlapped with one another to define a QD with a diameter ~ 10–20 nm and achieve full control of the electron occupation in the QD. In this way, the QD could be emptied down to single electron. With an external magnetic field, the degeneracy of spin states could be lifted with a Zeeman energy between spin-up and spin-down. Then a qubit can be defined by these two quantum states. By controlling the tunnel rate between the QD and the reservoir or among two QDs, the electron spin direction can be read out using Elzerman readout method or Pauli spin blockade method (see Fig. 1(b)). When a microwave burst with the qubit frequency is applied to one of the electrodes (with natural or synthetic spin-orbit coupling) or to a stripline antenna, the qubit could be driven coherently to oscillate between spin-up and spin-down. Based on Elzerman readout, several research groups have demonstrated single- and two-qubit quantum gate operations with fidelities over 99.9%[4, 5] and 98%[6], respectively; while based on Pauli spin blockade, two groups recently reported high temperature (~1 K) operation of single- and two-qubit gates[7, 8], showing the potential superiority over superconducting qubits that needs the outside temperature to be ~ 10 mK.

Apart from the overlapping gate architecture, there are also some foundry based gate structures that are under development. In 2018, Intel Corporation reported a novel dual nested gate integration process for creating Si QDs based on their fin field-effect transistor (FinFET) technology (see Fig. 1(c)). And in 2019, they demonstrated Coulomb blockade in the QD and tunable tunnel coupling between QDs[9], suggesting this new gate architecture could be used to form spin qubits. In 2020, several groups also reported single-electron control in a two dimensional array of Si QDs (see Fig. 1(d)) that fabricated at CEA_LETI using a technology adapted from a commercial fully-depleted silicon-on-insulator transistor (FD-SOI) technology[10]. These new gate architectures for Si QDs, with the power from industry, may shed light on the realization of large-scale silicon quantum processors.

Although the control fidelity of spin qubits in Si QDs could be very high, the interaction between spin and valley degree of freedom in Si QDs still distracts the researchers' attention. In 2013, Andrew S. Dzurak's group at University of New South Wales first reported spin relaxation "hot spot" in silicon[11], which could make the spin-up state relax to the spin-down state within a time much smaller than 1 ms, limiting the spin readout fidelity. This phenomenon is caused by mixing of spin with valley states (spin-valley mixing), a special state in silicon that could have an energy gap (valley splitting) similar to Zeeman energy. In 2014, L. M. K. Vandersypen's group at Delft University of Technology reported that spin-valley mixing could also impose adverse effect on spin coherence time[12], limiting the improvement of the spin control fidelity. One way to circumvent this problem is to push the unwanted valley states away from the defined qubit space by increasing the valley splitting. This has been investigated in depth, though still limited by the nonuniformity and complex properties of materials. The other way is to investigate the intrinsic properties of spin-valley mixing. In 2020, Guoping Guo's group at University of Science and Technology of China (USTC) found the spin relaxation rate near the "hot spot" could be suppressed by more than two orders of magnitude (see Fig. 2), permitting a relaxation time nearly 100

Correspondence to: G P Guo, gpguo@ustc.edu.cn

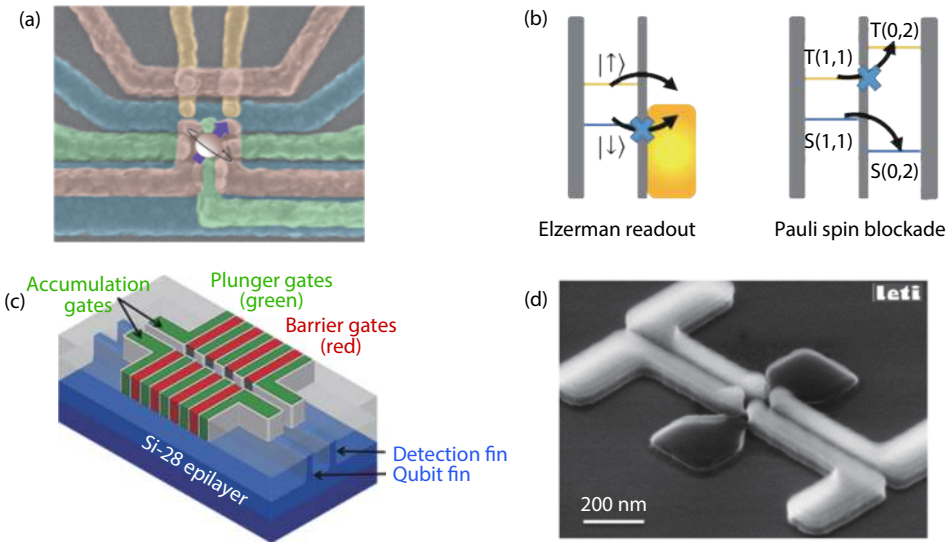

Fig. 1. (Color online) (a) False-color scanning electron microscopy (SEM) image of an overlapping-gate Si QD. (b) Energy level arrangement for Elezerman readout and Pauli spin blockade readout. (c) Dual nested gate integration of Si QDs using fin field-effect transistor (FinFET) technology. (d) SEM image of a two dimensional array of Si QDs using fully-depleted silicon-on-insulator transistor (FD-SOI) technology.

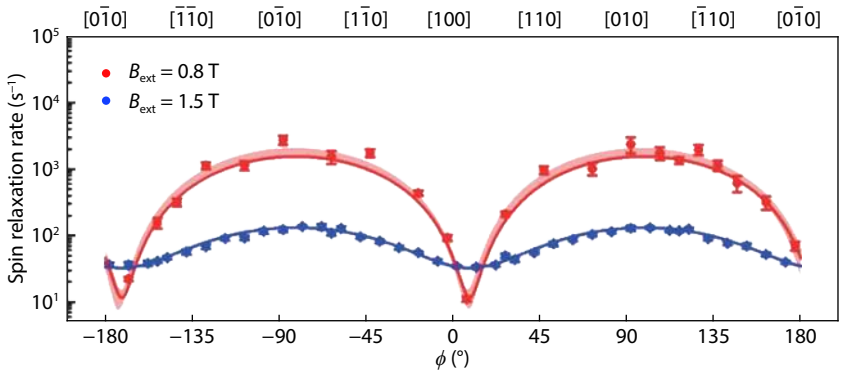

Fig. 2. (Color online) Angle dependence of the relaxation rate measured with different magnetic field strengths.

ms, via rotating the magnetic field direction[13]. This discovery opens up a new way to suppress the adverse effect of spin-valley mixing by controlling the external fields. In the future, extensive studies and better probe methods are still needed to take the understanding of these interactions to a next level, and finally overcome the challenges caused by spin-valley mixing.

In a European quantum technologies roadmap published in 2018[14], they underlined that the next-step goal for spin qubits in silicon contain the "unit cell" demonstration of a scalable 2D spin qubit architecture. Indeed, this is not futureless considering the demonstration of the initial trial of the industry to fabricate scalable Si QDs. Also, in 2020, researchers at Delft University of Technology demonstrated the first silicon based quantum computing platform in the cloud. Although there are only two spin qubits in it, it may be a beginning of the development of large scale spin control in Si QDs. In the next ten years, to achieve this final goal, some stage goals could be demonstrated from easy to difficult. To sum it up, we list them as follows:

1) Control of a linear array of spins with high fidelity single- and two-qubit gates;

2) Readout of a linear array of spins with high fidelity and fast speed for feedback control;

3) Control of a scalable two-dimensional array of spins with high fidelity single- and two-qubit gates;

4) Readout of a scalable two-dimensional array of spins with high fidelity and fast speed for feedback control;

5) Demonstration of error correction code based on an array of spin qubits.

References

[1] Zhang X, Li H O, Cao G, et al. Semiconductor quantum computation. Natl Sci Rev, 2019, 6, 32

[2] Hanson R, Kouwenhoven L P, Petta J R, et al. Spins in few-electron quantum dots. Rev Mod Phys, 2007, 79, 1217

[3] Zwanenburg F A, Dzurak A S, Morello A, et al. Silicon quantum electronics. Rev Mod Phys, 2013, 85, 961

[4] Yoneda J, Takeda K, Otsuka T, et al. A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%. Nat Nanotechnol, 2018, 13, 102

[5] Yang C H, Chan K W, Harper R, et al. Silicon qubit fidelities approaching incoherent noise limits via pulse engineering. Nat Electron, 2019, 2, 151

[6] Huang W, Yang C H, Chan K W, et al. Fidelity benchmarks for two-qubit gates in silicon. Nature, 2019, 569, 532

[7] Yang C H, Leon R C C, Hwang J C C, et al. Operation of a silicon quantum processor unit cell above one kelvin. Nature, 2020, 580,

350

[8] Petit L, Eenink H G J, Russ M, et al. Universal quantum logic in hot silicon qubits. Nature, 2020, 580, 355

[9] Pillarisetty R, George H C, Watson T F, et al. High volume electrical characterization of semiconductor qubits. 2019 IEEE International Electron Devices Meeting (IEDM), 2019, 31.5.1

[10] de Franceschi S, Hutin L, Maurand R, et al. SOI technology for quantum information processing. 2016 IEEE International Electron Devices Meeting (IEDM), 2016, 13.4.1

[11] Yang C H, Rossi A, Ruskov R, et al. Spin-valley lifetimes in a silicon quantum dot with tunable valley splitting. Nat Commun, 2013, 4, 2069

[12] Kawakami E, Scarlino P, Ward D R, et al. Electrical control of a long-lived spin qubit in a Si/SiGe quantum dot. Nat Nanotechnol, 2014, 9, 666

[13] Zhang X, Hu R Z, Li H O, et al. Giant anisotropy of spin relaxation and spin-valley mixing in a silicon quantum dot. Phys Rev Lett, 2020, 124, 257701

[14] Acín A, Bloch I, Buhrman H, et al. The quantum technologies roadmap: A European community view. New J Phys, 2018, 20, 080201