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Low on-resistance 1.2 kV 4H-SiC power MOSFET with $R_{on, sp}$ of 3.4 mΩ·cm^2

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Abstract: A 4H-SiC power MOSFET with specific on-resistance of 3.4 mΩ·cm^2 and breakdown voltage exceeding 1.5 kV is designed and fabricated. Numerical simulations are carried out to optimize the electric field strength in gate oxide and at the surface of the semiconductor material in the edge termination region. Additional n-type implantation in JFET region is implemented to reduce the specific on-resistance. The typical leakage current is less than 1 μA at V_{DS} = 1.4 kV. Drain–source current reaches 50 A at V_{DS} = 0.75 V and V_{GS} = 20 V corresponding to an on-resistance of 15 mΩ. The typical gate threshold voltage is 2.6 V.

Key words: 4H-SiC; electric field strength; floating guard ring; specific on-resistance

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1. Introduction

SiC MOSFETs have achieved great improvements, both in device design and material fabrication technology[1–5]. Most leading semiconductor companies are working to commercialize SiC MOSFETs. The major designs of SiC MOSFETs typically follow the 'VDMOS' structure for CREE, ST and 'UMOS' structure for ROHM and Infineon. The former is also called a planar MOSFET and the latter is known as a trench MOSFET. Devices of extremely low on-resistance and medium voltage rating (1200 V / 25 mΩ: C2M0025120D, 900 V / 10 mΩ: CPM3-0900-0010A) are commercially distributed from CREE[6, 7]. Meanwhile, devices from ROHM and Infineon both exhibit high gate threshold voltages, making the design of the control system more compatible with that of Si counterparts[8, 9]. However, increasing the voltage rating to some extent goes against decreasing on-resistance, and vice versa. Developing devices with both low on-resistance and medium-to-high voltage rating is of great significance and interest. As reported, on-resistance is mainly limited by the low inversion layer mobility (μ_{FE}), which is typically a few tens, much less than the body electron mobility (about 1000 cm^2·V^{-1}·s^{-1})[2, 10, 11]. Very high state density (D_{it}) at the SiC/SiO$_2$ interface is thought to heavily restrict the channel mobility[12]. Nitric oxide (NO) annealing after oxidation effectively lowered D_{it}, thus raising the channelmobility to 20–30 cm^2·V^{-1}·s^{-1}[13]. Several methods have been shown that they can increase μ_{FE} evidently, such as introducing boron or phosphorus atoms into the gate oxide layer and depositing a thin metallic layer before oxidation[14–17]. However, they can only be utilized in industrial manufacture provided long time reliability. Therefore, post-oxidation annealing in NO ambient is still the major adopted process. The process that we employed in manufacturing shows no obvious disadvantage than other manufacturers. Thus, optimizing the epi-layer parameters, cell pitch geometry and doping parameters are regarded as practical methods to enhance the current capability.

In our previous work, we (i.e. Huang) developed a 1200 V / 40 mΩ MOSFET[18]. The resistance of JFET region still limits the total specific on-resistance ($R_{on, sp}$). In addition, the area of ohmic contact and gate-to-source gap can be reduced due to the improvement of fabrication recipe. In this paper, we have reduced the on-resistance by additional n-type doping in JFET region, reducing the cell pitch and optimizing the drift layer parameters. According to the simulation results, the electric field strength in JFET region changes with the doping concentration. We have optimized the JFET width to keep the electric field strength under a safe value and we have simultaneously acquired a decreased JFET resistance. Finally, we have achieved a specific on-resistance of about 3.4 mΩ·cm^2, reduced 47% compared with former work. Consequently, we have designed and fabricated SiC MOSFETs with on-resistance of 15 mΩ which is a considerable low value in the voltage rating of 1.2 kV.

2. Design and simulation

Our simulated models and simulation results will be discussed in this section, including epi-layer parameters, floating guard ring (FGR) type edge termination, cell pitch geometry and JFET region.

2.1. Determination of epi-layer parameters

The target voltage rating is mainly supported by the thickness and doping concentration of the epi-layer, which shall be taken into consideration at the beginning of device design. A planar junction with the same doping depth as the P-well is modeled and simulated by SILVACO ATLAS TCAD. Fig. 1 shows the theoretical breakdown voltages (BV) of modeled planar junction structures. The thickness of epi-layer varies from 8 to 12 μm, and the n-type doping concentration varies from 6 × 10^{15} to 1.4 × 10^{16} cm^{-3}. The BV increases

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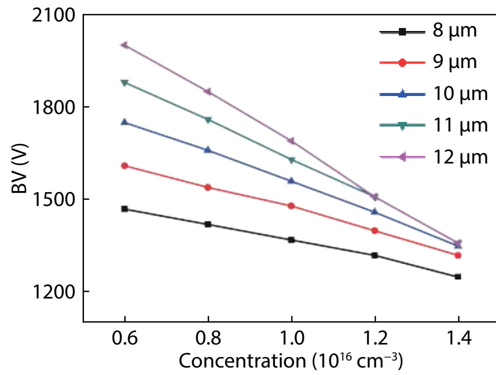

Fig. 1. (Color online) Theoretical breakdown voltages of epi-layers with various thickness and doping concentration.

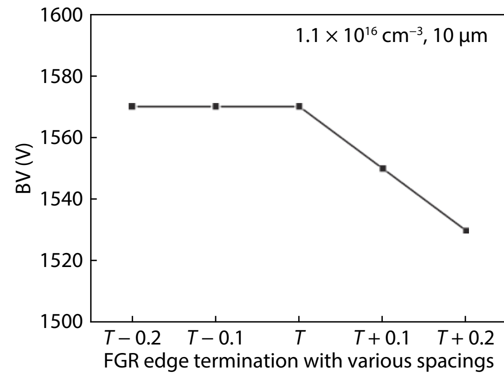

Fig. 3. Breakdown voltages of FGR with different spacing arrays.

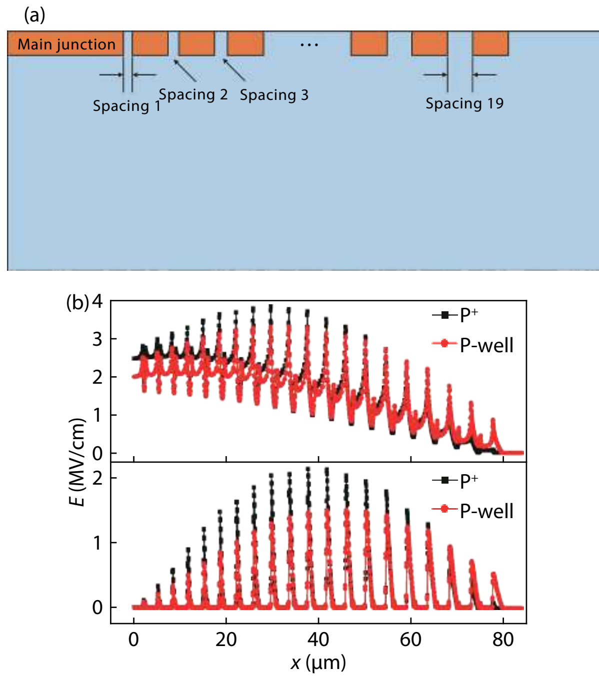

Fig. 2. (Color online) (a) Modeled FGR type edge termination structure. (b) E-field strength profiles comparison between P-well doped and P$^+$ doped FGR type edge termination. Both data are extracted under breakdown statuses of the two terminations, respectively. Upper one corresponds to E-field at the depth of p–n junction and bottom one corresponds to E-field near the surface of the edge termination.

while adding the thickness and decreasing the doping concentration of epi-layer. Because we aim to design a device with a voltage rating of 1.2 kV, the preferred BV should not be less than 1.5 kV. Following the simulation results, we choose a thickness of 10 μm and n-type doping concentration of 1.1×10^{16} cm^{-3} as parameters of the device drift epi-layer, corresponding to a BV of 1510 V. Compared with former results from Huang, the optimization of epi-layer results in specific on-resistance decreasing by about 0.4 mΩ·cm^2.

2.2. Design of float guard ring (FGR) type edge termination

FGR type edge termination is selected thanks to its convenient fabrication process. An FGR with doping profile same with P-well is simulated. Fig. 2(a) shows an edge termination containing 19 rings with 2.5 μm width and first ring spacing of 0.8 μm. The following spacing between nearby rings increases gradually to 2.4 μm. Compared with P$^+$ doped FGR edge termination, the P-well doped FGR edge termination has a lower maximum electric field (E-field) strength at the depth of p–n junction under breakdown states, as can be seen in Fig. 2(b). P-well and P$^+$ doping was modeled with a junction depth of about 0.8 and 0.6 μm, respectively. P-well doping has a retrograde profile and P$^+$ doping has a box-type profile with maximal doping concentration over 1×10^{20} cm^{-3}. The E-field strength near the semiconductor surface is lower for P-well doped termination compared with that of P$^+$ doped termination, and also under each one's breakdown status. The lower electric field strength near the semiconductor surface indicates a lower drain-source leakage current and a better stability. We furtherly simulate P-well doped FGR edge termination with various ring spacing arrays. The baseline FGR is labeled as 'T', while 'T + 0.1' refers to add 0.1 μm to all numbers in array 'T'. 'T + 0.2', 'T – 0.1', and 'T – 0.2' are named in the same way. BVs of all FGR edge terminations are presented in Fig. 3. All BVs exceed 1.5 kV and 'T – 0.1' is desirable for the sake of stability during manufacture.

2.3. Optimizing the cell pitch

To increase the current density, we constrict the width of P-well implanted region from 9 to 7 μm. The specific on-resistance is reduced by about 1.0 mΩ·cm^2 while the JFET region is unchanged.

2.4. Optimization of electric field strength in gate oxide with additional n-type doping in JFET region

To design a planar type MOSFET, the JFET region is of great concern because of its considerable contribution to the total conducting resistance for MOSFETs with low-to-medium voltage ratings. To reduce the JFET region resistance, additional n-type doping is introduced. Fig. 4(a) shows the specific on-resistance of SiC MOSFET with and without n-type doping in JFET region. Without JFET doping (baseline), the on-resistance increases dramatically when constricting the JFET width. With additional n-type doping, the total doping concentration reaches 1×10^{17} cm^{-3} in the JFET region and the specific on-resistance obviously reduces. When choosing the JFET width, the electric field strength near the surface of JFET region is of great concern. When applying a proper V_{DS} (turn off state) along the surface of JFET region, the electric field strength reaches its maximum at the middle point. The maximum value increases when increasing JFET width. Stronger field in JFET region results in a stronger field in gate oxide. We seek to keep the maximum value of E-field in gate oxide

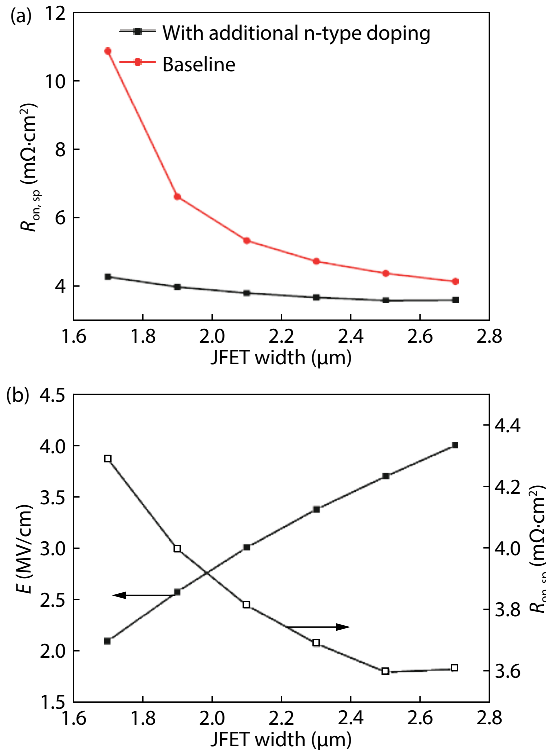

Fig. 4. (Color online) (a) Specific on-resistance with and without additional JFET doping. (b) Electric field strength in gate oxide and specific on-resistance dependence on JFET width.

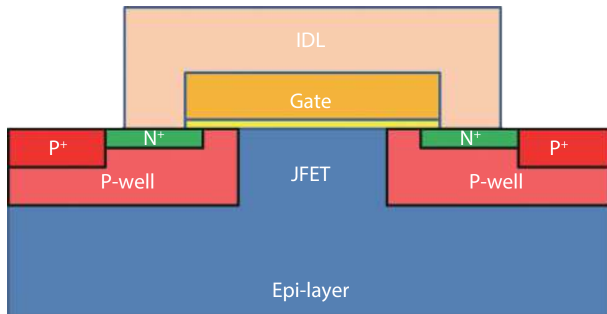

Fig. 5. (Color online) Doping regions of designed SiC MOSFET including P-well, N+, P+, and JFET regions.

(E_{max}) below 4 MV/cm. Consequently, we simulate the electric field strength in gate oxide with JFET doping, the results can be seen in Fig. 4(b). A 2.6 μm JFET region is satisfied, at which the specific on-resistance is reduced by about 28% with JFET doping. If E_{max} is maintained under 3 MV/cm as usual (corresponds to 2.1 μm JFET), then the corresponding specific on-resistance will decrease by about 25% with JFET doping. For better reliability of the gate oxide, we choose to use 2.1 μm JFET in our design.

3. Fabrication

A 10 μm epi-layer with n-type doping concentration of 1.1×10^{16} cm^{-3} was grown on the 'Si face' of a heavily doped n-type 4H-SiC substrate, which was cut with an offset angle of 4 degrees. Doping regions are shown in Fig. 5 including P-well regions, N+ source regions, P+ regions, and JFET doping region.

P-well doping with retrograde profile was first achieved by several aluminum implantations. A heavily nitrogen doped region with box profile formed N+ source. The MOS channel was acquired by the self-alignment method, with a length of 0.7 μm. P+ regions were achieved by heavy dose aluminum doping. To reduce the resistance of the JFET region, additional low dose nitrogen doping was implemented. Doping of FGR type edge termination was realized at the same time with P-well process. After all of the doping processes, dopants were activated at 1870 K. Then, gate oxide layer (55 nm) was thermally grown at 1520 K in dry O_2 ambient followed by an annealing process in NO ambient, also at 1520 K. Degenerated doped polysilicon layer (500 nm) was deposited and etched into the gate structure. Ohmic contact between nickel and N+ source/P+ region was formed by annealing at 1170 K in vacuum. Intermediate dielectric layer was deposited and via holes were opened soon after. Finally, thick metal layers were evaporated as electrodes at both sides of the wafer. The final wafer is shown in Fig. 6 and the target device is 5.2 × 5.5 mm² with an active region area of 22.5 mm².

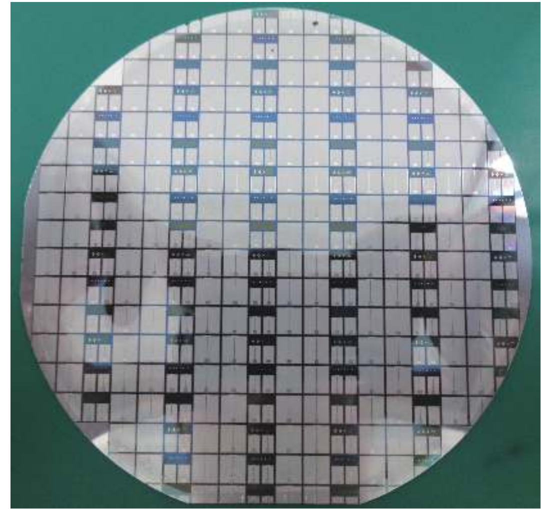

Fig. 6. (Color online) Photo of fabricated 1.2 kV / 15 mΩ devices.

A boron doped polysilicon gate was used instead of a phosphorus doped gate to obtain a higher gate threshold voltage.

4. Results and discussion

First, we verify the protection efficiency of FGR type edge termination with P-well doping. The breakdown voltages of PiN diodes are shown in Fig. 7. The designed edge termination structure has a breakdown voltage that is higher than 1550 V.

Gate threshold voltage (V_{GS}) is measured by applying $V_{GS} = V_{DS}$ at which I_D = 15 mA, which exhibits a typical value around 2.6 V, increasing by 0.5 V compared with phosphorus doped polysilicon gate. The pulsed current–voltage (I–V) curves under various gate voltages are shown in Fig. 8. This MOSFET conducts 50 A current at V_{DS} = 0.75 V and V_{GS} = 20 V, corresponding to an on-resistance of 15 mΩ and specific on-resistance of 3.4 mΩ·cm².

The drain–source leakage current is measured by applying a step-by-step voltage to drain the electrode, while keeping source and gate electrodes shorted to ground. The leakage current is less than 1 μA at V_{DS} = 1.4 kV, indicating a good turn off state, as shown in Fig. 9. The dashed-red line rep-

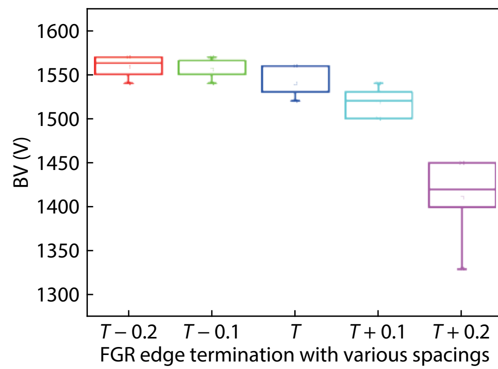

Fig. 7. (Color online) Breakdown voltages of PiN diodes with different FGR spacing arrays.

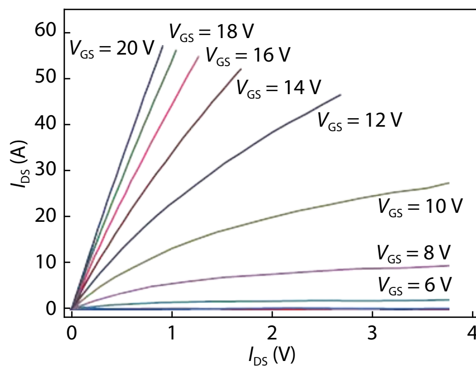

Fig. 8. (Color online) Current–voltage curves of various gate voltages.

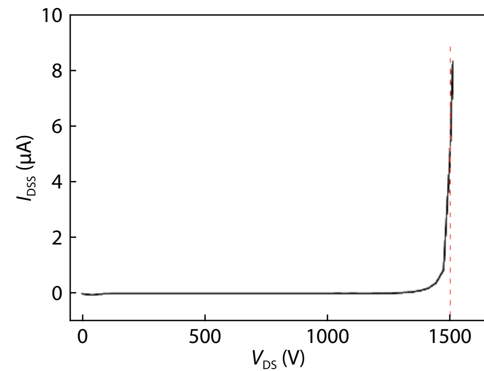

Fig. 9. (Color online) Drain–source leakage current at V_{GS} = 0 V. The dashed red line represents V_{DS} = 1.5 kV.

resents V_{DS} = 1.5 kV. The breakdown voltage obviously exceeds 1.5 kV.

5. Conclusion

The design of our device is optimized by including epilayer parameters, cell pitch size, doping concentration in JFET region and width of JFET region. Cell pitch size and JFET region optimizations both make significant efforts to the reduction of specific on-resistance. JFET region needs careful design for both doping concentration and width. These two parameters together count for the on-resistance and E-field in gate oxide (under turn-off state). By reducing cell pitch size, the specific on-resistance decreases by about 1 mΩ·cm^2. By reducing JFET width and adding n-type doping in JFET region, the specific on-resistance decreases by about 1 mΩ·cm^2 and the E-field in gate oxide is still in a safe range. Edge termination is also doped by P-well recipe and a lower maximum E-field is achieved under breakdown status. Finally, 1.2 kV / 15 mΩ SiC MOSFETs are realized with $R_{on,\ sp}$ of 3.4 mΩ·cm^2, breakdown voltage exceeding 1.5 kV and gate threshold voltage around 2.6 V.

Acknowledgements

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