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Mathematical analysis of organic-pass transistor using pseudo-p-OTFTs

Shagun Pal and Brijesh Kumar†

Department of Electronics and Communication Engineering, MMMUT Gorakhpur- 273010, India

Abstract: Steady state behavior analysis of organic thin film transistor (OTFTs) has been thoroughly researched in the past few decades. Yet, this static logic analysis has drawbacks of high power dissipation and high power consumption, and a large number of prerequisites in the number of transistors for the digital logic circuit application. Hence, to overcome these basic fundamental drawbacks of static logic, the dynamic logic study of organic thin film transistor has been analyzed in this paper. The fundamental basic of dynamic logic is a pass transistor for which logic high and logic low model is designed at an operating voltage of 5 V and frequency of 5 kHz. Additionally, the novel approach of analytical model for organic pass transistor (OPT) circuit is included and verified using MATLAB. The transient individualities of organic pass transistor OPT are examined through Atlas 2-D numerical device simulator. The reduction in the power dissipation along with additional voltage scaling and reduction in the clock frequency such as pipelining may further enable the applications into more complex VLSI ICs.

Key words: organic-pass transistor (OPT); logic high; logic low; pseudo-p; dynamic state; analytical model

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1. Introduction

Organic electronics have attracted enormous attention in the recent years because of their advantages and compatibility with flexible electronics. An organic thin film transistor (OTFT), due to its low cost and flexible nature, finds applications in radio frequency identification (RFID) tags, sensors, digital switches, actuators, smart cards, memory circuits and Flexible display driven as backplane using OTFTs[1–4]. In all these applications, logic gates using organic TFTs are required, which should fulfill the performance criteria in terms of wide output voltage range, circuit area and power consumption.

The most ideal conformation for the building blocks of using digital logic circuits is CMOS configuration which provide the benefits of existence of complementary technology. However, the complementary logic circuits are not quite feasible in organic TFTs because of the difference in mobility charge carrier of p- and n-type transistors, which effects the robustness of digital design. Unipolar technologies have an advantage over complementary technology because they are less complex in terms of fabrication and provide less manufacturing cost. Yet, they have a disadvantage of large area and power dissipation[5]. Previous works has reported the design of organic TFTs using conventional Zero-VGS (ZVLL) and diode connected (DLL) p-type OTFT[6]. However, these configurations consume a high steady state power and the circuit area is high because the pull down requires the large W/L ratio to shift the output voltage close to 0 V. Subsequently, this leads to serious design criteria to solve these problems. Consequently, pseudo-CMOS logic circuits[7, 8] were proposed, which are still under the constant interest of researchers. This logic is helpful in providing a large dynamic output range but, due to its usage of additional power supply circuitry, high steady state power consumption and large circuit area, it still needs improvement. This can be achieved by using Dual gate OTFT, which increases the process steps[9].

So far, these circuits were based on the steady state behavior of the logic (i.e. static logic), which is highly reliable for the flexible electronic operations. A differential logic circuit is another recent approach to analyses the issues related to static logic[10]. This circuit make use of combinational logic circuits and positive feedback, which provide strong pull-up and pull-down paths. Consequently, it consumes negligible steady state current but as the number of transistors required is doubled therefore the circuit area is increased. Thus, dynamic logic is becoming more of an interest to implement a complex digital circuitry as it provides less area and negligible steady state current[11]. Kim *et al.*[12] first proposed the concept of dynamic logic circuits using n-type a-IGZO TFTs to resolve the problem. This paper hence-forth makes use of the concept and has proposed the design of dynamic logic circuits using p-type OTFTs. The fundamental block of dynamic logic is the pass transistor. Elsobky *et al.*[13] mentions the concept of pass transistor and has designed 1-stage shift register based on a new biased load dynamic flip flop.

In this work, the analytical modelling of organic pass transistor has been done for the logic high and logic low. The result has been verified through calculation and simulation. Making use of this analytical model concept, the paper is sub-sectioned into four categories. The first section deals with the state of art of the work acknowledged in the field of digital circuits logic using organic thin film transistor. Additionally, the basic of dynamic logic circuit is the pass transistor, which has been studied for the logic high and low signal of the organic thin film transistor thereby making use of the basic compact

Correspondence to: B Kumar, bkiitr@gmail.com
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model of the MOSFET. Lastly, the results are verified with the analytical work in order to study the robustness of the design for the further use in more complex digital circuitry.

2. Organic pass transistor (OPT)

The basic building block of p-type dynamic logic circuitry is the pass transistor[14]. This section deals with the analytical modelling of organic pass transistor. The working model here is taken from the conventional compact model used for MOSFET keeping in advent of the fact that the basic difference between the working of MOSFET and OTFT is the inversion of charge in the previous one, followed by accumulation of charge in the latter. Compact DC model for OTFT[15, 16] has been defined previously and in this paper the standard equation used for OTFTs drain current equations are conventionally recognized in Ref. [17].

$$I_{ds} = \frac{W}{L}\mu C_i\left[\left(V_{gs} - V_t\right)V_{ds} - \frac{1}{2}V_{ds}^2\right]. \tag{1}$$

For linear region,

$$V_{ds} \leqslant V_{gs} - V_t,$$

$$I_{ds} = \frac{W}{L}\mu_l C_i\left[\left(V_{gs} - V_t\right)V_{ds}\right]. \tag{2}$$

For saturation region,

$$V_{ds} > V_{gs} - V_t,$$

$$I_{ds} = \frac{W}{2L}\mu_s C_i\left[\left(V_{gs} - V_t\right)^2\right], \tag{3}$$

where W, L, C_i, μ_l, μ_s and V_t are channel width, channel length, gate insulator capacitance per unit area, linear mobility, saturation mobility and threshold voltage respectively. An OTFT uses an electric field to modulate the conduction of an active layer located at the interface between an insulator and organic semiconductor. Hence, it is a field effect transistor (FET) similar to the well-known metal oxide field effect transistor (MOSFET), which is a fundamental block for integrated circuits. A distinguished feature between an organic TFT (O-TFT) and MOSFET is the principle of operation; i.e., channel formation in OTFT is through accumulation process wherein MOSFET through inversion process as also reported in Refs. [18, 19]. This paper adopts the model given by Gundlach *et al.*[20] where field effect mobility of OTFT is extracted from the drain current equations described for the single crystalline MOSFET as per given in Eq. (1)[17]. Hamilton *et al.*[21] has reported the concept of dispersive carrier transport in the organic material that modified the conventional equation of MOSFET for OTFT and discussed through Eqs. (1)–(3) with an additional parameter γ, associated with the non-linear behavior of the device as in Eqs. 2(a) and 3(a)

$$I_{ds}^{lin} = -\mu_{lin}C_{ox}\frac{W}{L}\left(V_{gs} - V_t\right)^{\gamma}V_{ds}, \tag{2a}$$

$$I_{ds}^{sat} = -\mu_{sat}C_{ox}\frac{W}{L}\left(V_{gs} - V_t\right)^{\gamma+1}, \tag{3a}$$

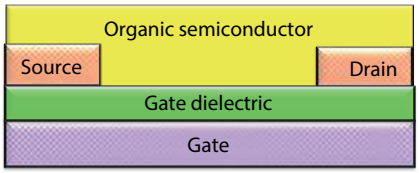

Fig. 1. (Color online) Schematic representation of the bottom gate bottom contact organic thin film transistor.

where μ_{lin} and μ_{sat} is the linear and saturation field effect mobility of the organic device. The parameter γ has been expressed in Eq. 3(b)

$$\gamma = 2\frac{T_o}{T} - 1. \tag{3b}$$

T_o is the characteristic temperature around the Fermi level of the inorganic semiconductor and is valid for the equation $T < T_o$. For organic semiconductor, γ is always greater than 1 and has been reported around 1.1.

The field effect mobility for the linear region is derived from the trans-conductance g_m and is given as in Eq. (4)

$$\mu_l = \frac{Lg_m}{WC_iV_{ds}}, \tag{4}$$

and the mobility in saturation region is calculated from Eq. (3) which is as follows:

$$\mu_s = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{ds}}}{\partial V_{gs}}\right)^2. \tag{5}$$

These equations work on the assumptions of constant mobility and ignore the dependence of gate voltage on mobility of organic transistors[22].

2.1. Device structure

OTFTs can be categorized as single gate and dual gate organic devices. A single gate transistor comprising of organic semiconductor as an active channel can be further categorized as the bottom contact and top contact, depending upon the position of the electrode. This paper adopts bottom gate bottom contact single gate OTFT, shown in Fig. 1 and, the device parameters from Ref. [9], as listed in Table 1.

2.2. Simulation study

The ATLAS (Silvaco) tool has made an excellent effort to study the device physics and behavior of organic thin film transistor using the Poole Frenkel mobility model[23] as in Eq. (6)

$$\mu(E) = \mu_0\exp\left[-\frac{\Delta}{kT} + \left(\frac{\beta}{kT} - \gamma\right)\sqrt{E}\right], \tag{6}$$

where $\mu(E)$, E and μ_0 denotes field dependent mobility, electric field, and null field mobility respectively. These, including γ, are the fitting parameters which are taken into effect for the simulation result and the mobility model. Δ and β are defined as the energy of activation and Poole-Frenkel hole aspect correspondingly. The Poole-Frenkel mobility model describes the conduction mechanism of the trap carrier owing to the electric field thermal excitation at the interface. Thermal disorder leads to charge carrier localization around the trap region thereby reducing the drain current (I_{ds}) at low field region.

Table 1. Device parameters for the organic material based device[9].

Parameter	Value
Gate electrode (Si)	150 nm
Bottom gate (SiO_2), t_{ox}	100 nm
OSC thickness (t_{osc}) (pentacene)	200 nm
Width of S/D (t_s/t_d) (gold)	80 nm
Active layer length (L)	25 μm
Active layer width (W)	800 μm

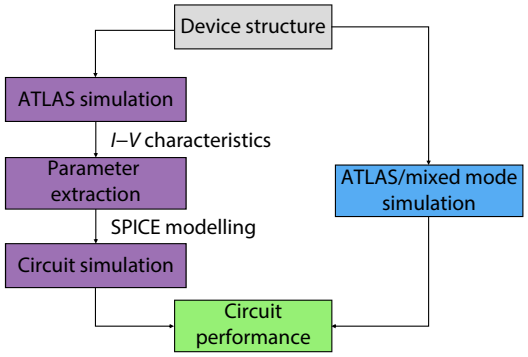

Fig. 2. (Color online) Schematic representation of the mixed mode analysis of ATLAS for circuit implementation.

The ATLAS simulation process typically consists of three different modes: 1) structural and geometrical description, 2) physical device models and 3) defining material properties, defects and device operating conditions. In the simulation process, the defined mobility model necessitates the calculation by considering the mesh analysis at each individual region, comprising of complex triangular grids. Henceforth, a high degree of accuracy depends upon the high degree of density of meshing. This simulator gives insight into the underlying microscopic mechanism of materials along with precise monitoring of the device dimensions[24]. It also exhibits finite element based 2D numerical simulator provide the implementation of the circuit applications in the digital as well as analog field using mixed-mode module of ATLAS. The ability of Mixed-Mode is to link any ATLAS device into a SPICE circuit. The process flowchart in Fig. 2 provides a schematic flow of the implementation of the digital logic using the TCAD tool.

2.3. Device characterization and parameter extraction

The electrical characterization including output as well as transfer characteristics is drawn in Figs. 3(a) and 3(b), respectively. The I_d–V_d curve in Fig. 3(a) shows the constant saturation variation suggesting a low device resistance while Fig. 3(b) shows the transfer characteristics analysis regarding behavior associated with the model at around the threshold voltage regime. The device parameters are extracted through simulation and validated with the experimental results as summarized in Table 2. These parameters show close proximity with the experimented work.

To show the linear and saturation characteristics using MATLAB, Table 3 shows the fitting parameter that is used to model the device for the validity and Fig. 4 shows the comparative analysis of the model[21], experimental and simulated transfer characteristics for the organic devices.

3. Analytical modelling of OPT

Previously reported work shows that logic gates are the

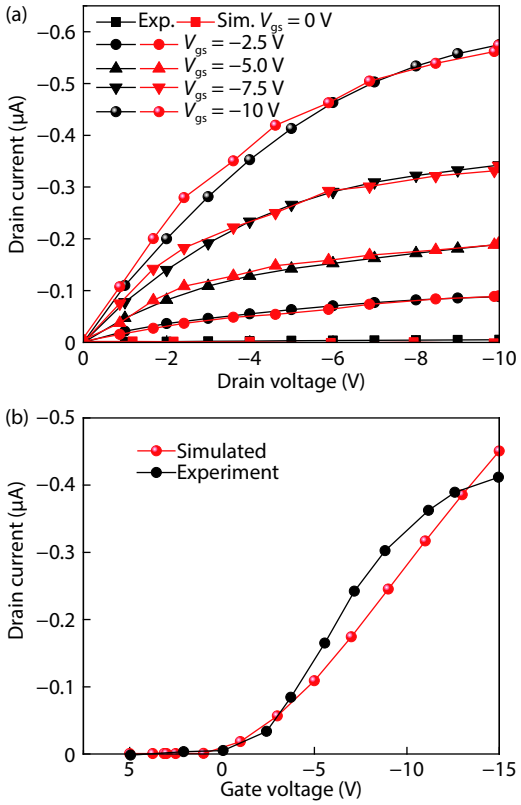

Fig. 3. (Color online) Experimental[9] and simulated device results: (a) output and (b) transfer characteristics curve.

essential block for digital and complex analog circuits. This section shows the basic working study of organic pass transistor for both the logics: high and low.

3.1. Logic high

This design depends upon the fact that the p-type organic pass transistor is able to pass logic high signal without any problem when the clock signal (CLK) signal is active low; i.e., 0 at its gate[25]. It can be hereby proved that p-type OPT is good at passing a "1" signal and is said to be strong high logic. Subsequently, this fact depends upon the logic level of the clock signal (CLK) whether it is high; i.e., active for the transfer of logic high signal or low for the transfer of logic low signal. In any of the case the dependence of logic level values assumes from the voltage at the soft node V_x.

Because the working of p-type OPT is considered to be converse of n-type, the proposed design is made for logic high Fig. 5(a) and logic low signal as in Fig. 6(a). In the logic high, the signal is passed through the pass transistor directly similar to the p-channel transistor in a complementary transmission gate switch. The promise of this approach is that fewer transistors are required to implement any function. In the following, we first examine the analytical model for charge up event for OPT. Assume that the voltage at the V_x is initially equal to 0 i.e. $V_x = 0$ V at $t = 0$. A logic high is given to the input terminal which corresponds to $V_{in} = V_{DD}$.

For the transistor T1, $V_{gs} = 0$ and $V_{ds} = V_{dd} = -V_{DD}$. Thus, T1 is in saturation region and hence C_x will charge up to the value given as:

$$C_x \frac{dV_x}{dt} = K_p \frac{W}{L}\left(V_{dd} - V_x - V_{tp}\right)^2. \quad (7)$$

Table 2. Electrical parameter comparison of pentacene-based single gate organic thin film transistor.

Parameter	Experiment[9]	Simulated
μ (cm^2/(V·s))	0.02	0.019
I_{on}/I_{off}	3.2×10^3	5.1×10^3
SS (V/dec.)	2.0	2.3
g_m (μS)	0.044	0.041
V_{TH} (V)	– 2.0	– 2.1

Table 3. Fitting parameters for the transfer characteristics using the model through MATLAB[21].

Parameter	Value
W/L	800/25
C_{ox}	0.345×10^{-9} F/cm^2
μ	0.012 cm^2/(V·s)
γ	2.1[21]
T_o	465 K[21]
V_t	–2.1 V

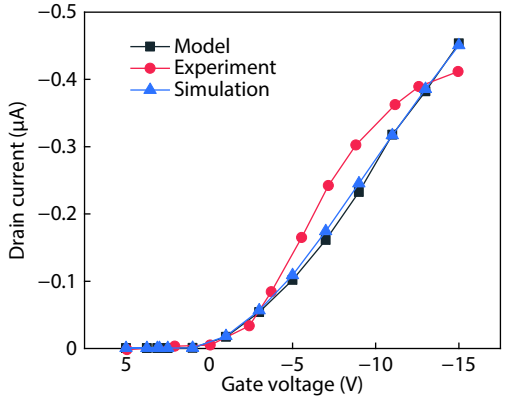

Fig. 4. (Color online) Transfer characteristics curve validity of simulated device through model[21] and experimental[9].

Integrating Eq. (5), we get

$$\int_0^t \mathrm{d}t = \frac{C_x L}{WC_{ox}} \int_0^{V_x} \frac{1}{V_{dd} - V_x - V_{tp}} \mathrm{d}V_x. \tag{8}$$

Integrating Eq. (6), we get

$$t_{sat} = \frac{C_x L}{WC_{ox}} \ln \frac{V_{dd} - V_{tp}}{V_{dd} - V_{tp} - V_x}, \tag{9}$$

$$\frac{WC_{ox}t_{sat}}{LC_x} = \ln \frac{V_{dd} - V_{tp}}{V_{dd} - V_{tp} - V_x}. \tag{10}$$

Taking antilog on both sides and considering saturation time as t we get:

$$\mathrm{e}^{\frac{WC_{ox}}{LC_x}t} = \frac{V_{dd} - V_{tp}}{V_{dd} - V_{tp} - V_x},$$

$$\mathrm{e}^{-\frac{WC_{ox}}{LC_x}t} = 1 - \frac{V_x}{V_{dd} - V_{tp}}. \tag{11}$$

Table 4. Comparison between analytical and simulation parameters for logic high transfer signal.

Parameter	Analytical	Simulated
Output voltage (V)	2.89	3

Solving the above, we get:

$$V_x = (V_{dd} - V_{tp})\left(1 - \mathrm{e}^{-\frac{WC_{ox}}{LC_x}t}\right). \tag{12}$$

The variation of the node voltage given by Eq. (10) is graphically shown in Fig. 5(b) with respect to time. The value rises and reaches the maximum value of V_{DD}–V_{tp}. Table 4 shows the comparative study between the simulated and analytical parameters for the logic high transfer signal. Fig. 5(c) shows the simulated transient behavior of the design for the time period of 4 ms. When the clock is high at the gate, the OPT is off and the input is low (i.e. V_{gs} = 0 then V_{ds} = V_{DD} = 5 V) and hence T1 transistor is in saturation and the analytical value from Eq. (10) is 2.89 V.

The analytical value is very much in close approximation of the simulation results and is derived from Eq. (10) which is tried to fit through MATLAB as shown in Fig. 5(b). The variation in the result is because the iteration process is done through Newton Raphson (NR) algorithm of ATLAS 2-D simulator. This algorithm is used in the transient state as well as steady state analysis. Moreover, in this work the full newton Raphson algorithm is used for the transient sate analysis.

3.2. Logic low

Previous work has shown that the pass transistor made using p-channel and n-channel for digital logic signals were operated using complementary clock signal at the gate in order to switch the transition from high to low, and vice versa[25, 26]. However, the main drawback of these complementary clock signals is to get completely off and on, and hence were not feasible in a hybrid electronic integrated circuit. This was overcome by the use of unipolar clock signal by replacing these channels into a transmission gate switch. Moreover, an alternative approach to static logic is a dynamic circuit design, which despite of having inferior robustness provides several advantages.

As p-channel device is considered to be a strong pull up as they are able to pass logic high signal discussed above. However, they are considered weak pull down because they are not able to pass logic low signal. Henceforth, in this work a new circuitry is proposed for the logic low. This circuitry is made using two inverters and one pass transistor as in Fig. 6(a). The transistor sizing used for the inverter circuits used for the organic pass transistor is listed in Table 5.

In order to provide the path for the discharging at the output, the biased load design has been implemented which make use of external bias voltage V_{bias}. The analytical study of this proposed design is done and verified by the simulation as shown in Fig. 6(c) through MATLAB and Fig. 6(d) respectively.

Consider Fig. 6(b), the circuitry is made using biased-load design. For the transistor T3,

$$V_{gs} = 0, \quad V_{ds} = -V_{DD}.$$

T3 is working in the linear region.

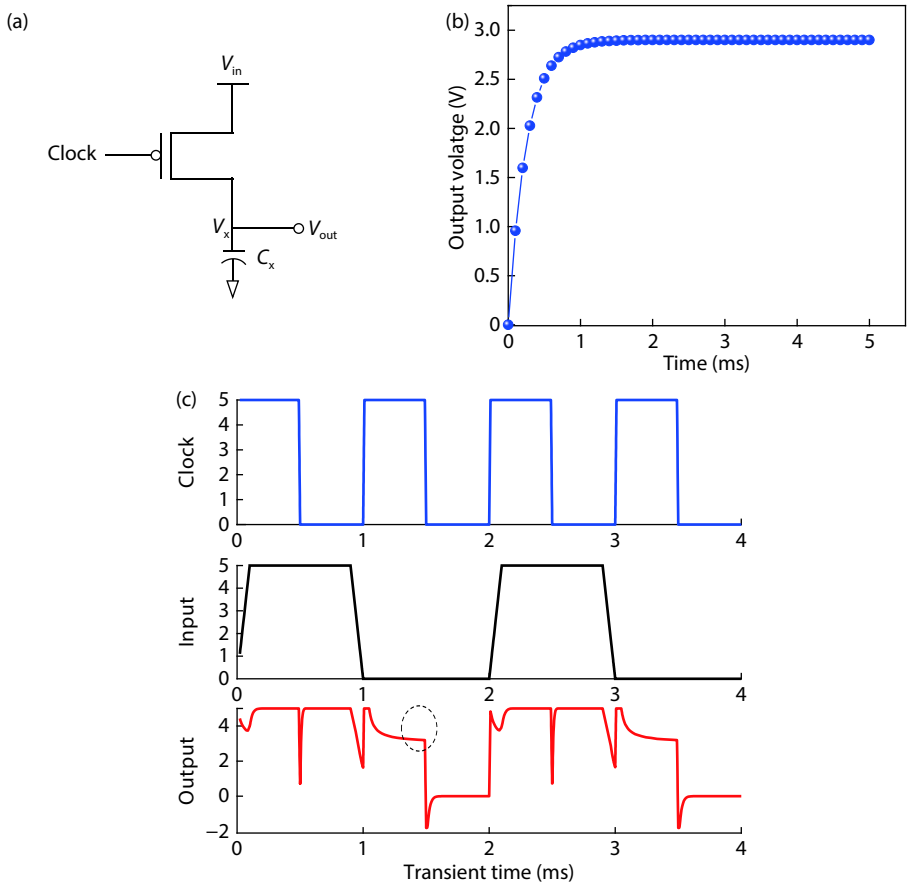

Fig. 5. (Color online) (a) The basic circuitry for logic high organic-PT. (b) Variation of output voltage with respect to time through MATLAB. (c) Simulation result for the logic high signal with the input supply of 5 V.

$$C_x\frac{dV_{o1}}{dt} = K_p\frac{W}{L}\left[\left(V_{gs}-V_{th}\right)V_{ds}-\frac{V_{ds}^2}{2}\right], \tag{13}$$

where $V_{gs} = 0$, $V_{ds} = -V_{DD}$ and $V_{th} = V_{tp}$,

$$2C_x\frac{dV_{o1}}{dt} = 2\left(-V_{tp}\right)\left[\left(V_{out}-V_{DD}\right)-\left(V_{DD}-V_{out}\right)^2\right]K_p\frac{W}{L}. \tag{14}$$

Putting $K = V_{out} - V_{DD}$

$$2C_x\frac{dV_{o1}}{dt} = 2\left(-V_{tp}\right)K-K^2, \tag{15}$$

$$2C_x\frac{dV_{o1}}{dt} = -K\left[2\left(V_{tp}+K\right)\right]K_p\frac{W}{L}, \tag{16}$$

$$\int_{V_{DD}}^{V_{tp}}\frac{dV_{01}}{-K(2V_{tp}+K)} = \int_0^t\frac{dt}{2C_x}K_p\frac{W}{L}. \tag{17}$$

Solving by the method of partial fractions we get

$$\int_{V_{DD}}^{V_{tp}}\frac{dV_{01}}{-K\left(2V_{tp}+K\right)} = \int_{V_{DD}}^{V_{tp}}\frac{\frac{-1}{2V_{tp}}}{K}+\int_{V_{DD}}^{V_{tp}}\frac{\frac{1}{2V_{tp}}}{2V_{tp}+K} = \frac{-1}{2V_{tp}}\ln K+\frac{1}{2V_{tp}}\ln\left(2V_{tp}+K\right), \tag{18}$$

where $K = V_{out} - V_{DD}$,

$$\frac{K_p\frac{W}{L}}{2C_x}t = \frac{1}{2V_{tp}}\ln\left(1+\frac{V_{tp}}{V_{tp}-V_{DD}}\right). \tag{19}$$

Taking antilog on both sides of Eq. (19), we get

$$1-e^{\left(K\frac{W}{L}/C_x\right)V_{tp}t} = \frac{2V_{tp}}{V_{out}-V_{dd}}, \tag{20}$$

$$V_{out}-V_{dd} = \frac{2V_{tp}}{1-e^{\frac{(KW/L)V_{tp}t}{C_x}}}, \tag{21}$$

$$V_{out} = V_{dd}+2V_{tp}\left(1-\exp\frac{KW/LV_{tp}t}{C_x}\right)^{-1}. \tag{22}$$

On expanding the series of $(1 - x)^{-1} = 1 + x + x^2 \ldots$. and neglecting the higher order terms in Eq. (22) we get:

$$V_{out} = V_{dd}+2V_{tp}\left(1+\exp\frac{KW/LV_{tp}t}{C_x}\right) \tag{23}$$

Finally, the variation of Eq. (23) is plotted as a function of time in ms in Fig. 6(c). Table 6 shows the comparative study between the simulated and analytical parameters for the logic low transfer signal.

If the node voltage goes higher than V_{DSAT}, the organic pass transistor starts operating in linear mode and discharging of the parasitic capacitance takes place through calculating the fall time expression and hence the following study is done to measure it. For the transistor T3, $V_{gs} = 0$, $V_{ds} = -V_{DD}$ then T3 is working in the linear region.

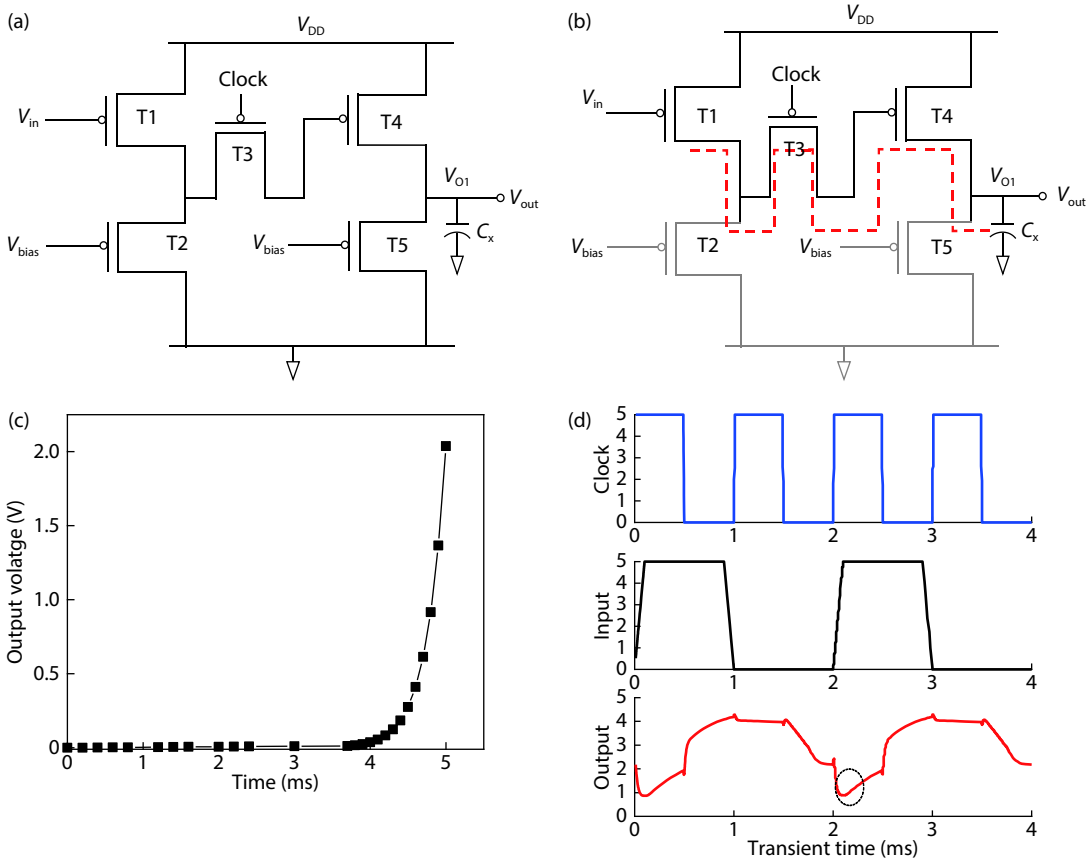

Fig. 6. (Color online) (a) The basic circuitry for logic low organic-PT. (b) working principle of the proposed model for logic low signal. (c) Variation of output voltage with respect to time through MAT Lab. (d) Simulation result for the logic low signal with the input supply of 5 V.

Table 5. Dimensions for the simulated parameters of the proposed inverter design.

Parameter	Value
W/*L* (T1)	5000 μm/100 μm
W/*L* (T2)	300 μm/100 μm
W/*L* (T3)	300 μm/100 μm
W/*L* (T4)	5000 μm/100 μm
W/*L* (T5)	300 μm/100 μm
C_{OLED}	0.6 nF

Table 6. Comparison between analytical and simulation parameters for logic low transfer signal.

Parameter	Analytical	Simulated
Output voltage (V)	0.012	0.5

$$C_x\frac{dV_{o1}}{dt} = K_p\frac{W}{L}\left[(V_{gs}-V_{th})V_{ds}-\frac{V_{ds}^2}{2}\right], \tag{24}$$

$$2C_x\frac{dV_{o1}}{dt} = 2(-V_{tp})\left[(V_{out}-V_{DD})-(V_{DD}-V_{out})^2\right]K_p\frac{W}{L}. \tag{25}$$

Putting $K = V_{out} - V_{DD}$,

$$2C_x\frac{dV_{o1}}{dt} = 2(-V_{tp})K-K^2, \tag{26}$$

$$2C_x\frac{dV_{o1}}{dt} = -K\left[2(V_{tp}+K)\right]K_p\frac{W}{L}. \tag{27}$$

$$\int_{V_{DD}}^{V_{tp}}\frac{dV_{01}}{-K(2V_{tp}+K)} = \int_0^t\frac{dt}{2C_x}K_p\frac{W}{L}. \tag{28}$$

Solving by the method of partial fractions we get

$$\begin{aligned}\int_{V_{DD}}^{V_{tp}}\frac{dV_{01}}{-K(2V_{tp}+K)} &= \int_{V_{DD}}^{V_{tp}}\frac{\frac{-1}{2V_{tp}}}{K}+\int_{V_{DD}}^{V_{tp}}\frac{\frac{1}{2V_{tp}}}{2V_{tp}+K}\\ &= \frac{-1}{2V_{tp}}\ln K+\frac{1}{2V_{tp}}\ln(2V_{tp}+K),\end{aligned} \tag{29}$$

where $K = V_{out} - V_{DD}$,

$$\frac{K_p\frac{W}{L}}{2C_x}t_{lin} = \frac{1}{2V_{tp}}\ln\left(2+\frac{V_{tp}}{V_{tp}-V_{DD}}\right), \tag{30}$$

$$t_{lin} = \frac{LC_x}{K_pWV_{tp}}\ln\left(2+\frac{V_{tp}}{V_{tp}-V_{DD}}\right). \tag{31}$$

Using $\frac{LC_x}{K_pWV_{tp}} = S$ (new constant),

$$t_{lin} = S\ln\left(2+\frac{V_{tp}}{V_{tp}-V_{DD}}\right). \tag{32}$$

The variation of new constant S can be analyzed by keeping this value in Eq. (1) of the drain current equation of organic thin film transistor in linear region. We find that I_{ds} is in-

versely proportional to S as given as in Eq. (33):

$$I_{ds} = \frac{C_x}{SV_{tp}}\left[\left(V_{gs} - V_t\right)V_{ds} - \frac{1}{2}{V_{ds}}^2\right]. \quad (33)$$

Thus, it is inferred that S is directly proportional to the length of the channel. Since, the channel length is dependent on the gate voltage hence it is also proportional to it. On calculating the unit of S, we found it is cm^2/V^2 which is the inverse of the square unit of energy of the channel. Hence channel length needs to be smaller in order to have strong energy variation.

4. Conclusion

In this paper, the mathematical model for the organic all p-type pass transistor (OPT) based on compact DC model of MOSFET is discussed. To validate the result, the OPT has been verified through analytical model using MATLAB. It was found that the simulated and the analytical parameters are very much in agreement to each other for the logic high and logic low level. This modelling will be helpful in designing dynamic logic circuits based on organic thin film transistors.

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