

A high performance adaptive on-time controlled valley-current-mode DC–DC buck converter

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Abstract: This paper presents an AOT-controlled (adaptive-on-time, AOT) valley-current-mode buck converter for portable application. The buck converter with synchronous rectifier not only uses valley-current-mode control but also possesses hybrid-mode control functions at the same time. Due to the presence of the zero-current detection circuit, the converter can switch freely between the two operating modes without the need for an external mode selection circuit, which further reduces the design difficulty and chip area. The converter for the application of high power efficiency and wide current range is used to generate the voltage of 0.6–3.0 V with a battery source of 3.3–5.0 V, while the load current range is 0.05–2 A. The circuit can work in continuous conduction mode with constant frequency in high load current range. In addition, a stable output voltage can be obtained with small voltage ripple. In pace with the load current decreases to a critical value, the converter transforms into the discontinuous conduction mode smoothly. As the switching period increases, the switching loss decreases, which can significantly improve the conversion efficiency. The proposed AOT controlled valley current mode buck converter is integrated with standard 0.18 μm process and the simulation results show that the converter provides well-loaded regulations with power efficiency over 95%. When the circuit switches between the two conduction modes drastically, the response time can be controlled within 30 μs . The undershoot voltage is controlled within 25 mV under a large current hopping range.

Key words: adaptive on-time; buck converter; fast response; constant frequency; high efficiency

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1. Introduction

Portable electronic devices such as mobile phones and laptops, are almost completely integrated into every aspect of people's daily life, which puts higher demands on the performance of the power management systems^[1–5]. DC–DC converters are used to generate many different output voltages from battery power supplies based on particular applications. That is the reason why control methods of the switching power supply are the main influencing factors of conversion speed and accuracy^[6]. Feedback control methods of the buck converter are mainly divided into voltage mode and current mode. Current-mode modulation has a faster transient response due to the direct feedback path from the inductor compared with voltage-mode control. Furthermore, a better output voltage with less voltage ripple can be obtained^[7, 8]. Currently, switching power supplies are developing towards lower input voltages with a wide input range. Therefore, the valley current control mode is increasingly receiving attention and application.

A common method to increase the power efficiency of buck converter is the constant on-time (COT) pulse frequency modulation (PFM) method^[9–11]. The traditional voltage mode COT control method has always been popular among researchers thanks to its simple circuit configuration, which can be realized just using a simple on-time control module and does not need a compensation network^[12]. However,

due to its constant on-time, it can only adapt to changes in input voltage, load current and output voltage by adjusting its switching period. If the switching frequency changes with the working conditions during the normal operation of the converter, it will bring serious electromagnetic interference (EMI) problems to the circuit, which affects the sensitivity of the phase-locked-loop (PLL) circuit and the ratio frequency integrated circuits^[8]. Pulse width modulation (PWM) method can be used under high load current conditions to maintain a constant frequency^[13–15]. But as the load current decreases, the power dissipation on the switches takes up a major part of the overall power consumption if the switching frequency remains at the initial constant value. Therefore, researchers have also proposed some methods of constant frequency modulation^[16–18].

In this paper, an adaptive on time (AOT) valley current mode control scheme is proposed in which the on-time can be adjusted dynamically during CCM and the frequency decreases with the load current under DCM. Constant frequency under CCM can reduce the adverse effects of frequency changes on the output while minimizing the electromagnetic problem simultaneously, which is beneficial to the design of the subsequent filter circuit. For circuit implementation, a simple and accurate zero current circuit is adopted, which allows the converter to switch smoothly between the two conduction modes without the need for an additional mode selection circuit. The rest of the paper is organized as follows. The design of several key modules is presented in Section 2. Simulation results and related analysis are given in Section 3. Finally, the paper is concluded in Section 4.

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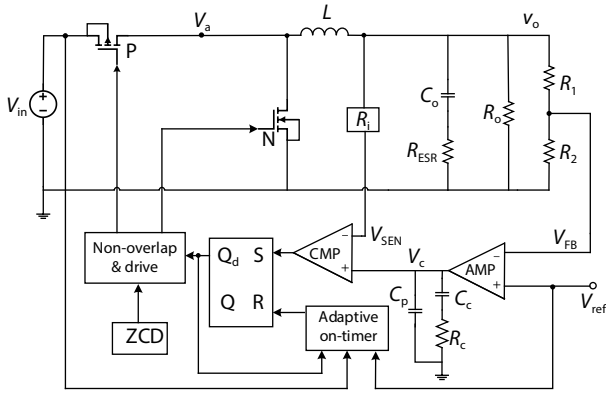


Fig. 1. Schematic of the AOT controlled buck converter.

2. Control strategy and design considerations

2.1. Overall circuit design

The system block diagram of the proposed adaptive on-time controlled buck converter is illustrated in Fig. 1 which is composed of power stage and feedback control stage. The power stage primarily includes two power transistors for on-off switching and a LC filter, passing the energy from the input to the output^[19].

The output voltage is divided by resistor R_1 and R_2 to produce a partial voltage V_{FB} , which is used to compare with a reference voltage V_{ref} . The current sensing circuit detects the current of the freewheeling transistor, and the detected signal V_{SEN} is input to the comparator simultaneously with the output of the error amplifier. When V_{SEN} is lower than V_c , the high level generated by the comparator is fed back to the power stage to turn on the P switch through a series of control modules. At the same time, the N switch is turned off to increase the output voltage until V_{FB} raises to V_{ref} . Then, the next conversion cycle starts. A filter network consisting of capacitor C_0 and inductor L produces a steady DC output voltage for DC-DC conversion.

In contrast from the traditional commonly used peak current mode control, this paper uses the valley current mode control and the advantages of the valley current mode are reflected in the following aspects.

(1) A lower duty cycle voltage conversion can be achieved, that is, a large input with a low output. When the duty cycle is reduced, the P switch has a shorter on-time, which put higher requirements on the performance of the conventional current sensing circuit. While the free-wheeling transistor has a longer on-time, so that the current sampling is more convenient.

(2) Better transient response performance. Unlike systems that use peak current mode control, the status of the power transistor which is controlled by the valley current mode is not synchronized with the clock signal, so it can be turned on or off at any time.

2.2. Constant frequency implementation

To eliminate the adverse effects of the varying frequency, parameters related to the switching frequency under CCM is analyzed theoretically:

$$V_L = L \times \frac{di_L}{dt} \Rightarrow \Delta i_L = \frac{V_L}{L} \times \Delta T. \quad (1)$$

In the conduction phase of the P switch, the change of in-

ductor current is calculated as follows:

$$\Delta i_L (+) = \frac{(V_{in} - V_{DSP} - I_L R_L) - V_o}{L} \times T_{ON}. \quad (2)$$

In the off phase of the P switch, the change of the inductor current is as follows:

$$\Delta i_L (-) = \frac{V_o + (V_{DSN} + I_L R_L)}{L} \times T_{OFF}. \quad (3)$$

When the circuit operates under steady state, the increase in inductor current in each cycle is equal to the amount of reduction. Therefore, the switching period can be obtained from Eq. (2) and Eq. (3):

$$T_s = \frac{V_{in} - V_{DSP} + 2I_L R_L + V_{DSN}}{V_o + V_{DSN} + I_L R_L} \times T_{ON}, \quad (4)$$

where the quantity, R_L is the equivalent resistance of the inductor. V_{DSP} and V_{DSN} represent the forward voltage drop of the P switch and the N switch, respectively. Since in a well-designed buck converter these parameters are quite small compared to the DC value of V_{in} and V_o , they can be neglected in the calculation process. The simplified calculation result is as follows:

$$T_s = \frac{V_{in}}{V_o} \times T_{ON}. \quad (5)$$

To keep the switching frequency unchanging in CCM, it is necessary to eliminate the influence of V_{in} and V_o by adjusting T_{ON} . Based on the traditional COT control, an input voltage feedforward control loop and an output voltage feedback loop are introduced. So that T_{ON} would vary with changes of input voltage and output voltage. Thereby, the frequency is stabilized at a constant value. The corresponding on-time is as follows:

$$T_{ON} = \frac{kV_{ref}C_1}{gV_{in}}, \quad (6)$$

where gV_{in} represents the value of the voltage controlled current source (VCCS), while kV_{ref} represents the value of the voltage controlled voltage source (VCVS). It is implemented by the circuit diagram shown in Fig. 2.

Since the actual output voltage is a variable with ripple component, if the output voltage is directly used to control the VCVS, the circuit would have stability problems. A reasonable solution is to use the reference voltage V_{ref} instead of the output voltage. When the VCCS (gV_{in}) charges the capacitor C_1 to the voltage of the VCVS (kV_{ref}), the input terminal of the RS flip-flop, R, will be triggered to high level, which turns the P switch off and turns the N switch on. Upon substituting Eq. (6) into Eq. (5), the final expression of T_s can be obtained as follows:

$$T_s = \frac{kV_{ref}C_1}{gV_o} \approx \frac{kC_1}{gm}, \quad (7)$$

where $V_o \approx mV_{ref}$, and the frequency here is constant without the influence of the input and the output voltage.

2.3. Stability analysis

To analyze the stability of the loop, it is necessary to un-

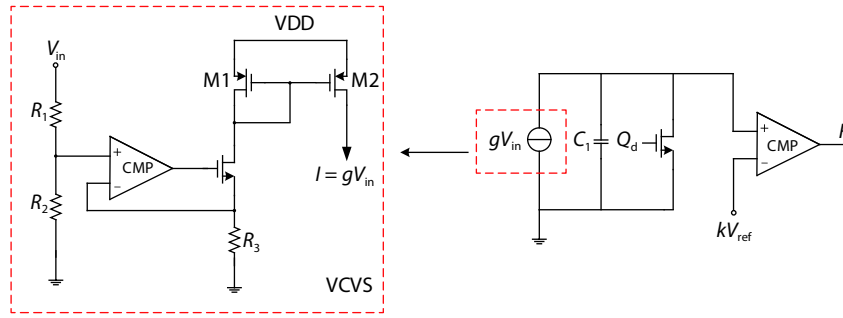


Fig. 2. The adaptive on-time controller.

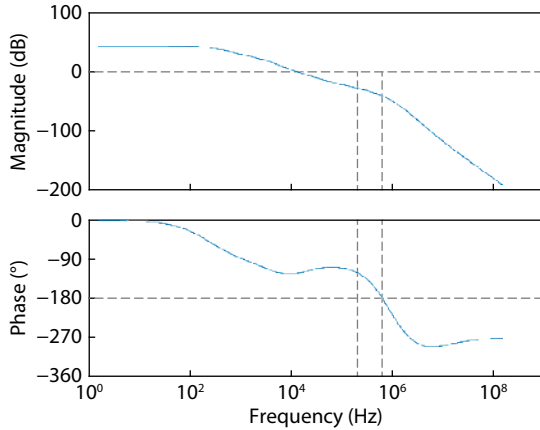


Fig. 3. Bode plot of closed loop after compensation.

derstand the transfer function of the closed-loop and analyze the impact of the zeros and poles on the system. We then determine whether the compensation network is prerequisite. Ref. [20] gives the categorical modeling method of the open loop for current mode control. In the modeling process, the switches, the inductor, the comparator, and the on-time controller are treated as a single entity, respectively. The describing function method is used to describe the transfer function from the signal V_c to the output signal V_o . The approximate loop gain function of the circuit is given as follows:

$$\frac{V_o}{V_c} = \frac{1}{R_i} \times \frac{1}{1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}} \times \frac{R_o(R_c C_o s + 1)}{R_o C_o s + 1}, \quad (8)$$

where $Q_1 = 2/\pi$, $\omega_1 = \pi/T_{ON}$. It can be seen markly from the transfer function that there are two poles which would cause the instability of the circuit.

To deal with this problem, a compensation network is indispensable for the system design. In this paper, a type II compensation network is introduced at the output of the operational amplifier, which is composed of parallel connection of resistor R_c , capacitor C_c and C_p , as shown in Fig. 1. This compensation network introduces two poles, while R_c and C_c are connected in series to produce a left half plane zero. This zero would compensate one pole of the original circuit by adjusting the magnitude of resistor R_c and capacitors C_c , C_p suitably. The gain point is extrapolated to make the feedback system more stable.

The loop-compensated transfer function is simulated in MATLAB and the Bode plot is shown in Fig. 3. The simulation is performed under the conditions of input and output

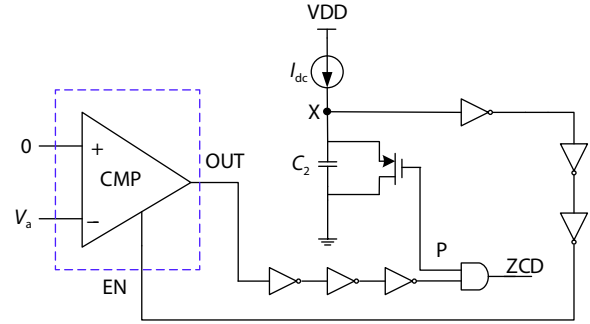


Fig. 4. Structure diagram of the zero crossing detection module.

voltage are 5 V and 1.8 V respectively, with the load current of 1 A. It can be seen from the Bode plot that the phase margin of the loop is 57.8 degrees, which satisfies the conditions for stable operation of the system.

2.4. Zero current detection

The buck converter discussed in this paper has a reference voltage of 1 V^[21] and operates at DCM under light load. In other words, when the inductor current drops to zero, the P switch and the N switch are turned off simultaneously to prevent the current from flowing back. In actual situations, when the inductor current drops to zero and the N switch is not turned off in time, there will be a current backflow, which will inevitably result in waste of energy. A zero current detection (ZCD) unit shown in Fig. 4 is added into the dead-time controller to monitor the inductor current. Since the high precision current detection circuit is complicated to design, the voltage V_a is detected actually. When the inductor current decreases, V_a is expressed as:

$$V_a = -I_L R_{ONN}. \quad (9)$$

In the discontinuous conduction mode, when the inductor current drops to zero, V_a equals to zero, too. Ideally, the moment when V_a is equal to zero is taken as the effective time of the ZCD output signal. However, due to the delay time of different circuit modules inside the converter, when V_a is equal to zero, it will take a delay time for ZCD to turn off the N switch.

As a result, the inductor current is still reversed during this delay time. Therefore, the value of V_a slightly below zero is used as the turning point^[22]. The critical V_a value used in this article is about -2.5 mV. Since the inductor current is always above zero in CCM, the ZCD signal keeps at low level to ensure the zero current detection module works only in DCM.

The overall circuit diagram of the threshold voltage com-

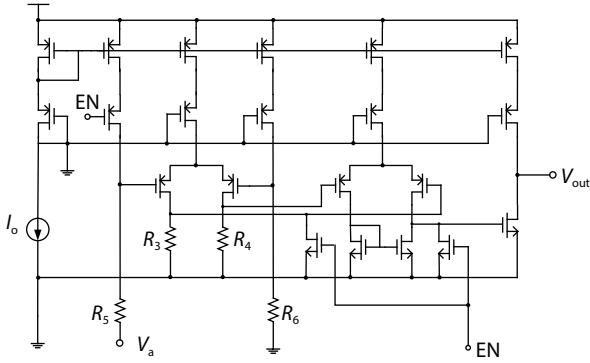


Fig. 5. The threshold voltage comparator.

parator is shown in Fig. 5. In practical applications, resistors R_3 – R_6 will be replaced by MOS transistors with constant bias. One of the advantages of this ZCD module, shown in Fig. 4, is that during the half cycle in which the P switch is turned on, that is, during the period in which the inductor current rises, the potential at point X is pulled to zero. As a result, a high level enable signal EN is generated, forcing the output of the threshold voltage comparator to a high level. Consequently, the output of the ZCD module is low during the entire charging process, which avoid a large part of energy loss. When P is high, capacitor C_2 is charged by the current source. While the potential of X rises to a certain threshold, the EN is turned to a low level, allowing the comparator to operate normally.

3. Simulation results

3.1. Switching frequency

From this analysis, the switching frequency should be ideally constant regardless of input voltage, output voltage and load current under CCM. The switching period T_s and on-time T_{on} of the converter is obtained by the simulation with standard 0.18 μm process, which is shown in Fig. 6. It is obvious from Fig. 6(a) that the switching period can be maintained at a quasi-fixed value over a large load range and the maximum changing rate can be controlled within 4%. Furthermore, the duty cycle is almost changeless as the load current if the input and output voltage are constant.

With a constant switching period, because the charge and energy delivered to the output capacitor of each cycle increase as $V_{in}^{[11]}$, the required on-time of P switch is reduced as the input voltage increases, as shown in Fig. 6(b). From the simulation results, the maximum changing rate of the switching frequency is about 5% within the test range 2.5–5 V. Conversely, in the case where the input voltage is constant, a larger turn-on time is required to charge the capacitor to obtain a larger output voltage. In other words, the duty cycle increases as the output voltage, as shown in Fig. 6(c). The maximum rate of change of the switching frequency obtained by simulation is approximately 2% within the output voltage range of 0.6–1.8 V. The above simulation results show that the major operation of AOT control is the variation of the duty ratio to obtain an expected frequency of regulator.

Compared with the traditional COT structure, the AOT structure proposed in this paper has better frequency characteristics when the input voltage and output voltage change. Simulation results for the two structures are given in Fig. 7.

The output voltage remains constant at 0.6 V when the input voltage changes from 0.8–5.0 V while the input voltage is kept at 5.0 V when the output voltage changes from 0.6–1.8 V. The switching frequency shows to be almost independent on the input voltage and output voltage under AOT control while the switching frequency of COT control varies dramatically with V_{in} and V_o . As we all know that a constant frequency is more conducive to the design of subsequent filter circuits and contributive to the stability of the whole system.

3.2. Transient performance

The ability for a converter to return to its steady state after the load current changes illustrates the robustness of the circuit^[23–25]. Fig. 8 shows the load transient waveforms. The output recovers its desired level with the error smaller than 1% in 6 and 2 μs , respectively, for the step-up and step-down load current steps between 0.4 and 1.2 A. In addition, the overshoot and undershoot voltages can also be controlled within 14 mV.

The output voltage ripple is composed of capacitor ripple and ESR ripple. So, the total ripple can be expressed as follows:

$$\begin{aligned} \Delta V_o &= \Delta V_c + \Delta V_{ESR} = \Delta i_L \left(R_{ESR} + \frac{1}{8f_s C_o} \right) \\ &= \frac{V_o(V_{in} - V_o)}{f_s L V_{in}} \left(R_{ESR} + \frac{1}{8f_s C_o} \right). \end{aligned} \tag{10}$$

In CCM, the switching frequency is quasi-constant, so that the amplitude of the output ripple is fixed at a constant value for a given input voltage and output voltage. It can also be seen from Fig. 8 that the magnitude of the output ripple is constant when only the load current changes. This phenomenon has been theoretically verified in Ref. [26].

To better illustrate the transient response characteristics of the AOT structure, comparisons in Table 1 are made to the two structures mentioned in Ref. [24] in voltage drop, voltage overshoot and recovery time. The standard of normalization is the characteristics of PWM structure. Its voltage drop is about 45 mV while the overshoot voltage is about 75 mV with a recovery time of 200 μs . From Table 1, the AOT control has faster transient performance and smaller voltage variation than PWM and COT control under load current steps.

3.3. Load regulation and line regulation

Load regulation rate is one of the ways to measure the performance of a power supply, which would reflect changes in output voltage as a function of load current. Its expression is as follows:

$$\eta = \frac{V_{o1} - V_{o2}}{V_{ref}(I_{o1} - I_{o2})}. \tag{11}$$

Actually, a change in the output load of the power supply will cause a slight change in the output voltage. For a good power supply, the changes of the output voltage due to load changes are small, typically 3%–5%. In this paper, the load regulation rate is measured under the condition of 1.2 V output voltage with the load current switching from 0.1 to 1 A. The simulation diagram is shown in Fig. 9 and the result is 0.19% after calculation, which is within acceptable limits.

The line regulation of the converter with AOT mode is

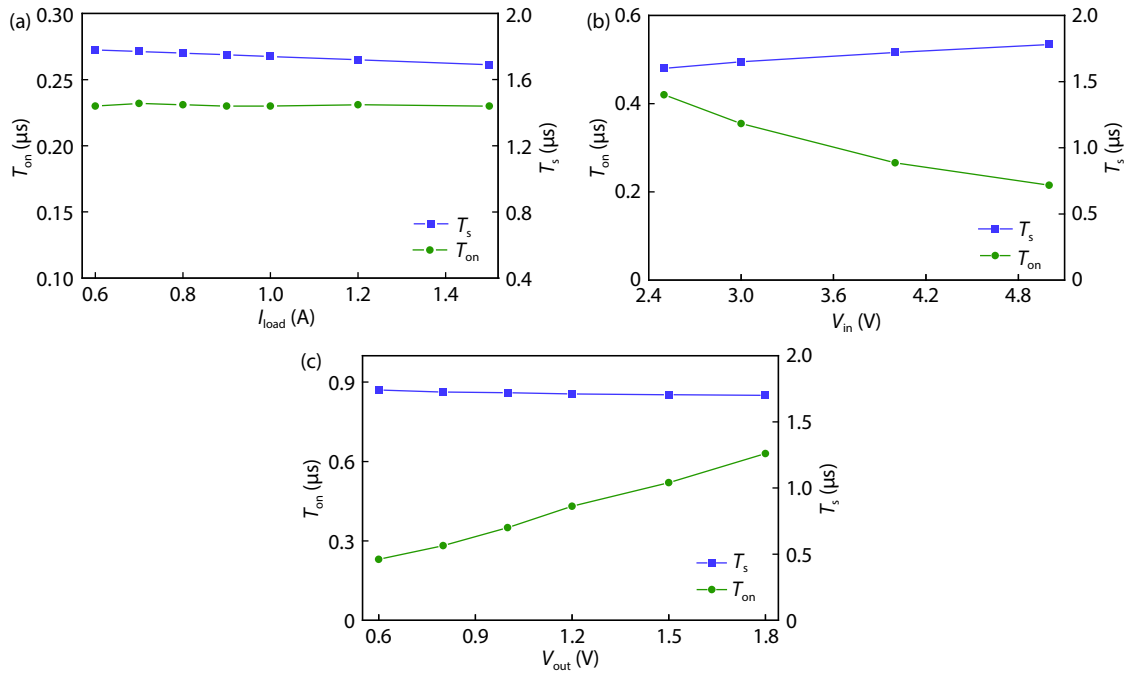


Fig. 6. (Color online) Simulation results of constant frequency. (a) Varying load current. (b) Varying input voltage. (c) Varying output voltage.

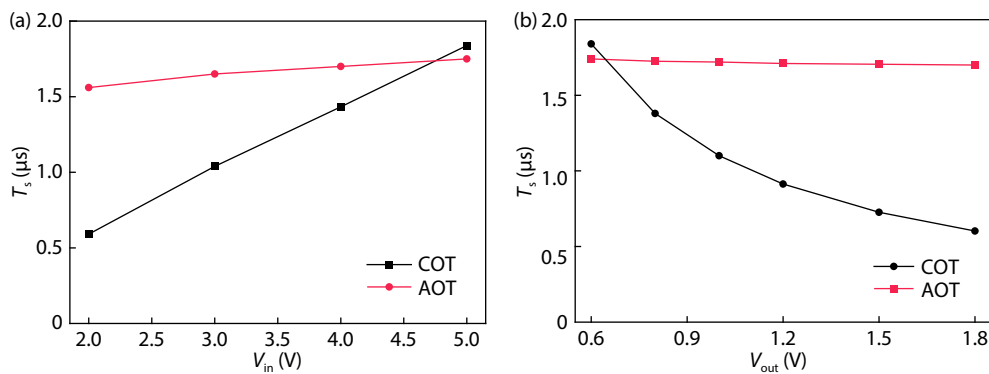


Fig. 7. (Color online) The relationship of T_s between traditional COT and AOT structure proposed in this paper. (a) Variable input voltage. (b) Variable output voltage.

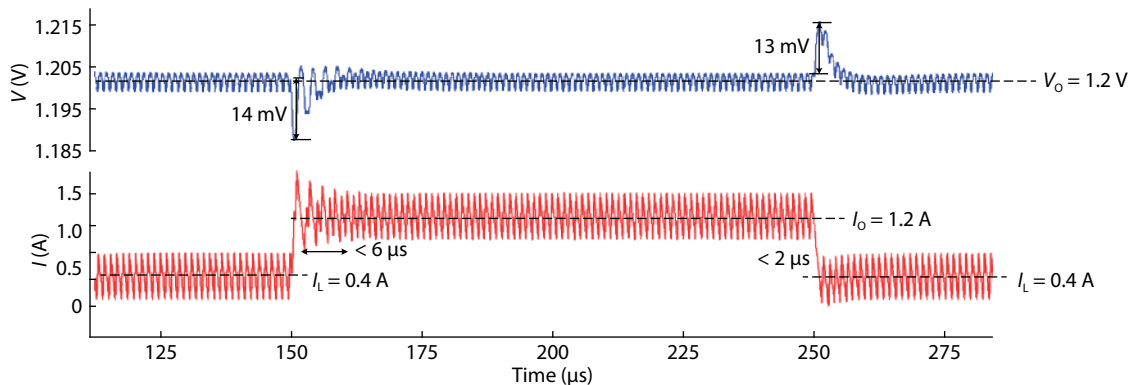


Fig. 8. (Color online) Simulated load transient response (V_o : 1.2 V, I_L : 0.4 A \rightarrow 1.2 A \rightarrow 0.4 A).

also obtained as expected. The ripple voltage is higher with a lower load current because the ripple voltage is inversely proportional to the switching frequency.

3.4. Conversion efficiency

The power efficiency is simulated versus the load cur-

rent and the output voltage as shown in Fig. 10. The peak power efficiency is 95.5% when the load current is 0.95 A and the output voltage is 1.8 V. As can be seen from the figures, the overall trend of the conversion efficiency increases first and then decreases. The load currents corresponding to the broken lines in Fig. 10 indicate that the critical current is

Table 1. Comparison results of transient performance between COT, PWM and AOT.

Control technique	Input voltage (V)	Output voltage (V)	Normalized voltage drop	Normalized voltage overshoot	Normalized setting cycle
Load step variation from 1 to 2 A					
COT-DPV ¹	5	1.5	0.78	0	0.81
PWM-DPV	5	1.5	1	0.36	1
AOT	5	1.5	0.58	0	0.25
Load step variation from 2 to 1 A					
COT-DPV	5	1.5	0	1.53	0.826
PWM-DPV	5	1.5	0.43	1	1
AOT	5	1.5	0	0.56	0.188

¹DPV: digital peak voltage

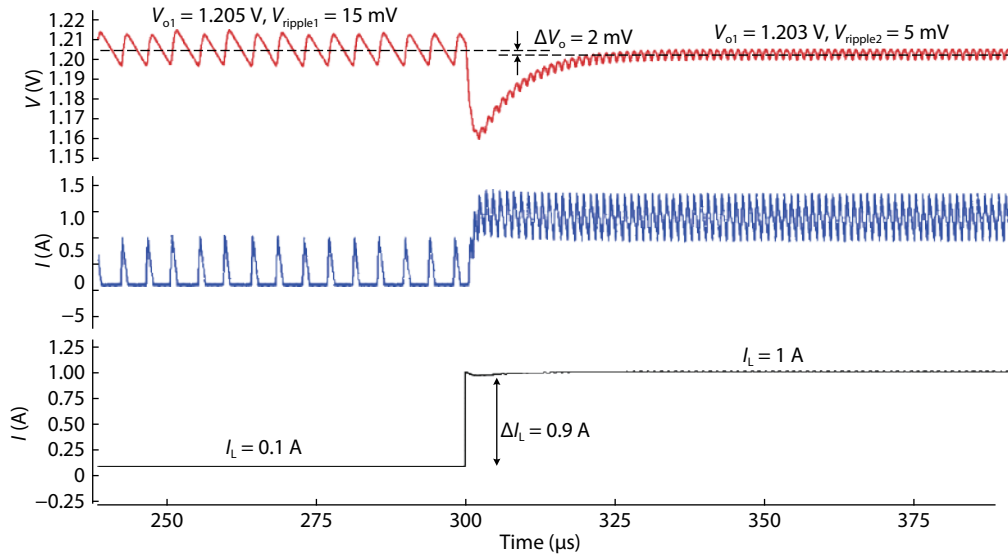


Fig. 9. (Color online) Output variation curve caused by load current variation.

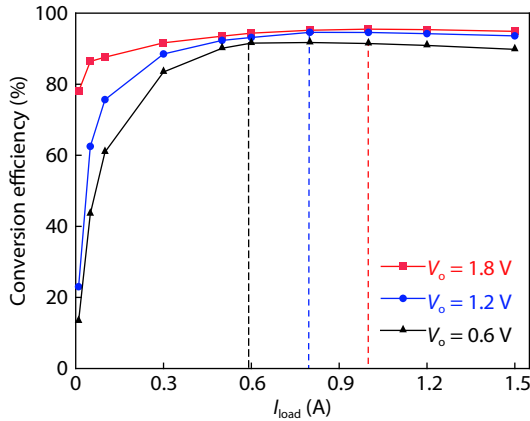


Fig. 10. (Color online) Conversion efficiency versus load current at different output voltages.

related to different output voltages. The crossover losses between the two switches are the main factors of the efficiency losses under light load current conditions which is because the moment when the P switch is turned off, the current flowing through it cannot fall to zero immediately and there is a voltage drop across the P switch, resulting in extra power loss in the case where current and voltage both exist. Meanwhile, there are similar power loss on the N switch.

When the load current is reduced to make the converter enter DCM, the conversion efficiency can still maintain a high level over a large load range, especially when the output

voltage is higher than 1.8 V. Until the current drops below about 0.1 A, the conversion efficiency drops significantly. The smaller the output voltage, the more obvious the trend. Under extremely light load conditions, the efficiency is greatly reduced due to the increasing proportion of quiescent current. To offset the switching loss, lower switching frequencies are adopted in DCM.

The maximum conversion efficiency under different control methods are further compared in Table 2. The maximum conversion efficiency of AOT can reach 95.5% when the output voltage is 1.8 V. As the output voltage decreasing, the conversion efficiency decreases slightly. The maximum conversion efficiency is about 92% with 0.6 V output voltage. The light load efficiency of the traditional PWM control mode can only reach about 20% while the efficiency of this AOT structure can reach 40% or more. Consequently, the conversion efficiency, especially the conversion efficiency under light load is improved. The performance summary of this design is presented in Table 3.

4. Conclusion

An adaptive-on-time valley current mode controlled buck converter with characteristics of constant frequency in CCM and variable frequencies in DCM is proposed for the application of wide current range and high power efficiency. The proposed converter is designed in standard 0.18 μm process, and composed of power and feedback control stages.

Table 2. Comparison results of different control methods.

Control technique	PWM/PFM ^[1]	PWM ^[26]	DLL ^[27]	SAW ^[28]	CTDT ^[29]	This work
Result	Simulation	Measure	Measure	Measure	Measure	Simulation
Process (μm)	0.35	0.13	0.5	0.35	0.25	0.18
V_{in} (V)	3.3–5	1.2	4.8	3.3	5	5
V_{o} (V)	0.5–3.0	0.6–1.05	3.3	0.3–2.5	1.5	1.8
Peak efficiency (%)	90	82.4	83	88.1	90.2	95.5
Inductor (μH)	500–3000	0.003–0.008	0.11–0.22	0.22	2.2	1.5
Output capacitor (μF)	50–200	0.00373	0.008–0.19	2.5	6	20
f_{sw} (MHz)	0.5–2.1	100	~30	25	0.5	1

Table 3. Performance summary.

Parameter	Value
Process	Standard 0.18 μm process
Supply voltage	3.3–5.0 V
Output voltage	0.6–3.0 V
Switching frequency	1 MHz
Load current	50–2000 mA
Inductor	1.5 μH
Output capacitor/ESR	20 μF /1 m Ω
Maximum Efficiency	95.5%
Load regulation rate	0.19%/A

First, this circuit can not only solve the problem caused by changing frequency of the traditional COT method but can also improve the conversion efficiency under light load compared with the PWM control mode. Second, it can operate stably under different conduction modes and transform freely without introducing large undershoot voltage and response time. The increase in the allowable output range and effective control of the voltage undershoot make the design of subsequent circuits less difficult. In addition, due to the introduction of variable frequency control in DCM, the overall switching efficiency is greatly improved. Simulation results show that the peak conversion efficiency can reach 95% with 1.8 V output in a large load current range. Besides, the efficiency can be improved as the voltage rises within a certain range, which is more suitable for battery supplied systems.

Acknowledgments

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