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A 0.1–1.5 GHz multi-octave quadruple-stacked CMOS power amplifier

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Abstract: In this letter, we design and analyze 0.1–1.5 GHz multi-octave quadruple-stacked CMOS power amplifier (PA) in 0.18 μm CMOS technology. By using two-stage quadruple-stacked topology and feedback technology, the proposed PA realizes an ultra-wideband CMOS PA in a small chip area. Wideband impedance matching is achieved with smaller chip dimension. The effects of feedback resistors on the RF performance are also discussed for this stacked-FET PA. The PA shows measured input return loss (< –10.8 dB) and output return loss (< –9.6 dB) in the entire bandwidth. A saturated output power of 22 dBm with maximum 20% power added efficiency (PAE) is also measured with the drain voltage at 5 V. The chip size is 0.44 mm^2 including all pads.

Key words: power amplifier; CMOS; stacked; multi-octave; resistive matching

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1. Introduction

Modern wireless communication systems working in 0.1–1.5 GHz have recently been developed, such as industrial scientific and medical (ISM), enterprise network, space and so on, which results in the desirability of a single chip CMOS transceiver to urgently reduce the overall cost. As a key component in the RF transceiver, there are still many challenges for the CMOS power amplifier (PA) design, which are mainly caused by the low breakdown voltage and lossy on-chip passive elements[1, 2].

In the ultra-broadband PA design, the common problem is that the optimum impedance varies as the frequency changes[3–5], which consequently makes it hard to realize a proper matching network and broaden bandwidth. A series of broadband impedance matching theories and techniques have been reported, including transformer-based matching network[4], differential distributed structure[6], LC filtering matching method[7], resistive feedback and transformer matching network[8], Darlington cascode topology and series peaking RL circuit method[9]. Nevertheless, due to the introduction of external components, including the on-chip passive inductor and transformer, the chip area has become unavoidably larger, especially when the design frequency range is located between 0.1–1.5 GHz. Thus, to cover this band, a novel matching approach is acquired to introduce fewer external components.

To solve these problems, stacked power amplifiers have become a popular choice in recent years. The transistors involved in this structure have the same current and superimposed voltage, and increasing the output voltage swing. The structure also enlarges the output impedance, which makes the broadband output matching easier. However, the input impedance remains nearly constant and requires additional matching[10–12]. Besides, the drain supply of each layer is superimposed to become the total supply voltage of the stacked amplifiers, thus the stacked structure requires a high supply voltage.

In this letter, a two-stage ultra-wideband stacked-FET PA in GLOBALFOUNDRIES 0.18-μm CMOS technology has been designed with a small chip dimension. Over 0.1 to 1.5 GHz, the saturated output power (P_{sat}) is about 22 dBm. Up to 20% PAE is acquired and the input VSWR is below 2 : 1.

2. Circuit design

2.1. The biasing condition of FETs

The biasing condition of FETs is one of the top priorities in circuit design. As the transistor and the working condition are determined, especially for the case of saturation condition, the drain current simply depends on the V_{gs}, when $V_{ds} > V_{sat}$ is satisfied.

The optimum load impedance Z_{opt} of the transistor is limited by the biasing condition. For the whole N-stacked FETs structure, the total optimal load impedance of the structure is $N \times Z_{opt}$. This means that we can control the optimum load impedance by adjusting the drain bias voltage. For the quadruple-stacked structure in this letter, to connect 50 Ω load directly without matching network, the total optimal load impedance of the second stage should be set at 12.5 Ω (4 × 12.5 = 50 Ω).

2.2. The impact of feedback resistor on input and output impedance

Fig. 1 shows an equivalent AC circuit model of a quad-

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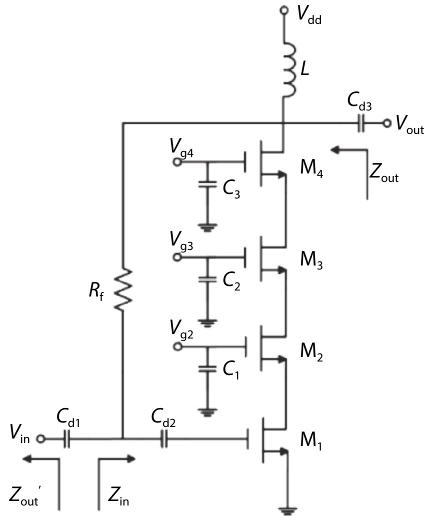

Fig. 1. The equivalent AC circuit.

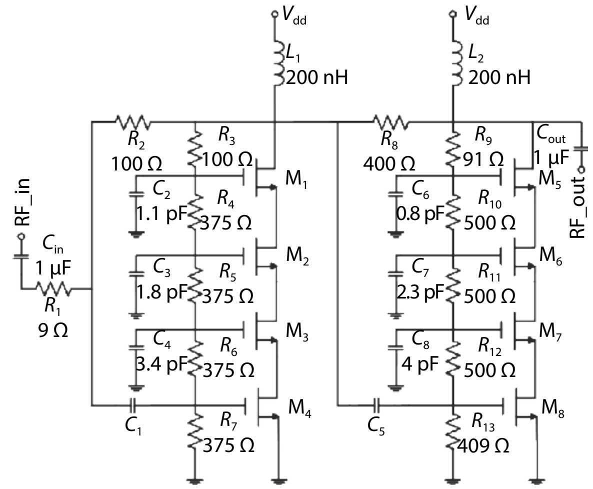

Fig. 2. Schematic of proposed PA.

ruple-stacked power amplifier. The structure mainly consists of four transistors (M_1, M_2, M_3, M_4) and capacitance C_1, C_2, C_3. C_{d1}, C_{d2}, C_{d3} are DC blocking capacitors, and R_f is a feedback resistor connected between the gate of M_1 and the drain of M_4.

As shown in Fig. 1, the transconductance g_{mstack} of the stacked PA can be derived as[13]:

$$g_{mstack} = \frac{g_{m1}}{\left(1+\dfrac{sC_{gs2}}{g_{m2}}\right)\left(1+\dfrac{sC_{gs3}}{g_{m3}}\right)\left(1+\dfrac{sC_{gs4}}{g_{m4}}\right)}. \tag{1}$$

Based on Refs. [14, 15], the closed-loop voltage gain A_v of the resistive negative feedback circuit can be derived as:

$$A_v = \frac{Z_L + g_{mstack}R_f Z_L}{Z_L - R_f}, \tag{2}$$

where Z_L is the 50 Ω output load impedance of the PA. The input impedance Z_{in} combined with the negative feedback structure can be derived based on Eq. (2).

$$Z_{in} = \frac{R_f}{j\omega C_{gs1}R_f + A_v - 1}, \tag{3}$$

where C_{gs1} is the gate-to-source capacitance, and the output impedance Z_{out} of the PA is:

$$Z_{out} = \frac{R_f + Z_{out'}}{1 + g_{mstack}Z_{out'}}. \tag{4}$$

Therefore, based on Eqs. (3) and (4), the feedback resistor affects the input and output impedance, by optimizing the feedback resistor R_f, the input and output impedance can be set at a value approached to 50 Ω in the specific frequency band.

2.3. The quadruple-stacked structure

The circuit topology in this design is shown in Fig. 2, and the power stage is made up of transistor M_5, M_6, M_7 and M_8, which is connected in series. To enhance the output power, a larger voltage swing is acquired, and thus a two-stage quadruple-stacked FETs structure is employed. The drain current is the same through each transistor, and the total drain bias voltage is superimposed. The gate bias voltage for each layer is obtained by dividing the supply voltage through resistors R_9, R_{10}, R_{11}, R_{12} and R_{13}. It is worth noting that a larger magnitude of impedance needs to be selected for the divider resistance to reduce the quiescent current and power consumption. To adjust the drain output impedance and signal of each layer, the grid voltage of the transistor in each layer is connected to a ground capacitor, forming an AC voltage divider structure with the gate-source capacitor. A feedback resistor R_8 is added to improve circuit stability. C_5 is used as DC-block between the two stages. The driver stage and power stage are set to be same structure. The input matching network consists of resistors R_1, R_2 and capacitance C_1, which aims to improve the stability and ensure the gain flatness of the circuit. Eight transistors are required in the circuit, M_1–M_8 are thick gate transistor. The width/length of M_1–M_2 is 1200 μm/0.35 μm, and the width/length of M_3–M_8 is 1600 μm/0.35 μm.

Moreover, the impedance for each transistor is affected by the phase-adjusting capacitances (C_2–C_4, C_6–C_8) and gate-to-source capacitance (C_{gs}) of each FET simultaneously. The key factor to build a 50 Ω stacked FETs is to realize the same transistor size, the same gate to source bias controlled by the voltage-dividing resistors, the same phase of RF voltage controlled by the phase-adjusting capacitances. In consideration of the potentially instability with lower drain voltage, the resistors in the circuit should be optimized to ensure *K*-factor greater than 1. The broadband input matching is obviously obtained by the resistor R_1, R_2 and R_8. R_1 can improve the matching results but decrease the gain of the circuit. The bandwidth response, input and output return loss, power gain and PAE of the circuit is mainly affected by R_2 and R_8.

Figs. 3 and 4 show the method of adjusting the value of R_2 to balance various indexes. As shown in the figures, when the values of R_2 reach 200 Ω, the simulated results of S_{11}, S_{21} and S_{22} are better than those in 100 and 300 Ω in 0.1–1.5 GHz. 22.3 dBm output power with 20.8% PAE at 0 dBm input power are acquired in post-layout simulation. Obviously, 200 Ω is the more reasonable value in the topology.

3. Experimental results

To verify the post-layout simulation results, the PA was fabricated as shown in Fig. 5. The total dimension of the chip

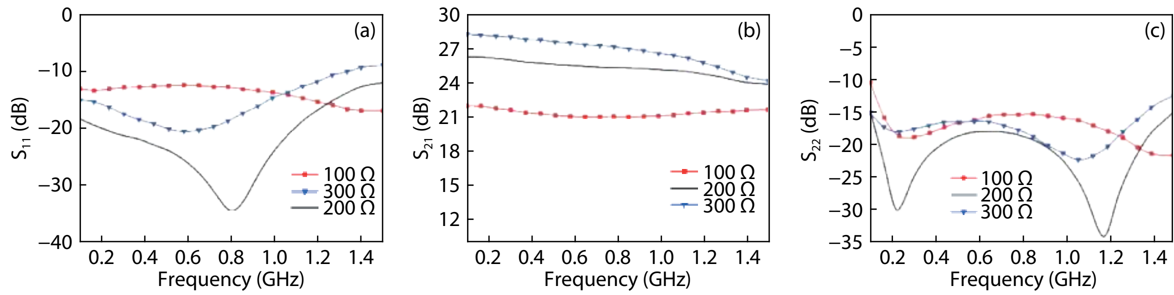

Fig. 3. (Color online) Effects of R_2 on S-parameter. (a) S_{11}. (b) S_{21}. (c) S_{22}.

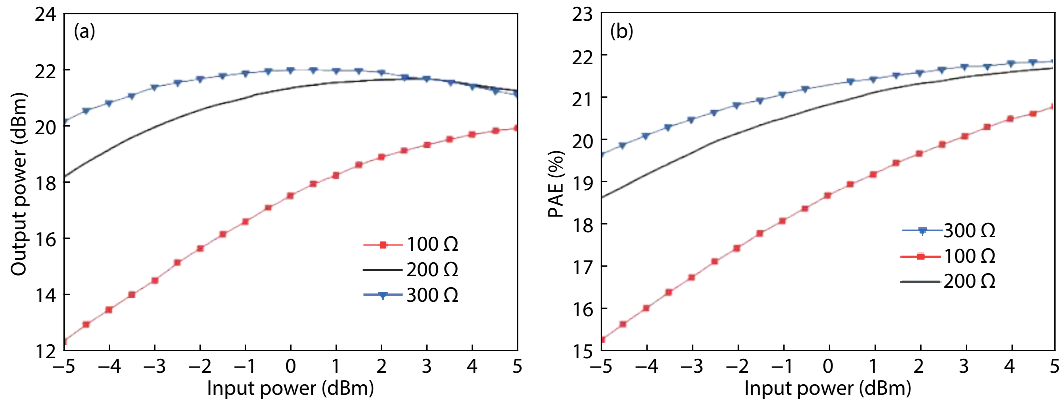

Fig. 4. (Color online) Effects of R_2 on output power and PAE (post-layout simulation). (a) Output power. (b) PAE

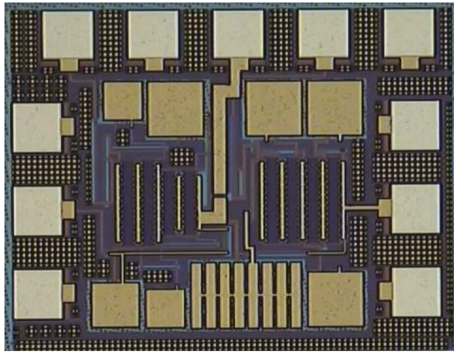

Fig. 5. (Color online) Microphotograph of the stacked PA.

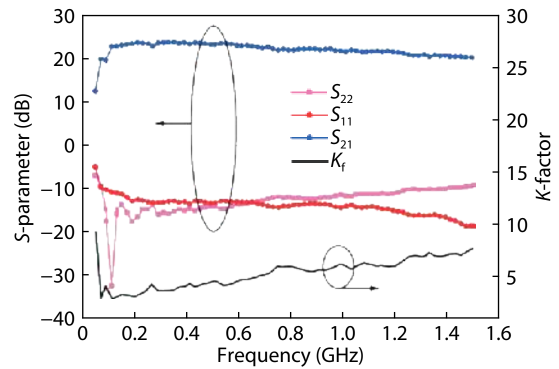

Fig. 7. (Color online) K-factor and S-parameters.

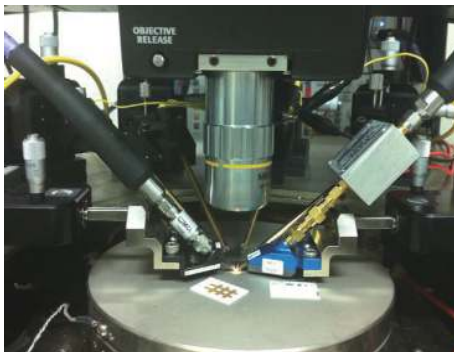

Fig. 6. (Color online) Photograph of the test system.

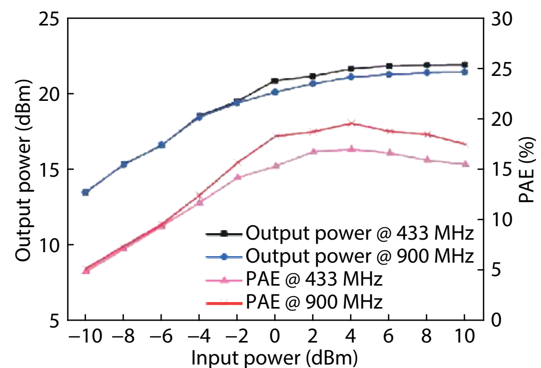

Fig. 8. (Color online) Output power and PAE.

is 0.58 × 0.76 mm^2 with bond pad. The testing system of the fabricated PA is shown in Fig. 6. Using bias-tees at the drain of two stages to provide the supply voltage. And the chip is tested on a probe station. Through a R&S ZVA40 network analyzer, the data of S_{11}, S_{21}, S_{22} is acquired. Measurement of the output power is accomplished by the R&S FSV40 frequency analyzer.

As shown in Fig. 7, the S scattering parameter and stability factor of the fabricated PA are measured. The minimum value of the measured K-factor is larger than 1, which means global stability of the circuit in the entire bandwidth.

Table 1. Performance of Broadband CMOS PAs.

Parameter	Ref. [4]	Ref. [6]	Ref. [7]	Ref. [8]	This work
Technology	90 nm	0.6 μm	0.18 μm	0.18 μm	0.18 μm
Frequency (GHz)	5.2–13	0.5–8.5	3.1–9	1–5	0.1–1.5
S_{11} (dB)	< –11	< –6	< –9	< –5	< –10.8
S_{22} (dB)	< –3.9	< –9.5	< –8	<–4	< –9.6
Gain (dB)	14	6	10	15 – 20	22.3 ± 1.5
OP_{1dB} (dBm)	22.6	–	6	20	21
Power (mW)	181	–	0	100	126
Peak PAE (%)	21.6	–	–	36	20
Area (mm²)	0.45 × 1.55	1.3 × 2.2	1.1 × 1	0.9 × 0.76	0.58 × 0.76

Table 2. Power consumption of each stage.

P_{in} (dBm)	V_{ds1} (V)	I_{ds1} (mA)	V_{ds2} (V)	I_{ds2} (mA)
–2	5	47	5	107
0	5	46	5	106
2	5	49	5	105
4	5	53	5	101

In the range of 0.1–1.5 GHz, the measured S_{11} (< –10.8 dB), S_{21} (22.3 ± 1.5 dB) and S_{22} (< –9.6 dB) indicate a feature of wide bandwidth, and shows a good gain flatness. Fig. 8 displays 22 dBm of saturated P_{out} and 20% peak PAE, respectively.

A comparison of performance indices reported in the literature with state-of-the-art is given in Table 1.

Compared with Ref. [4] and Ref. [8], the proposed PA shows a lower PAE based on the power consumption of each stage, as shown in the Table 2. The reason is that the first stage of the PA consumes more power than expected, which decreases the efficiency of the circuit.

Nevertheless, his work achieves a good performance in gain and bandwidth with a smaller chip size.

4. Conclusion

In this letter, a novel circuit for a 0.1–1.5 GHz multi-octave PA in a small chip dimension was proposed. The combination of stacked structure and feedback resistors greatly enhance the bandwidth of the circuit. Meanwhile, the dimension of the chip is also decreased by resistive matching networks. Our measurement results show that greater than 22 dBm output power from 0.1 to 1.5 GHz, and 20% peak PAE was realized, a gain flatness of 22.3 ± 1.5 dB was measured. This indicates that the proposed structure is suitable for low-breakdown voltage CMOS process in the ultra-broadband PA.

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