ARTICLES

Journal of Semiconductors
(2020) 41, 032102
doi: 10.1088/1674-4926/41/3/032102

Small-signal modeling and parameter extraction method for a multigate GaAs pHEMT switch

Lin Luo, Jun Liu†, Guofang Wang, and Yuxing Wu

Key Laboratory of RF Circuits and Systems, Ministry of Education, Hangzhou Dianzi University, Hangzhou 310018, China

Abstract: This paper presents an accurate small-signal model for multi-gate GaAs pHEMTs in switching-mode. The extraction method for the proposed model is developed. A 2-gate switch structure is fabricated on a commercial 0.5 μm AlGaAs/GaAs pHEMT technology to verify the proposed model. Excellent agreement has been obtained between the measured and simulated results over a wide frequency range.

Key words: GaAs pHEMTs; switch; small-signal model; parameter extraction

Citation: L Luo, J Liu, G F Wang, and Y X Wu, Small-signal modeling and parameter extraction method for a multigate GaAs pHEMT switch[J]. *J. Semicond.*, 2020, 41(3), 032102. http://doi.org/10.1088/1674-4926/41/3/032102

1. Introduction

Currently, GaAs pHEMT switches play a more and more important role in RF switching and exhibit excellent performance in modern communication systems[1, 2]. Compared to traditional devices, GaAs pHEMT switches provide lower insertion loss, higher isolation, and a wider work frequency band. As the isolation and insertion loss requirements of switches for different circuits vary, multi-gate structures are also popularly used in designs.

Accurate device modeling is a very important part of the semiconductor industry. For HEMT devices, the related research and literature have become popular, but generally only for common-source structures[3–11]. However, much less research is related to the modeling of GaAs pHEMT switches[12–16]. GaAs pHEMT switches are common gate devices with a feature that distinguishes them from other structures. To prevent leakage of the RF signal, GaAs pHEMT switches are connected to a sufficiently large resistor at the gate. The parasitic environment of the GaAs pHEMT switches is different due to the unique structures; thus, the traditional small-signal model extraction method is no longer applicable. A simple topology cannot accurately describe the performance of a device with a high frequency[12]. The optimization-based extraction method is time consuming[13]. Several different researches have raised some issues that need to be considered in the modeling of GaAs pHEMTs[14–16]. The low-frequency dispersion effect due to surface traps has an effect on the gate capacitor, and the pulse method is effective in improving the modeling accuracy[14]. A significant effect of the precise multi-capacitive current path on the switch model precision has been found[15]. The gate leakage prevention resistors of the switching device contribute to the extraction of the gate capacitor[16]. Currently, there are many articles that mention the modeling of switches[12–16], but the detailed extraction process for a multi-gate structure is not developed.

This paper presents a direct extraction method for GaAs pHEMT switches with a model that can be extended to multi-gate devices. In Section 2, the devices involved in this work and the related measurement instruments are introduced. The extraction process of the external parasitic parameters and intrinsic capacitor is described in detail in Section 3. Section 4 presents a verification of the model and a comparison of the simulated and measured data. Finally, the conclusions of this paper are presented.

2. Devices and instruments

The GaAs pHEMT switches employed in this work include one switch with the normal common-gate GaAs pHEMT structure and a GaAs pHEMT switch whose gate is connected with a blocking resistor. In addition, the measured device includes a separate open structure for the extraction of the external parasitic capacitors. This device is grown on a 50 nm thick GaAs substrate as shown in Fig. 1, followed by a GaAs buffer layer to improve the effect of substrate defects of the channel. The channel is formed at the top of the InGaAs layer, and the electrons are provided by the upper AlGaAs layer. Ohmic contacts are created on the uppermost layer.

Fig. 2 shows the layout of the dual-gate GaAs pHEMT switch. The gate length of the GaAs pHEMT switch is 0.5 μm, the total width is 625 μm (125 μm $\times$ 5), whose number of fingers is 5 with 125 μm finger width. and the value of the resistor switch connected to the gate is 20 kΩ. The multi-gate device is extended with dual, triple and quadruple gates. An advanced measurement system is used to characterize the considered GaAs pHEMT switches. The instruments in the measurement system include: a Cascade probe station, which can support on-chip testing; an Agilent 4156C DC power supply to provide a specific bias voltage to operate the switch at a specific voltage; and a Keysight vector network analyzer (VNA) for the two-part *S* parameter measurements for the model extraction and verification at 20 GHz.

Correspondence to: J Liu, ljun77@hdu.edu.cn
Received 22 JULY 2019; Revised 20 OCTOBER 2019.

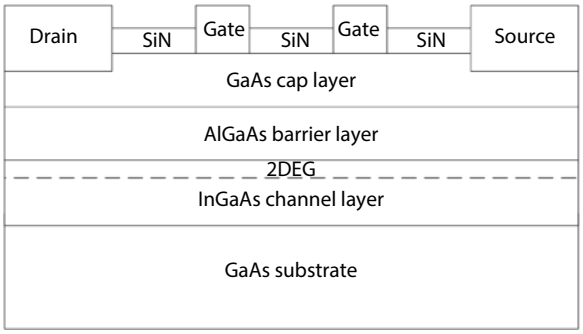

Fig. 1. Cross-sectional structure of the dual-gate GaAs pHEMT switch.

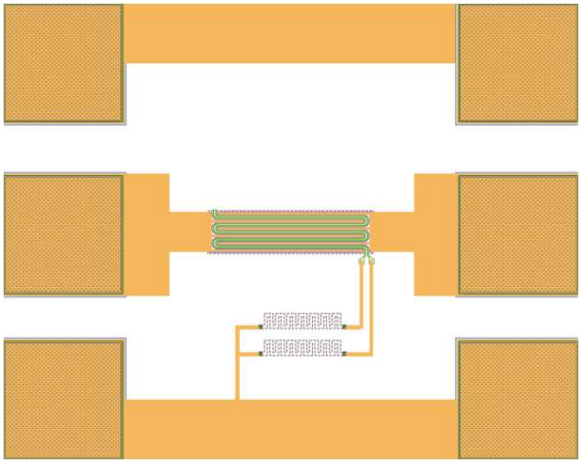

Fig. 2. (Color online) Layout of the dual-gate GaAs pHEMT switch (125 μm × 5).

3. Extraction procedure

In this paper, the intrinsic structure of a multi-gate device can be represented by a series connection of the intrinsic structure of single-gate switches[14]. A specific circuit is proposed in this work as shown in Fig 3. In this circuit, C_{dp} and C_{sp} are the parasitic capacitors due to the package effects, and R_{dp} and R_{sp} are the parasitic resistors due to the same effects. R_d, R_s, R_g, L_d, L_s and L_g account for the parasitic resistors and inductors due to the contacts with the drain, source and gate, respectively. Here, C_{gd}, C_{gs} and C_{ds} are the gate-to-drain capacitor, gate-to-source capacitor and drain-to-source capacitor, which are the intrinsic capacitors. R_{gd} and R_{gs} are chosen to control the voltage of C_{gs} and C_{gd}, which can improve the accuracy of parameter extraction at different voltages. R_{ds} represents the channel resistors between the drain and the source. R_G is a large resistor (20 kΩ) that can prevent the leakage of the RF signal. The source resistance to the inter-gate region R_m, the gate-to-gate coupling capacitor C_{gg*}, and the external capacitor between the drain and source C_{ds} are introduced.

It is of great importance to accurately extract the external parasitic parameters in the modeling of small-signal models. An incomplete or exaggerated removal of the extrinsic capacitors influences the subsequently extracted elements and thus introduces errors. From the paper[17], we know that the extraction of extrinsic parasitic capacitors is achieved mainly with the following two mainstream extraction methods: (1) the traditional cold-FET pinch extraction method[18] and (2) the open structure method[19]. Since the open structure has been designed, the open de-embedding method is used to extract the parasitic parameters. For the parasitic capacitor, the open structure has the same size as that of the extraction switch device. C_{dp} and C_{sp} are the parasitic capacitors of the pad to the ground, and C_{dsp} represents the parasitic capacitor between the two sides of the pad.

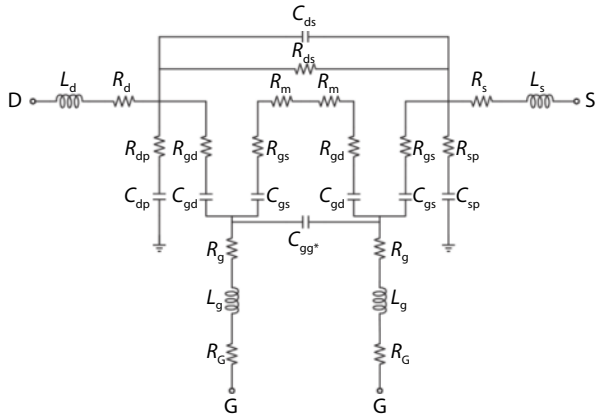

Fig. 3. Small-signal equivalent circuit of the dual-gate GaAs pHEMT switch.

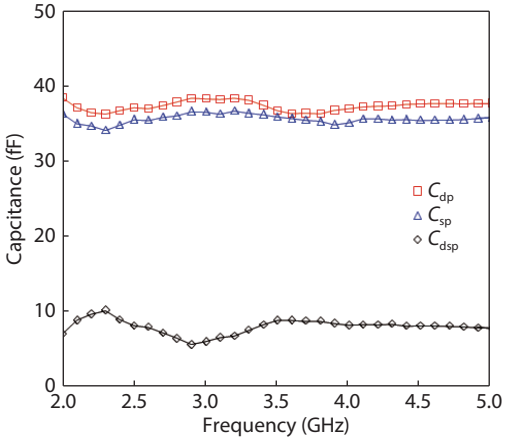

Fig. 4. (Color online) Extracted parasitic capacitances versus frequency.

The imaginary part of the *Y*-parameters can be expressed with the following formula:

$$\mathrm{Imag}\left(Y_{11}\right) = j\omega\left(C_{dp} + C_{dsp}\right), \tag{1}$$

$$\mathrm{Imag}\left(Y_{12}\right) = \mathrm{Imag}\left(Y_{21}\right) = -j\omega C_{dsp}, \tag{2}$$

$$\mathrm{Imag}\left(Y_{22}\right) = j\omega\left(C_{sp} + C_{dsp}\right), \tag{3}$$

$$C_{dp} = \mathrm{Imag}\left(Y_{11} + Y_{12}\right)/\omega, \tag{4}$$

$$C_{sp} = \mathrm{Imag}\left(Y_{22} + Y_{12}\right)/\omega, \tag{5}$$

$$C_{dsp} = -\mathrm{Imag}\left(Y_{12}\right)/\omega. \tag{6}$$

The extracted parameters via Eqs. (1)–(6) are shown in Fig. 4.

After de-embedding the effect of the pad parasitic capacit-

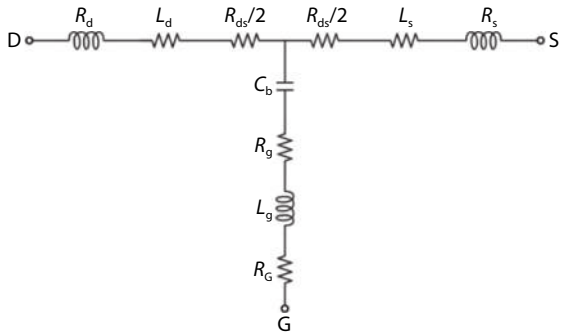

Fig. 5. Equivalent circuit of the GaAs pHEMT switch under the condition (V_{ds} = 0 V, V_{gs} = 0 V).

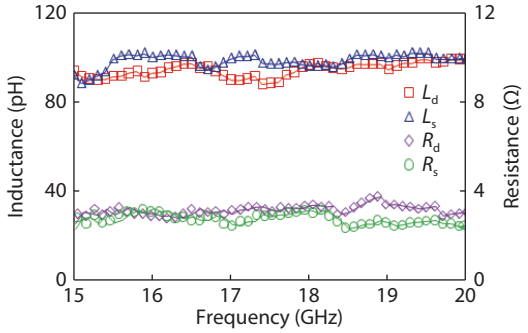

Fig. 6. (Color online) Extracted parasitic inductors versus frequency.

ors, the other parasitic parameters can be extracted from the *Z*-parameters under the condition (V_{ds} = 0 V, V_{gs} = 0 V). The equivalent topology is shown in Fig. 5. R_d, R_s and R_g are the parasitic resistors. L_d, L_s and L_g represent the parasitic inductors. R_{ds} is the channel resistors, and C_b represents the effect of the gate capacitors, including C_{gs}, C_{gd} and C_{gg*}.

The *Z*-parameters can be expressed as the following formula:

$$Z_{11} = R_d + \frac{R_{ds}}{2} + R_g + R_G + j\left[\omega\left(L_g + L_d - \frac{1}{\omega C_b}\right)\right], \quad (7)$$

$$Z_{12} = Z_{21} = R_g + R_G + j\left[\omega\left(L_g - \frac{1}{\omega C_b}\right)\right], \quad (8)$$

$$Z_{22} = R_s + \frac{R_{ds}}{2} + R_g + R_G + j\left[\omega\left(L_g + L_s - \frac{1}{\omega C_b}\right)\right]. \quad (9)$$

Since the blocking resistor R_G = 20 kΩ prevents the leakage of RF signal, L_g and R_g can be ignored. The extracted parameters are shown in Fig. 6.

After all of the external parasitic parameters have been removed, the intrinsic parameters can be accurately extracted. However, the gate is equivalent to an open circuit to the ground because the resistor R_G prevents the leakage of RF signal. For this case, the equivalent circuit is shown in Fig. 7.

Because the depletion layer under the gate is symmetric, it can be assumed that:

$$C_{gd} = C_{gs} = C_g, \quad R_{gd} = R_{gs} = R_{gds}. \quad (10)$$

R_m is small enough to be ignored. At this time, the *Y*-parameters are expressed as follows:

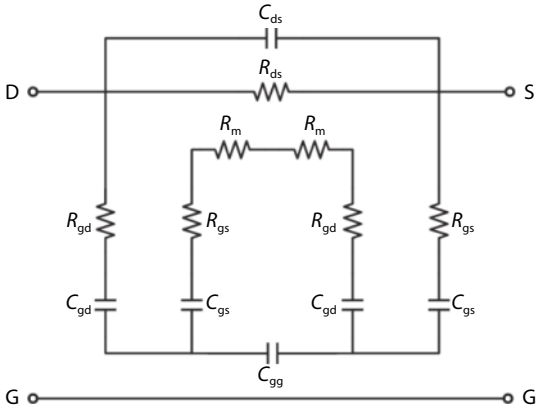

Fig. 7. The intrinsic part with R_G, which blocks the RF signal.

$$Y_{11} = \frac{1}{R_{ds}} + j\omega C_{ds} + Y_{tmp}, \quad (11)$$

$$Y_{12} = Y_{21} = -\frac{1}{R_{ds}} - j\omega C_{ds} - Y_{tmp}, \quad (12)$$

$$Y_{22} = \frac{1}{R_{ds}} + j\omega C_{ds} + Y_{tmp}. \quad (13)$$

Y_{tmp} represents the intermediate variable of the admittance, and the specific form is as follows:

$$Y_{tmp} = \frac{1}{2R_{gds} + \frac{1}{2j\omega C_g} + \frac{\left(2R_{gds} + \frac{1}{2j\omega C_g}\right)\frac{1}{j\omega C_{gg*}}}{\left(2R_{gds} + \frac{1}{2j\omega C_g}\right) + \frac{1}{j\omega C_{gg*}}}}. \quad (14)$$

It can be obtained that:

$$Y_{11} = -Y_{12} = -Y_{21} = -Y_{22}. \quad (15)$$

Obviously, the intrinsic parameters cannot be extracted. Because the channel carrier under the gate is depleted in the deep-off-state, the intrinsic capacitors are mainly the fringe capacitance. The intrinsic capacitors (C_{gs}, C_{gd} and C_{ds}) should be extracted from the GaAs pHEMT switch without the gate resistor R_G. The device behaves as a common-gate structure of a pHEMT. With the effect of the inductor being ignored at low frequencies, considering only the imaginary part of the *Y*-parameter, the equivalent circuit is expressed as follows:

$$\mathrm{Imag}\left(Y_{11}\right) = j\omega\left(C_{gd} + C_{ds}\right), \quad (16)$$

$$\mathrm{Imag}\left(Y_{12}\right) = \mathrm{Imag}\left(Y_{21}\right) = -j\omega C_{ds}, \quad (17)$$

$$\mathrm{Imag}\left(Y_{22}\right) = j\omega\left(C_{gs} + C_{ds}\right). \quad (18)$$

The extracted results via Eqs. (16)–(18) are shown in Fig. 8.

Under the same conditions, the channel resistors are extracted by the real part of the *Y*-parameter:

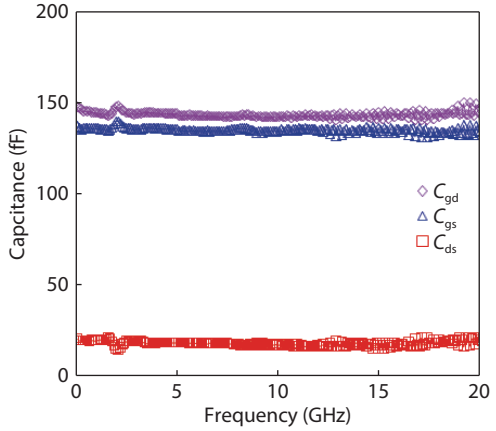

Fig. 8. (Color online) Intrinsic capacitances versus frequency for the common-gate GaAs HEMT without R_G.

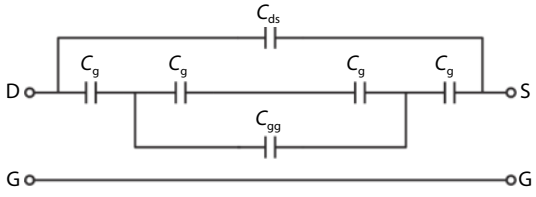

Fig. 9. Equivalent circuits of the dual-gate GaAs pHEMT switch.

Table 1. Intrinsic elements of the GaAs HEMT switch with a gate size of 5 × 125 μm.

State	C_{gd}	C_{gs}	C_{ds}	C_{gg*}	R_{ds}
On state	1.5 pF	1.5 pF	20.1 fF	74.2 fF	4.5 Ω
Off state	145 fF	137 fF	20.1 fF	64 fF	96 kΩ

$$\mathrm{Real}\,(Y_{21}) = -\frac{1}{R_{ds}}. \tag{19}$$

It is worth mentioning that the gate-to-gate capacitor C_{gg*} is adjusted to fit the off-state capacitor values. After all of the external parasitic parameters have been removed, considering only the imaginary part of the *Y*-parameter at low frequencies, the equivalent topology of the capacitors can be expressed as Fig. 9. The gate is equivalent to an open circuit to the ground. In the above extraction process, $C_{gs} = C_{gd} = C_g$ is verified. Therefore, the imaginary part of Y_{11} can be derived as fellow:

$$\mathrm{Imag}\,(Y_{12}) = -j\omega\left(C_{ds} + \frac{\frac{1}{2}C_{g^*}\left(\frac{1}{2}C_g + C_{gg^*}\right)}{\frac{1}{2}C_g + \left(\frac{1}{2}C_g + C_{gg^*}\right)}\right). \tag{20}$$

C_{gg*} can be accurately extracted because C_g and C_{ds} have been extracted from common-gate HEMTs.

Since all the extrinsic parasitic parameters are accurately extracted, the extracted intrinsic parameters hardly change with frequency. Table 1 summarizes the selection of the extracted values for the on and off states. So far, all the parameters of the dual-gate switch are extracted completely, and the verification of the model is discussed in the next section.

4. Model verification

The above extraction method is applied to extract the parameters of a GaAs HEMT switch with a measurement frequency range extending from 100 MHz to 20 GHz. Devices with dual, triple and quadruple gates are verified, considering a gate length of 0.5 μm and a gate total width of 625 μm (125 μm × 5). The fitting results of the GaAs HEMT switches are shown in Table 2.

Table 2. Intrinsic parameters of GaAs HEMT switches with different gates.

Gate	Dual	Triple	Quadruple
C_{ds}(on) (fF)	20.1	15.21	11
C_{gs}(on) (pF)	1.5	2.12	2.82
C_{gd}(on) (pF)	1.5	2.15	2.73
R_{ds}(on) (Ω)	4.5	5.76	7
C_{ds}(off) (fF)	20.1	15.21	11
C_{gs}(off) (fF)	137	144	152
C_{gd}(off) (fF)	145	148	161
R_{ds}(off) (kΩ)	96	182	160
C_{gg*}(off) (fF)	64	76.27	121.6

Table 3. The error percentage of GaAs HEMT switches with different gates.

Gate	Dual	Triple	Quadruple
S_{11}(off)	0.7586	0.909	1.131
S_{12}(off)	2.519	2.294	1.981
S_{21}(off)	2.412	2.378	2.066
S_{22}(off)	1.362	2.518	1.746
S_{11}(on)	2.257	2.477	2.197
S_{12}(on)	1.157	2.285	2.805
S_{21}(on)	0.7694	0.6054	0.604
S_{22}(on)	2.2924	1.201	0.573

Fig. 10 shows a comparison of the *S*-parameters between the simulation and the measurement of the on and off states in Smith charts. The agreements between the measured and simulated data are excellent over a wide frequency range.

The error formulations can be expressed using the following equations:

$$e = \frac{|S_{simu}(i) - S_{meas}(i)|}{\sqrt{\frac{\sum_n (S_{meas}(i))^2}{n}}}, \tag{21}$$

where S_{simu} and S_{meas} represent the simulated and measured data sets, and n is the number of data points included in each data set. Table 3 shows the error percentage of different devices. The verification and accuracy are guaranteed. The percentage errors between the measured and simulated data are within 3%. Table 3 shows the different errors of each device.

The insertion loss and isolation results of the GaAs pHEMT multi-gate switch with a gate total width of 5 × 125 μm are shown in Fig. 11. The results of the modeling procedure fit the measurements well up to 20 GHz.

5. Conclusion

A small-signal equivalent circuit for multi-gate GaAs pHEMTs in RF switching mode is proposed, and a direct extraction method is developed. By comparing the measured *S*-parameters with the model simulation results, it is found that the

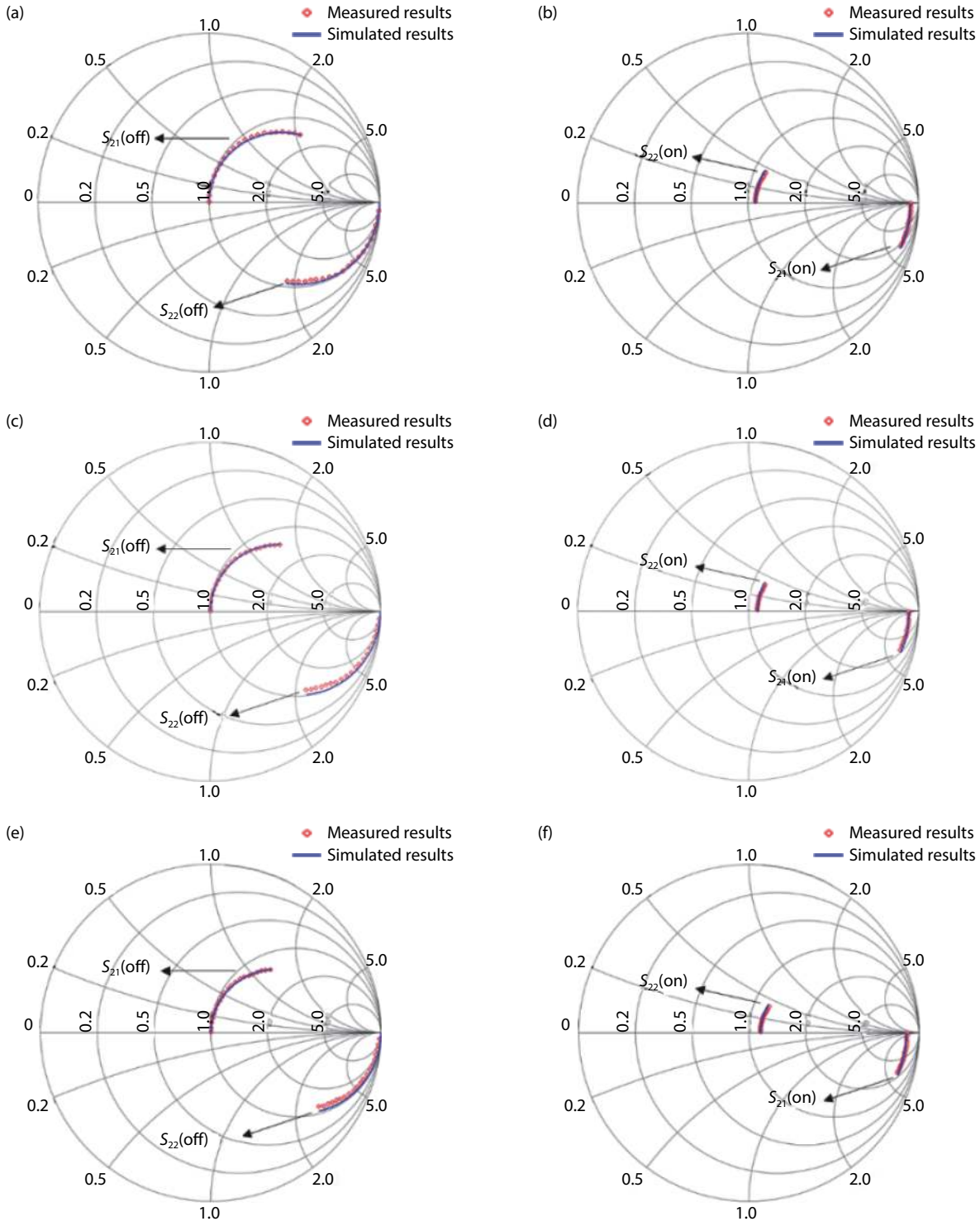

Fig. 10. (Color online) Comparison of the *S*-parameters between the simulation (-) and measurement (◇) over a frequency range of 0.1–20 GHz for a device with size of 5 × 125 μm: (a) dual-gate off state, (b) dual-gate on state, (c) triple-gate off state, (d) triple-gate on state, (e) quadruple-gate off state, and (f) quadruple-gate on state.

model provides high accuracy and strong reliability. Good fitting results for different gates also confirm the scalability of the extraction method. This extraction method can be applied to multi-gate GaAs pHEMT switch devices.

References

[1] Tosaka H, Fujii T, Miyakoshi K, et al. An antenna switch MMIC using E/D mode p-HEMT for GSM/DCS/PCS/WCDMA bands application. IEEE MTT-S International Microwave Symposium Digest, 2003, 519

[2] Chiu H C, Cheng C S, Wu C S. Enhancement-and depletion-mode InGaP/InGaAs pHEMTs on 6-inch GaAs substrate. 2005 Asia-Pacific Microwave Conference Proceedings, 2005, 4

[3] Khusro A, Hashmi M S, Ansari A Q, et al. An accurate and simplified small signal parameter extraction method for GaN HEMT. Int J Circuit Theory Appl, 2019, 47(6), 941

[4] Chen Y, Xu Y, Luo Y, et al. A reliable and efficient small-signal parameter extraction method for GaN HEMTs. Int J Numer Model: Electron Networks, Devices Fields, 2018, e2540

[5] Bilevich D V, Popov A A, Salnikov A S, et al. Automatic nonlinear

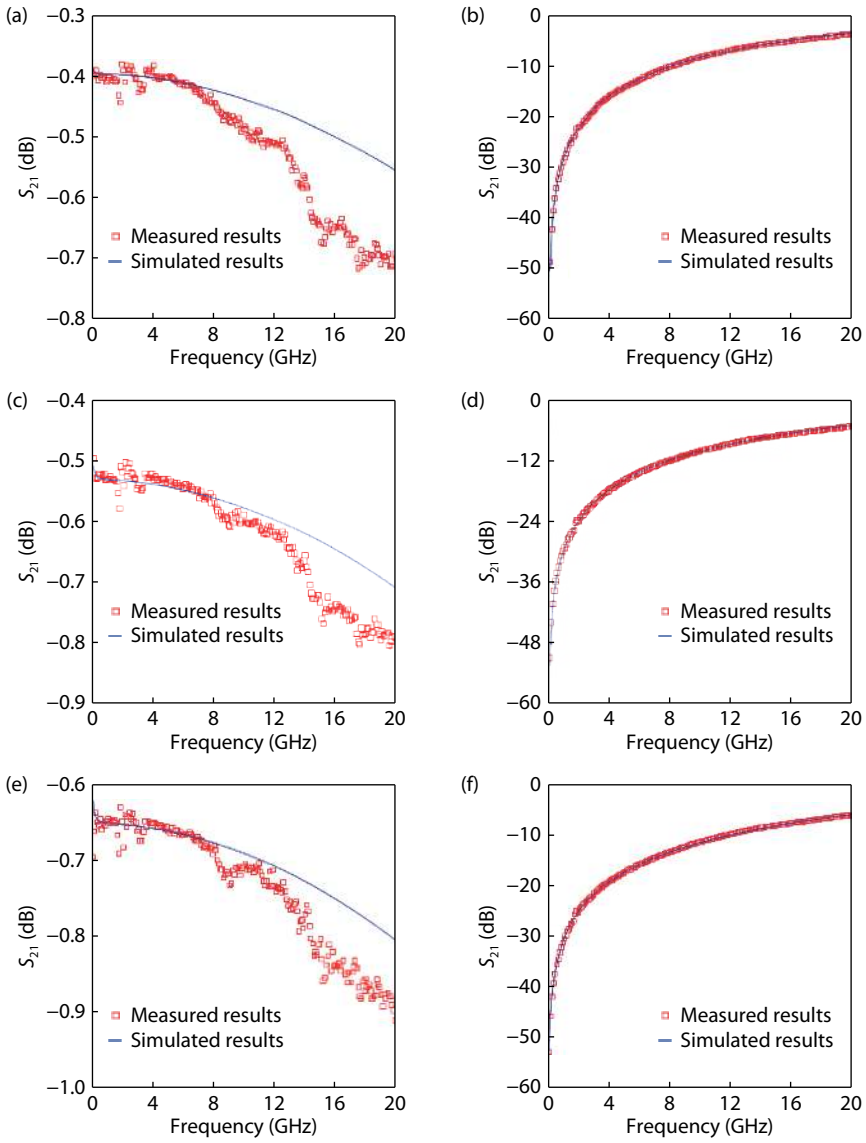

Fig. 11. (Color online) Illustration of the simulated and measured insertion loss and isolation (0.1–20 GHz) for a device with a size of 5 × 125 μm. (a) Insertion loss (dual-gate off state). (b) Isolation (dual-gate off state). (c) Insertion loss (triple-gate on state). (d) Isolation (triple-gate off state). (e) Insertion loss (quadruple-gate on state). (f) Isolation (quadruple-gate off state).

modeling technique for GaAs HEMT. 2018 Dynamics of Systems, Mechanisms and Machines (Dynamics), 2018, 1

[6] Yu L, Zheng Y K, Zhang S, et al. Small-signal model parameter extraction for AlGaN/GaN HEMT. J Semicond, 2016, 37(3), 034003

[7] Gibiino G P, Santarelli A, Filicori F. Charge-conservative GaN HEMT nonlinear modeling from non-isodynamic multi-bias *S*-parameter measurements. Int J Microwave Wireless Technol, 2019, 11(5/6), 431

[8] Changsi W, Yuehang X, Zhang W, et al. An improved temperature-dependent large signal model of microwave GaN HEMTs. J Semicond, 2016, 37(7), 074006

[9] Yu W H, Yang S Y, Hou Y F, et al. Small signal model and low noise application of InAlAs/InGaAs/InP-based PHEMTS. J Infrared Millimeter Waves, 2018, 37(6), 683

[10] Panda J, Jena K, Swain R, et al. Modeling on oxide dependent 2DEG sheet charge density and threshold voltage in AlGaN/GaN MOSHEMT. J Semicond, 2016, 37(4), 044003

[11] Panda D K, Lenka T R. Modeling and simulation of enhancement mode p-GaN Gate AlGaN/GaN HEMT for RF circuit switch applications. J Semicond, 2017, 38(6), 064002

[12] Jain N, Gutmann R J. Modeling and design of GaAs MESFET control devices for broad-band applications. IEEE Trans Microwave Theory Tech, 1990, 38(2), 109

[13] Ehoud A, Dunleavy L P, Lazar S C, et al. Extraction techniques for FET switch modeling. IEEE Trans Microwave Theory Tech, 1995, 43(8), 1863

[14] Takatani S, Chen C D. Nonlinear steady-state III–V FET model for microwave antenna switch applications. IEEE Trans Electron Devices, 2011, 58(12), 4301

[15] Tao Y, Hu Z F, Fan Y, et al. Direct extraction method of HEMT switch small-signal model with multiparasitic capacitive current path. Int J RF Microwave Comput-Aid Eng, 2019, 29(6), e21690

[16] Geng M, Li P X, Luo W J, et al. Small-signal modeling of GaN HEMT switch with a new intrinsic elements extraction method. Chin Phys B, 2016, 25(11), 117301

[17] Alt A R, Marti D, Bolognesi C R. Transistor modeling: Robust small-signal equivalent circuit extraction in various HEMT technologies. IEEE Microwave Mag, 2013, 14(4), 83

[18] White P M, Healy R M. Improved equivalent circuit for determination of mesfet and hemt parasitic capacitors from "coldfet" measurements. IEEE Microwave Guided Wave Letts, 1993, 3(12), 453

[19] Dambrine G, Cappy A, Heliodore F, et al. A new method for determining the FET small-signal equivalent circuit. IEEE Trans Microwave Theory Tech, 1988, 36(7), 1151