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RF performance evaluation of p-type NiO-pocket based β-Ga_2O_3/black phosphorous heterostructure MOSFET

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Abstract: The radio-frequency (RF) performance of the p-type NiO-pocket based β-Ga_2O_3/black phosphorous heterostructure MOSFET has been evaluated. The key figure of merits (FOMs) for device performance evaluation include the transconductance (g_m) gate dependent intrinsic-capacitances (C_{gd} and C_{gs}), cutoff frequency (f_T), gain bandwidth (GBW) product and output-conductance (g_d). Similarly, power-gain (G_p), power added efficiency (PAE), and output power (P_{OUT}) are also investigated for large-signal continuous-wave (CW) RF performance evaluation. The motive behind the study is to improve the β-Ga_2O_3 MOS device performance along with a reduction in power losses and device associated leakages. To show the applicability of the designed device in RF applications, its RF FOMs are analyzed. With the outline characteristics of the ultrathin black phosphorous layer below the β-Ga_2O_3 channel region, the proposed device results in 1.09 times improvement in f_T, with 0.7 times lower C_{gs}, and 3.27 dB improved G_P in comparison to the NiO-GO MOSFET. The results indicate that the designed NiO-GO/BP MOSFET has better RF performance with improved power gain and low leakages.

Key words: wide band-gap semiconductor; RF FOMs; Ga_2O_3; black phosphorus

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1. Introduction

The demand for high-performance, compact, and battery-operated devices for RF applications leads to the need for technology where power losses should be low[1]. To reduce the losses associated with the RF power devices, silicon material needs to be replaced by the other semiconductor material because the devices based on this technology are reaching their theoretical limits[2]. To compensate for several limitations found in Si-based devices, wide bandgap (WBG) semiconductors like GaN (~3.4 eV) and SiC (~3.3 eV) became the favorable materials to be opted[3]. In high power applications, the devices based on WBG (i.e GaN & SiC) semiconductor materials show the excellent capability of withstanding high breakdown voltage (V_{br}) with reduced power losses and leakages in comparison to Si[4]. However, for efficient implementation of high-power RF amplifiers with stable high-temperature operation certain parameters such as R_{ON}, off-state leakage current, switching speed, and $V_{br,}$ need to be optimized[5].

As a power electronics semiconductor, β-Ga_2O_3 has emerged in several fields from very high voltage power switching[5–7] to even GHz RF power amplification[8]. This is due to the advantage of high theoretical critical field strength (E_c) that surpasses both the SiC and GaN E_c values[9]. The two important high-frequency power device figure-of-merits (FOMs); i.e., the Johnson (2844.4) and Baliga's (3214.1) FOMs are found to be exceptionally high for Ga_2O_3 concerning silicon[10]. With its mobility ranging as 100 $cm^2/(V{\cdot}s)$, β-Ga_2O_3 transistors trend an opportunity towards operating as amplifiers that can be used for RF applications; i.e., RF amplifiers, RF switches and many more[5, 8].

In RF and power electronic applications based on gallium oxide MOS technology, several types of research have been carried out[3–10]. Mastro *et al.* discloses the reference to further opportunities in space of Ga_2O_3 and formulated a study that depicts Ga_2O_3 possess high electron saturation velocity (v_{sat}) along with high output current density, which gives a high value of cut-off frequency[10]. Further, Higashiwaki *et al.* demonstrates the performance of gallium oxide MOSFET under depletion mode operating condition and observed that 2 μm of gate length MOS device result in minimum off-state leakage current with I_{ON}/I_{OFF} ratio greater than 10^{10}[4]. Green *et al.* diverted the further study of gallium oxide MOSFET towards RF performance and stated its high value of g_m (21 mS/mm) and f_T (3.3 GHz)[8].

As 2D material technologies emerge in the space for future electronic devices, black phosphorous (BP) and also graphene have become rewarding materials. Recently, due to excellent electron transport properties, graphene has been the main focus for future RF electronics[11]. Being considered as a gapless semiconductor, graphene has an advantage of higher carrier mobility even at room temperature, which adds that β-Ga_2O_3 quite compatible with it. However, due to its poor saturation behavior, the use of graphene in RF and switching applications is still limited.

BP has been considered as another tunable bandgap material[12] with its higher carrier mobility stated as 1000 $cm^2/(V{\cdot}s)$. Due to the improved saturation behavior property, BP is particularly suited as an alternative for graphene[11, 13]. Li *et al.* fabricated FET based upon BP crystals with thickness referring to few nanometers. Reliability in these devices was observed at room temperature with 7.5 nm thickness and drain current modulation of 10^5 results in a better *I–V* characte-

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ristic[14]. Yan *et al.* studied the performance of β-Ga_2O_3/graphene heterostructure in a vertical barristor. The fabricated structure results in a high breakdown field of ~5 MV/cm and was found to be close to the theoretical E_c of β-Ga_2O_3 (~8 MV/cm)[15]. A comprehensive study for analog and RF performance of BP (20 nm) based MOSFET was analyzed by Kumar *et al.*[16]. The figure of merits investigated was $-f_T$, f_{max}, stern stability factor, various power gains along with parasitic capacitances at THz frequency range. The results show that the designed device is more suitable for RF applications. Yadava and Chauhan insights the introduction of a single layer of graphene/BP in Ga_2O_3 MOSFET to improve its RF performance. The losses associated with the introduction of the BP layer in Ga_2O_3 MOSFET has not been discussed in the above work[17]. But the problem lied in the β-Ga_2O_3 doping profile as the lack of p-type doping on β-Ga_2O_3 limits certain operations. Usually, for growing β-Ga_2O_3 single crystals and thin films, n-type was considered because their existence of unmeant impurities[18].

To overcome the lack of p-type conductivity in Ga_2O_3, p-type oxide (like Ir_2O_3, NiO) based heterostructures were considered[19]. Usage of the MOSFET with p-type Ir_2O_3 oxide-based channel region was demonstrated by FLOSFIA Inc.[20], which is considered as a groundbreaking work for future high-power electronics devices. Kokunan *et al.* fabricated the NiO/Ga_2O_3 hetero-junction diode by growing the p-type NiO layer on the Ga_2O_3 substrate using the sol-gel technique. The fabricated devices showed good rectifying behavior with a ratio $>10^8$ at ± 3.0 V[21]. The RF performance investigation of NiO (p-type) pocket based Ga_2O_3 MOSFET was done by Yadava and Chauhan, where the capacitance C_{gs}, which has a direct correlation with the device leakage, decreases with the use of NiO pocket region at both of the channel interfaces[22].

This paper investigates the impact of the BP layer on the RF performance of NiO pocket based gallium oxide MOSFET. The key FOMs for device performance evaluation includes the transconductance (g_m), gate dependent intrinsic-capacitances (C_{gd} and C_{gs}), cutoff frequency (f_T), gain bandwidth (GBW) product and output-conductance (g_d). Similarly, power-gain (G_p), power added efficiency (PAE), and output power (P_{OUT}) are also investigated for large-signal continuous-wave (CW) RF performance evaluation.

2. Device description

The structures of p-type NiO-pocket based β-Ga_2O_3 and p-type NiO-pocket based β-Ga_2O_3/black phosphorous heterostructure MOSFETs are shown in Figs. 1(a) and 1(b), respectively. Figs. 2(a) and 2(b) depicts the lattice temperature of conventional and p-type NiO-pocket based MOSFETs obtained at V_{DS} = + 40 V and V_{GS} = + 4 V. In β-Ga_2O_3 MOSFET shown in Fig 2(a), the maximum value of lattice temperature reaches to ~ 422 °C. However, with the use of p-type NiO-pocket in the device and under the similar device operating conditions, it only reaches 400 °C. Similarly, Figs. 3(a) and 3(b) shows the potential distribution of conventional and p-type NiO-pocket based MOSFETs respectively. In Fig. 3(b), the use of p-type NiO-pocket at both the channel interfaces results in a minute decrease in the potential is observed. This decrease is due to the abrupt transition in the device impurity doping profile from Ga_2O_3 (n-type) channel to NiO-pocket (p-type) regions.

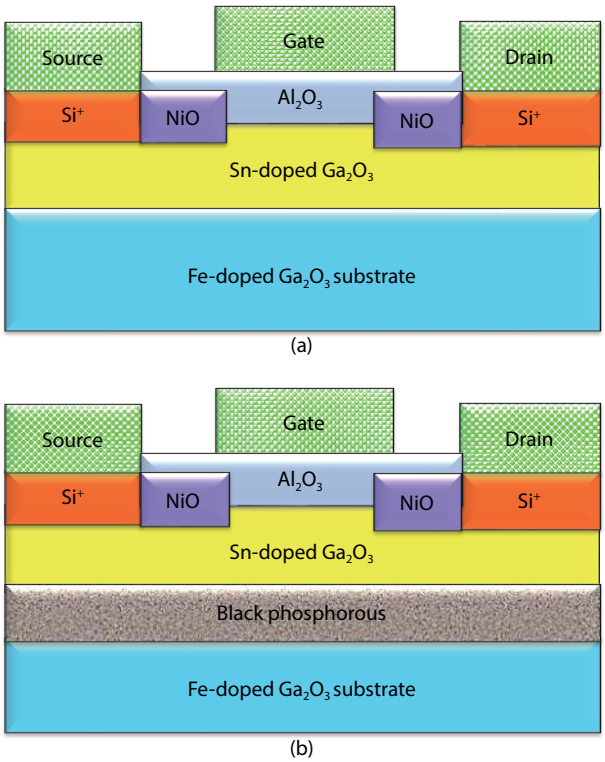

Fig. 1. (Color online) (a) P-type NiO-pocket based β-Ga_2O_3 MOSFET. (b) P-type NiO-pocket based β-Ga_2O_3/black phosphorous heterostructure MOSFET.

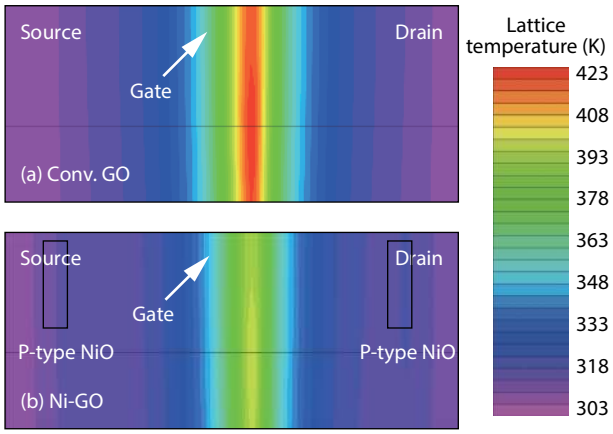

Fig. 2. (Color online) Lattice temperature in (a) β-Ga_2O_3 MOSFET and (b) P-type NiO-pocket based β-Ga_2O_3 MOSFET.

In the device, a 300 nm thick n-type β-Ga_2O_3 channel region was made to grow on a single crystal of β-Ga_2O_3 substrate. The n-type impurity doping concentration of the channel region is ~7×10^{17} cm^{-3} and around half of this is assumed to be activated by considering the measured *C–V* data of the fabricated gallium oxide MOS device[4]. The formation of source and drain electrodes is carried out by utilizing multiple Si^+ implants with a 150 nm deep box profile of n-type having a doping concentration of 3×10^{19} cm^{-3} optimized from the collective data of the device[4].

The overall distance between the source and drain region was 20 μm. On the top of the channel region, a 20 nm thick Al_2O_3 layer was made to deposited as a gate dielectric layer accompanied by the deposition of 2 μm long Ti/Pt/Au metal gate on the top. In NiO-pocket based β-Ga_2O_3/BP heterostructure MOSFET, a BP layer of 10 nm thick was made to de-

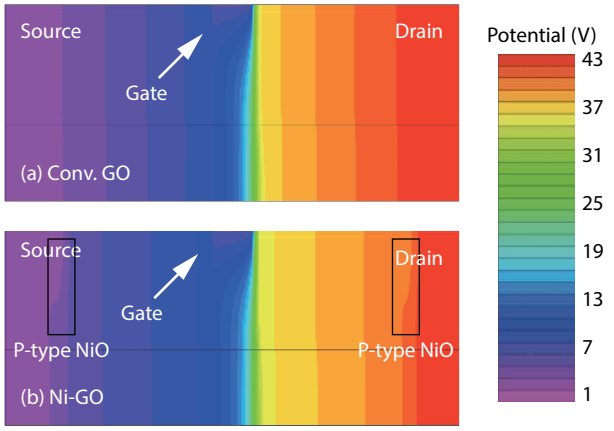

Fig. 3. (Color online) Potential distribution in (a) β-Ga_2O_3 MOSFET and (b) P-type NiO-pocket based β-Ga_2O_3 MOSFET.

Table 1. Material parameters used in the simulation of the β-Ga_2O_3/BP heterostructure MOS device.

Parameter	β-Ga_2O_3[4]	Black phosphorous[14]
Bandgap energy (eV)	4.8	1.88
Local conduction band density of states (10^{17} cm^{-3})	37.2	0.3
Work function (eV)	5.23	4.56
Electron affinity (eV)	4.0	5.5
Relative permittivity (F/m)	10.0	6.1

posited over the substrate, while keeping other conditions similar. The important material parameters used in the design of the β-Ga_2O_3/BP heterostructure MOS device are summarized in Table 1.

3. Simulation and model calibration method

All the parameters and RF FOMs are extracted out from the ATLAS device simulation tool[23]. The Newton numerical technique is used to obtain numerical solutions because it provides better convergence. For obtaining in the device LAT.TEMP parameter is set up in the model parameter. Using equation (1), we can attain temperature-dependent electron mobility with lattice temperature coefficient TMUN = 2[23]. Along with the ATLAS simulation tool, ATHENA (process simulator) is also used to pro-create multiple Si^+ implantations[4] using a material implant model called BCA.

$$\mu_{n0} = \mathrm{MUN}\left(\frac{T_L}{300}\right)^{-\mathrm{TMUN}}, \quad (1)$$

where μ_{n0} is low field mobility, MUN is the electron mobility and T_L is lattice temperature.

In the material parameters of the BP region (see Table 1), the bandgap (E_g) is set to 1.88 eV, the relative permittivity and electron affinity of 6.1 and 5.5 eV are taken, respectively. These parameters are obtained from the experimental measurement of the BP FET given by Li *et al.*[14].

4. Feasible fabrication steps of the devices

The fabrication of the gallium oxide MOSFET was already demonstrated by Higashiwaki *et al.*[4] and Zing *et al.*[24]. In the initial fabrication step, a single-crystal of the β-Ga_2O_3 substrate is made to doped with Fe, over which an Sn doped 300 nm thick n-Ga_2O_3 channel layer was formed by using the

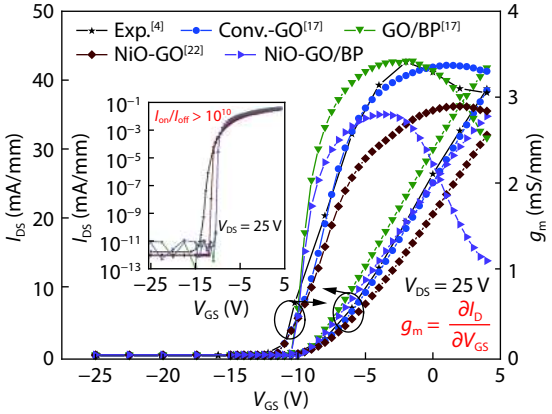

Fig. 4. (Color online) Transfer (I_D–V_{GS}) and transconductance (g_m) behavior of the devices. Inset: I_D–V_{GS} in log-scale.

MBE technique[4]. Using Knudsen cells, Sn and Ga fluxes are carried out by powdered SnO_2 and Ga metal, respectively. Followed by growing of the SiO_2 layer using PECVD[4, 6]. To open up, source, and drain regions, lithography is being performed. Generally, to carry out these fabrication steps, often positive PR along with maskless lithography is used[25]. Using multiple Si^+ implantations, source, and drain electrode regions are defined accompanied by annealing[25]. Thereafter, two NiO pocket regions of 10 nm thicker in length were made to form at the channel (drain/channel & source/channel) interfaces. Now, the grown NiO region is made p-type (impurity concentration ~1.6×10^{17} cm^{-3}) by adding Li as an acceptor impurity[21]. After this, the removal of the deposited SiO_2 on the gate region was done by using RIE[4]. Now, the ALD technique is utilization for the deposition of Al_2O_3 of 20 nm thick as a gate dielectric layer followed by RIE[25, 26]. Soon after the fourth lithography, a 2 μm long Ti/Pt/Au metal gate is formed over the top of the gate oxide layer[4, 25]. For both Ga_2O_3/BP and p-type NiO pocket based β-Ga_2O_3/BP heterostructure MOSFETs, a process step is maintained soon after Ga_2O_3 substrate formation. For this process step, the PDMS stamping technique is used to deposit a thin layer of BP over the substrate layer followed by epitaxial growth of the channel region[16, 17].

5. Results and discussion

To examine RF performance of the devices, the FOMs such as transconductance (g_m) gate dependent intrinsic-capacitances (C_{gd} and C_{gs}), cutoff frequency (f_T), gain bandwidth (GBW) product and output-conductance (g_d) are used. All of the analysis is done by using ATLAS 2D simulator[23].

Fig. 4 shows the DC transfer characteristics of simulated devices, to consider the effect of NiO pocket on β-Ga_2O_3 MOSFET with the BP layer. The transfer and the output characteristics of the devices are shown in Figs. 4 and 5, respectively, in which the conventional device is taken from the reported literature and is very much in agreement with the experimental device demonstrated by Higashiwaki *et al.*[4].

In Fig. 4, the increased carrier to carrier scattering at the channel interfaces results in a small increase in the value of drain current (I_D) in p-type NiO pocket based Ga_2O_3 (NiO-GO)[22] MOSFET in comparison to the Conventional Ga_2O_3 MOSFET (Conv. GO)[17], experimental Ga_2O_3 MOSFET (Exp.)[4] and β-Ga_2O_3/BP (GO/BP) heterostructure MOSFET. For the devices,

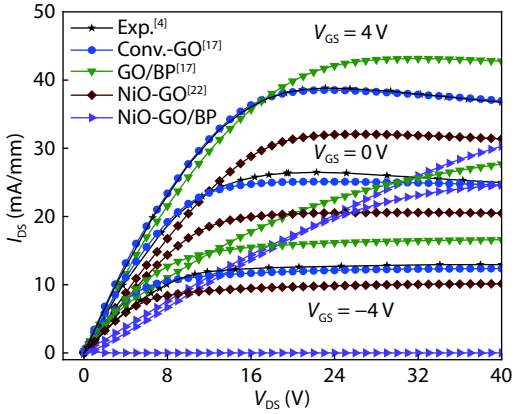

Fig. 5. (Color online) Output characteristics (I_D–V_{DS}) of the devices.

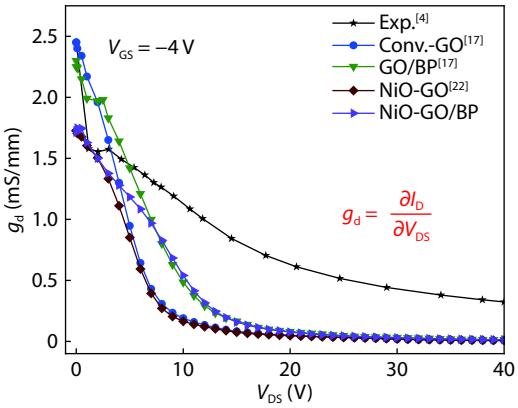

Fig. 6. (Color online) Output conductance (g_d) behavior of the devices.

the value of the I_{on}/I_{off} ratio of about 1 × 10^{10} is observed with off-state leakage in the range of a few pA.

Fig. 6 shows the output conductance characteristics of the device plotted between g_d and V_{DS} with V_{GS} = –4 V. For high gain applications, a device should possess a lower value of g_d which can be seen in p-type NiO β-Ga_2O_3/BP (NiO-GO/BP) heterostructure MOSFET. For a device to be used for RF applications, higher output gain requires lower output conductance as depicted in Eq. (3).

By performing small-signal AC analysis after the post-processing operation of DC results, one can obtain the device C_{gd} and C_{gs} values at the constant frequency of 0.8 GHz using DC gate voltage swept from –25 to 4 V. Figs. 7 and 8 represent the variation in C_{gd} and C_{gs} for different V_{GS} values, respectively. The increased capacitive coupling between the gate and drain terminals of the NiO-GO[22] and NiO-GO/BP MOSFETs results in larger C_{gd} value in comparison with Conv. GO MOSFET[17]. However, the C_{gs} value which straightly contributes to the leakage is found to be 0.7 times lesser for NiO-GO/BP MOSFET on comparing to NiO-GO[22] MOSFET.

$$g_m = \frac{\partial I_D}{\partial V_{GS}}, \tag{2}$$

$$g_d = \frac{\partial I_D}{\partial V_{DS}}, \tag{3}$$

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \tag{4}$$

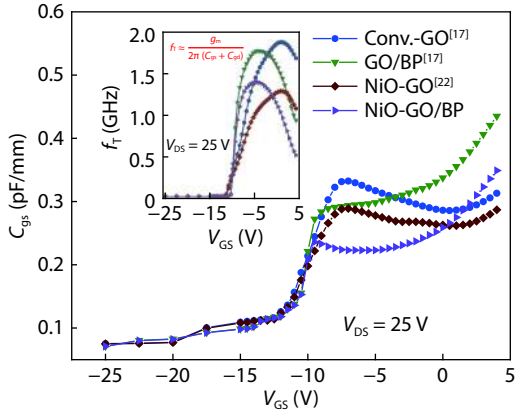

Fig. 7. (Color online) Intrinsic capacitance (C_{gs}) versus gate voltage (V_{GS}). Inset: f_T versus V_{GS}.

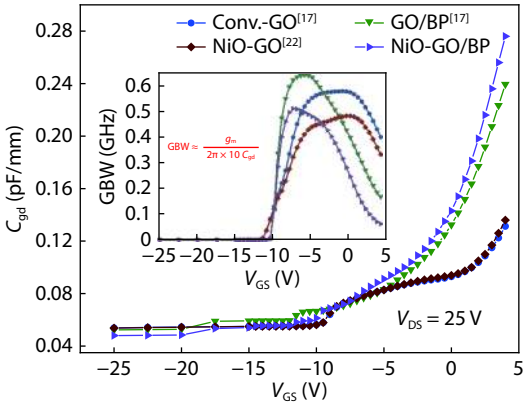

Fig. 8. (Color online) Intrinsic capacitance (C_{gd}) versus gate voltage (V_{GS}). Inset: GBW versus V_{GS}.

$$\text{GBW} = \frac{g_m}{2\pi \times 10 \times C_{gd}}, \tag{5}$$

$$f_T = f_0 \cdot |H_{21}|. \tag{6}$$

The f_T (see Eq. (4)) is the key FOMs for the depiction of the high-frequency performance of RF devices. The cutoff frequency also stated as GBW (see Eq. (5)) is simultaneously related to H_{21} (short-circuit current gain). Regarding the two-port network, H_{21} is known as the ratio of output terminal current to the input terminal current of small-signal with output short-circuited. This parameter is frequency-dependent and its magnitude sweeps at high frequencies with a slope of –20 dB/dec. Keeping this justification, f_T can be termed as the frequency value at which the magnitude of H_{21} decreases to unity. Using Eq. (6) we can evaluate the f_T and inset of Fig. 7 shows the f_T curve of the proposed device. A smaller value of f_T is observed in the case of NiO-GO[22] and NiO-GO/BP MOSFETs in comparison to the Con. GO[17]. However, a 1.09 times improvement in the value of f_T is found in NiO-GO/BP MOSFET in comparison to NiO-GO[22] MOSFET.

In Fig. 8, the inset graph indicates that the GBW product decreases with the use of the NiO pocket region of p-type in the device. This is due to the decreased value of g_m. However, to compensate for this, a thin BP layer is used below the channel region which improves GBW product in comparison to NiO-GO[22] MOSFET.

In large-signal RF applications, P_{OUT}, PAE, and G_P are ana-

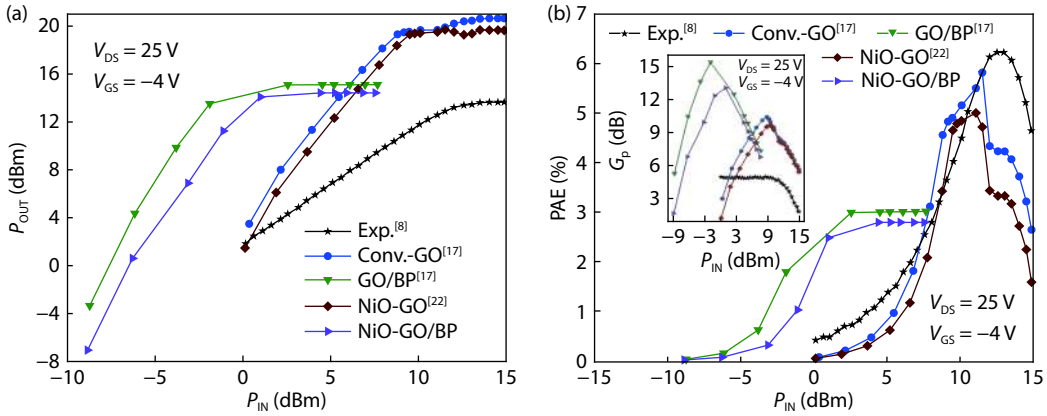

Fig. 9. (Color online) (a) Output power (P_{OUT}) versus input power (P_{IN}). (b) Power-added-efficiency (PAE) versus input power (P_{IN}). Inset: Output power gain (G_P) versus P_{IN}.

Table 2. RF performance comparison of the reported gallium oxide MOSFETs with the proposed NiO-GO/BP MOSFET.

Reference	MOSFET	C_{gs} (pF)	C_{gd} (pF)	f_T (GHz)	GBW (GHz)	P_{OUT} (dBm)	(PAE) (%)	G_P (dB)
Ref. [8]	Exp. GO	–	–	3.30	–	13.71	6.3	5.10
Refs. [4, 17]	Conv. GO (Exp. GO. by Higashiwaki *et al.*)	0.33	0.13	1.87	0.5	20.64	5.8	10.50
	GO/BP	0.43	0.22	1.77	0.64	15.11	3.0	15.31
Ref. [22]	NiO-GO	0.29	0.13	1.27	0.48	19.30	4.8	9.75
This work	NiO-GO/BP	0.23	0.18	1.37	0.51	14.73	2.8	13.02

lyzed. Fig. 9 (see Figs. 9(a) and 9(b)) represent the plot of P_{OUT}, G_P, and PAE versus P_{IN} at V_{DS} and V_{GS} of 25 and –4 V, respectively. For any MOSFET based power amplifiers, efficiency (η) can be estimated out as (see Eq. (7)):

$$\eta = \frac{P_{Load}}{P_{Supply}}, \tag{7}$$

where P_{Load} is the average power delivered to load terminal and P_{Supply} is average supply power. In the power amplifiers, where heat dissipation is of major concern, PAE (see Eq. (8)) is used as an important FOM.

$$PAE = \frac{P_{Load} - P_{Input}}{P_{Supply}}, \tag{8}$$

where P_{Input} is the average input power.

In the NiO-GO/BP MOSFET based PA circuit, due to the increased feedback (which increases the value of C_{gd} as stated above), the value of both PAE & G_P decreases (see Fig. 9(b)). However, these large-signal RF FOMs are found to be improved on comparing it with NiO-GO[22] MOSFET, which is depicted because there is an introduction of the BP layer underneath the channel region. For GO/BP MOSFET, the measured G_P is 13.02 dB and is 3.27 dB superior to NiO-GO[22] MOSFET. Nevertheless, the value of PAE measured is 2.03% less efficient to NiO-GO[22] MOSFET. Also, we can see from Table 2 that NiO-GO/BP MOSFET shows better RF performance with improved power gain and low leakages.

6. Conclusion

The p-type NiO pocket in Ga_2O_3/black phosphorous heterostructure MOSFET is used to improve the device performance by reducing the leakages and other associated losses. The FOMs that are used in this analysis to investigate its applicability in the RF applications are f_T, g_m, g_d, and the intrinsic capacitances (C_{gd} and C_{gs}) and large-signal RF FOMs like P_{OUT}, G_p, and PAE. The I_{on}/I_{off} of about 1×10^{10} is observed with off-state leakage in the range of a few pA. The C_{gs} value which straightly contributes to the leakage is found to be 0.7 times lesser for NiO-GO/BP MOSFET along with 1.09 times improvement in f_T in comparison to that of NiO-GO[22] MOSFET. In the NiO-GO/BP MOSFET based PA circuit, due to the increased feedback (which increases the value of C_{gd} as stated above), the value of both PAE & G_P decreases. However, these large-signal RF FOMs are found to be improved on comparison with NiO-GO[22] MOSFET and this is depicted because there is an introduction of the BP layer underneath the channel region. For GO/BP MOSFET, the measured G_P is 13.02 and is 3.27 dB superior to NiO-GO[22] MOSFET. Nevertheless, the value of PAE measured is 2.03% less efficient to NiO-GO[22] MOSFET. The obtained results show that the NiO-GO/BP MOSFET has better RF performance with improved power gain and low leakages. The RF performance of the proposed device can be improved with the development of p-type material for Ga_2O_3 semiconductor-based devices.

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