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Performance of hydrogenated diamond field-effect transistors on single and polycrystalline diamond

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Abstract: In this work, we investigate the influence of defect concentration of the diamond substrates on the performance of hydrogen-terminated diamond field-effect transistors by Raman spectra, pulsed *I–V* characteristics analysis, and radio frequency performances measurements. It is found that a sample with higher defect concentration shows larger drain-lag effect and lower large-signal output power density. Defects in the diamond act as traps in the carrier transport and have a considerable influence on the large-signal output power density of diamond field-effect transistors. This work should be helpful for further performance improvement of the microwave power diamond devices.

Key words: diamond; transistor; trap; defect; power density

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1. Introduction

Due to their wide band gap (5.47 eV), high breakdown electric fields (~10 MV/cm), large thermal conductivity (22 W/(cm·K)) and large carrier saturation velocity (~1 × 10^7 cm/s), hydrogen-terminated diamond field-effect transistors (FETs) are promising materials for high-power and high-frequency devices[1]. It has been found that two-dimensional hole gas (2DHG) formed on the surface of hydrogen-terminated diamond and showed promising electrical performance. For a hydrogen-terminated diamond sample, the reported maximum drain current density (I_{DS}) has reached 1.3 A/mm[2]. The maximum oscillation frequency (f_{max}) of 120 GHz has been reported in a polycrystalline hydrogen-terminated diamond FETs[3]. The highest reported output power density at 1 GHz has reached 3.8 W/mm in polycrystalline hydrogen-terminated diamond FETs[4], and 815 mW/mm at 2 GHz[5]. By now, the polycrystalline diamond FETs show comparable or even better direct current (DC) and radio frequency (RF) performances than single crystal diamond FETs[6, 7]. This indicates that the advantage of single crystal diamond is not exerted. The crystal quality of the single crystal diamond need to be further improved[8]. An insight of the performance's key influence factors of hydrogen-terminated diamond FETs needs to be provided.

In this work, a comparative study was performed on the DC and RF performance of hydrogen-terminated polycrystalline and single crystal diamond FETs considering the influence of defect concentration of the diamond substrates. A self-aligned fabrication process was used to fabricate the diamond FETs. Ohmic contact metal was Au and gate dielectric was self-oxidized alumina.

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2. Experiments

Three diamond samples were used to fabricate diamond FETs, as shown in Table 1. For the polycrystalline diamond (samples of I-PC, and II-PC), hydrogen termination was formed by the microwave plasma chemical vapor deposition (MPCVD) treatment technique in H_2 plasma. For the single crystal (001) diamond sample (III-SC), the hydrogen-termination was formed by homoepitaxial growth process as stated in Ref. [7]. Micro-Raman scattering experiments with laser line of 532.2 nm and powder X-ray diffraction (XRD) were performed at RT. The self-aligned fabrication process of the diamond FETs can be found in our previous study[5].

3. Results and discussion

Fig. 1 shows the Raman spectra and XRD pattern of the three diamond samples. It can be seen that the background of the sample I-PC is very small. But for the samples II-PC and III-SC, the background line shows a significant upward movement, which is proven to be due to the increase of defect and impurity content[9]. This indicates that the quality of sample II-PC is poor. Sample III-SC also has some defects and impurities. And sample I-PC shows high quality. We measured the nitrogen content of the three samples by secondary ion mass spectroscopy (SIMS) and found that the nitrogen content for II-PC sample is 0.23 ppm, and III-SC sample is 0.21 ppm. And for the I-PC sample, the nitrogen content is under the detection limit of SIMS. Nitrogen should be the main impurities in the samples.

The gate length and source–drain space of the three dia-

Table 1. Critical dimensions and DC characteristics of the diamond FETs.

Sample name	I_{ds} (mA/mm)	g_m (mS/mm)	Gate length and source–drain space	Drain-lag effect
I-PC	323	66	T-gate, L_g = 350 nm, L_{SD} = 3 μm, W_g = 100 μm × 2	2.7%
II-PC	466	58	Rectangular gate, L_G = 400 nm, L_{SD} = 1.6 μm, W_g = 100 μm × 2	10%
III-SC	233	62	T-gate, L_g = 350 nm, L_{SD} = 2 μm, W_g = 100 μm × 2	3.7%

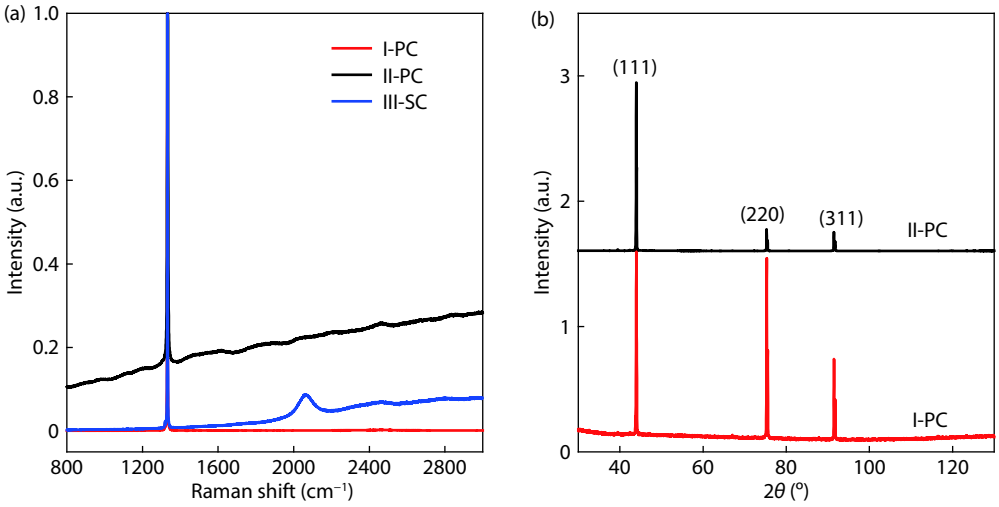

Fig. 1. (Color online) (a) Raman spectra of the I-PC, II-PC, and III-SC diamond samples. (b) XRD pattern of I-PC, and II-PC diamond samples.

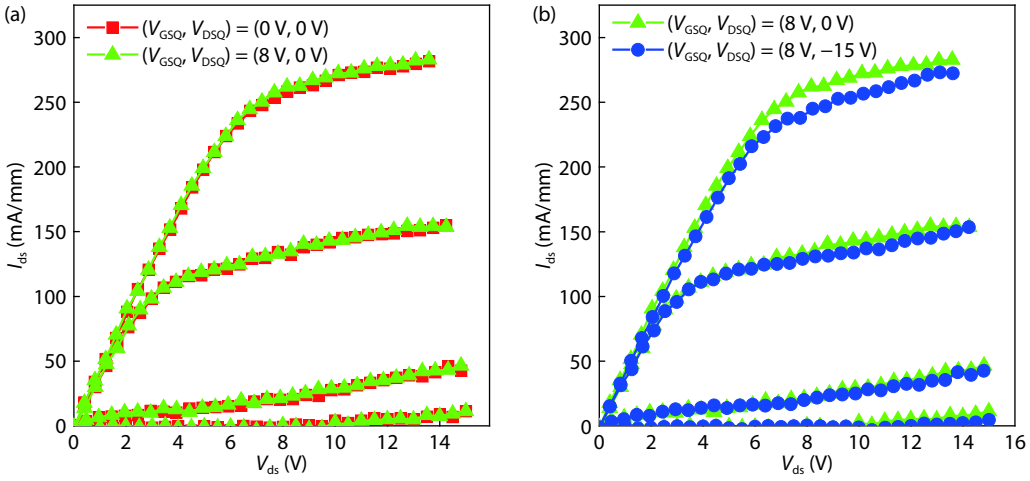

Fig. 2. (Color online) Pulsed *I–V* characteristics of III-SC diamond FET.

mond samples were shown in Table 1[5, 10, 11]. As shown in Table 1, the polycrystalline diamond FETs (I-PC and II-PC) show higher maximum saturation source–drain current I_{ds} than the single crystal diamond FET (III-SC). This may be due to the different orientations of the single crystal and polycrystalline diamond samples. The orientation of the single crystal diamond is (001). The polycrystalline diamond samples are composed of grains with different orientations, including (111), (220), and (311), as shown in Fig. 1(b). As reported by Sato *et al.*, the sheet density of (110), and (111) H-terminated surfaces are higher than that of (100) surfaces[12]. From first-principle calculations, the VBM level is the highest for (110), second highest for (111), and the lowest for (100)[13] and the hole concentration depends on the C–H bond density[14]. And the values of their maximum transconductance g_m are comparable for the three samples.

Pulsed *I–V* characteristics for the III-SC sample at different quiescent bias points were measured, as shown in Fig. 2. The measured results for the I-PC and II-PC samples have been shown in our previous work[5, 11]. The setting conditions for pulsed *I–V* characteristics measurements are the same with our previous work[5]. It was found that for all the three samples, the gate-lag effect (traps respond to the gate voltage) is negligible. The drain-lag effect (traps responded to the drain voltage) induces the maximum drain current decrease, as shown in Fig. 2(b). The maximum drain current degeneration values induced by drain-lag effect are 2.7%, 10%, and 3.7%, respectively, as shown in Table 1. Combined with the Raman results in Fig. 1(a), the high defect concentration and impurity content in the diamond samples, the large drain-lag effect exists in the FETs. This indicates that the N impurities and defects in the diamond will act as traps in the car-

Table 2. Component parameters for the three diamond FETs.

Sample	C_{gs} (fF)	C_{gd} (fF)	g_m (mS)	R_i (Ω)	R_g (Ω)	R_d (Ω)	R_s (Ω)	f_T (GHz)	f_{max} (GHz)
I-PC	172.4	5.54	22.3	16	23	49	38	17	30
II-PC	102.4	17.6	20.7	14.6	32	30.3	27.7	20.7	19.5
III-SC	130	8.9	20.8	7.8	18	42	35	23	49

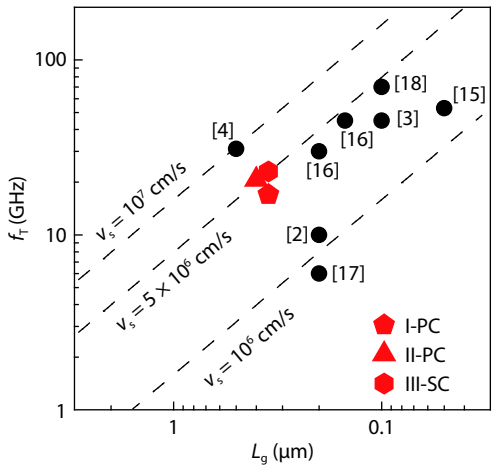

Fig. 3. (Color online) Relationship of cutoff frequency f_T with gate length for diamond FETs[2-4, 15-18].

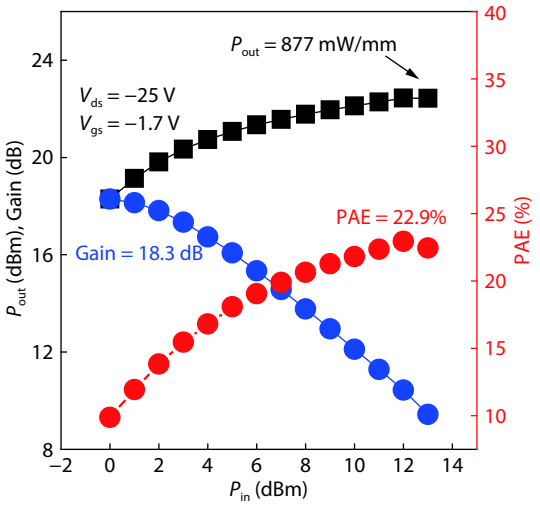

Fig. 4. (Color online) Large signal performance of I-PC diamond FET at 2 GHz power sweep (A-class).

rier transport.

The small signal *S*-parameters of the diamond FETs were measured between 0.1–30 GHz[5, 10, 11]. Open and short structures were used to remove the parasitic elements. The relationship of current cut-off frequency f_T and gate length (L_g) of the diamond FETs is shown in Fig. 3[2–4, 15–18]. The extrinsic saturation drift velocities v_s of the three samples (I-PC, II-PC, and III-PC) are all around 5×10^6 cm/s, as shown in Fig. 3.

The component parameters of the three diamond samples extracted from the small single parameters are shown in Table 2. The three samples show comparable cut-off frequency f_T, but f_{max} values show big difference. The extrinsic f_{max} for transistors can be expressed as[19]

$$f_{max} = \frac{g_m / 2\pi(C_{gs}+C_{gd})}{2\sqrt{g_{ds}(R_i + R_s + R_g) + g_m R_g \dfrac{C_{gd}}{C_{gs}}}}. \quad (1)$$

It can be seen that the parasitic resistance has strong influence on the extrinsic f_{max} for transistors. The f_{max} value of sample II-PC is the lowest. This is due to its rectangular gate structure, which makes the gate resistance R_g large, as shown in Table 2.

Fig. 4 shows the RF power output characteristic measured at 2 GHz under a continuous-wave signal (A-class) for the I-PC diamond FET. As shown in the figure, the maximum gain is 18.3 dB and the power added efficiency (PAE) is 22.9%. The maximum output power density (P_{out}) reaches 877 mW/mm at 2 GHz for our diamond FET. It is the best reported output power density for diamond FETs measured at 2 GHz[5, 10, 17, 20]. The P_{out} can be estimated by

$$P_{out} = \frac{I_{ds\text{-}max}(V_{work} - V_{knee})}{4}, \quad (2)$$

where $I_{ds\text{-}max}$ is the maximum drain current density, V_{work} is the drain voltage for the measurement of P_{out}, and V_{knee} is the knee voltage. The large-signal power gain result shows that the device exhibits a large compression even at class-A operation. The possible reasons are that the drain current density (323 mA/mm) is small, and the knee voltage (~6 V) is high for the H-terminated diamond FETs. The sheet resistance of the H-terminated diamond is high (~kΩ/□), and the parasitic resistance is high (poor Ohmic contact). Table 3 shows the compare of measured output power density and calculated output power density for the three diamond samples (I-PC, II-PC, and III-PC). The drain voltage values for the measurements of the three samples are −25, −24, and −25 V, respectively. It can be seen that for all three samples, the measured output power densities are lower than the calculated output power densities, which should be due to the trapping effects. The knee voltage will increase at continuous drain voltage and the drain current will degrade. Both of them would cause a decrease in output power. The II-PC sample shows the largest degrade in output power density. This is consistent with the pulsed *I*–*V* measurement. This sample shows the largest maximum drain current degeneration induced by drain-lag effect. These results indicate that defects and N impurities in the diamond act as traps in the carrier transport and have great influence on the output power characteristics of diamond FETs.

Table 3. Compare of measured and calculated output power densities for the three diamond samples (I-PC, II-PC, and III-PC).

Sample	Measured output power density (mW/mm)	Calculated output power density (mW/mm)	Measured conditions	
			V_{ds}(V)	V_{gs}(V)
I-PC	877	1600	−25	−1.7
II-PC	745	2100	−24	−1
III-SC	815	1200	−25	−1

4. Conclusion

In summary, three kinds of diamond FETs were fabricated on polycrystalline and single crystal hydrogen-terminated diamond with different defect levels and impurity contents. Direct current and radio frequency performances analysis show that the frequency of devices depends mainly on the parasitic parameters, which are closely related to the device structure. Meanwhile, the output power density is greatly influence by the defect and impurity level of the samples. The defects and impurities in the diamond act as traps in the carrier transport. The trapping effects induce the knee voltage increase and the drain current degrade at continuous drain voltage. Diamond with high crystal quality and low impurity level is in great demand for microwave power devices.

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