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Journal of Semiconductors
(2020) 41, 122403
doi: 10.1088/1674-4926/41/12/122403

Design of GGNMOS ESD protection device for radiation-hardened 0.18 μm CMOS process

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Abstract: In this paper, the ESD discharge capability of GGNMOS (gate grounded NMOS) device in the radiation-hardened 0.18 μm bulk silicon CMOS process (Rad-Hard by Process: RHBP) is optimized by layout and ion implantation design. The effects of gate length, DCGS and ESD ion implantation of GGNMOS on discharge current density and lattice temperature are studied by TCAD and device simulation. The size of DCGS, multi finger number and single finger width of ESD verification structures are designed, and the discharge capacity and efficiency of GGNMOS devices in ESD are characterized by TLP test technology. Finally, the optimized GGNMOS is verified on the DSP circuit, and its ESD performance is over 3500 V in HBM mode.

Key words: total ionizing dose; RHBP; GGNMOS; ESD ion implantation; STI; TLP; leakage current; DCGS

Citation: J W Wu, Z G Yu, G S Hong, and R B Xie, Design of GGNMOS ESD protection device for radiation-hardened 0.18 μm CMOS process[J]. *J. Semicond.*, 2020, 41(12), 122403. http://doi.org/10.1088/1674-4926/41/12/122403

1. Introduction

With the improvement of process, the design challenges of ESD have become increasingly significant[1]. The introduction of ultra shallow junction, silicide and epitaxial layer has a negative impact on ESD performance. In ultra deep submicron CMOS process, because the breakdown voltage of thin gate oxide is low, an effective on-chip ESD protection circuit must be added to clamp the over impulse voltage on the internal gate oxide. To obtain the robustness of the built-in ESD device, additional ion implantation process can be used to increase the junction depth of the source and drain improve the ESD performance. The on-chip ESD protection device will be limited by thin gate oxide breakdown voltage and MOSFET drain breakdown voltage. NMOS devices are usually used as on-chip ESD protection devices in ultra deep submicron process, and GGNMOS devices are commonly used. The main problem of this device is that it is unable to fully open multiple fingers in the process of electrostatic discharge, so part of silicide needs to be shielded for better ESD capability.

The radiation-hardened bulk CMOS process technology adopts an epitaxial layer technology[2], which improves the LET threshold of SEL (single event latch up). In this way, the bulk resistance is reduced, and the ESD performance is reduced accordingly. Due to the decrease of well resistance, uniform triggering is difficult. The GGNMOS device based on the original ESD design rules can not trigger multiple fingers evenly, the ESD current cannot be fully released, and the triggered fingers burn out prematurely due to overheating.

The significance of this paper: through studying the working mechanism in the ESD event of GGNMOS devices, parameters such as breakdown voltage, holding voltage, internal resistance and so on are optimized. By means of device simulation, process experiment, TLP test verification and circuit ESD capability evaluation, the development and verification of the radiation hardened 0.18 μm bulk silicon CMOS process ESD protection device GGNMOS based on epitaxial wafers are completed. Without additional process steps, the ESD performance of GGNMOS can reach HBM 3500 V. The GGNMOS device has small area consumption, good robustness, excellent leakage characteristics and radiation hardness.

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Received 30 MARCH 2020; Revised 27 APRIL 2020.

2. ESD protection design

The structure of the IC (integrated circuit) chip ESD protection system is shown in Fig. 1[3], including: input level protection circuit, output level protection circuit, power clamp, power to ground ESD protection device, diodes between different power supplies. ESD protection circuit uses one-way conduction devices (diodes or devices with parasitic diodes, triodes, GGNMOS, GCNMOS, GRNMOS, GDPMOS, SCR, etc.)[4, 5] and powerful power to ground clamp circuit, which is connected with ground wire through low resistance power line, providing effective discharge path for various ESD discharge conditions. Among them, GGNMOS is commonly used in the ESD protection circuit of ultra deep submicron integrated circuit process with good compatibility and ESD performance.

The typical input and output port ESD protection is shown in Fig. 2[6]. Generally, the secondary protection structure is adopted. The output stage and the middle between the input primary stage and the second stage usually use a current limiting resistor of tens of ohms to protect the gate oxygen breakdown of the core (not shown in the picture).

As shown in Fig. 3, the main working principle of GGNMOS ESD device is taking advantage of NMOS device avalanche breakdown and lateral parasitic NPN (LNPN) transistor to turn on large current conduction to realize an effective method to protect the integrated circuit from damage in ESD events.

GGNMOS typical high current *I*–*V* curve *ABCDE* is shown in Fig. 4, in which the horizontal axis represents the voltage

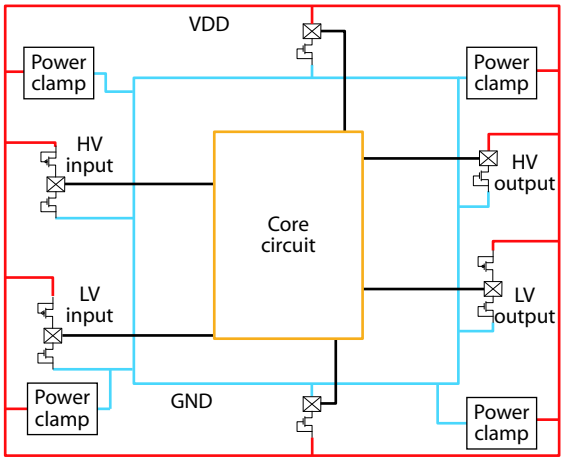

Fig. 1. (Color online) The structure of IC (integrated circuit) chip ESD protection system.

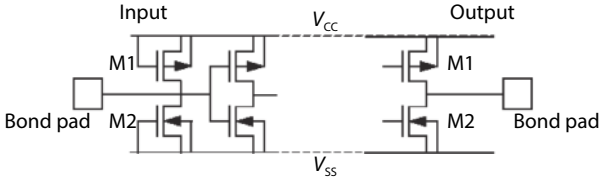

Fig. 2. CMOS input and output ESD protection circuit.

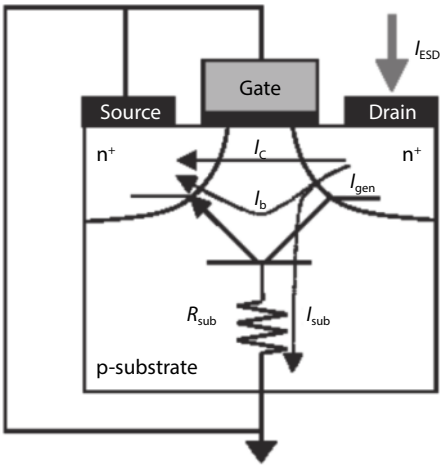

Fig. 3. ESD working principle of GGNMOS device.

of ESD device port, the vertical axis represents its current, and the dotted line with arrow represents the ESD design window. 1) Point *B* V_{t1} is the trigger voltage of GGNMOS transverse parasitic NPN transistor, which is strongly related to the reverse biased breakdown voltage of NMOS drain PN junction. In ESD event, the reverse biased voltage of drain junction increases in a positive direction, which causes the avalanche breakdown of drain PN junction, the current flows to the substrate and body contact end, and the potential difference is formed in the body area. When the source-bulk PN junction barrier voltage drops 0.6–0.7 V, a positive bias is generated, a large number of injected electrons are quickly collected and accelerated. When the discharge coefficient is greater than 1, a positive feedback is generated, and the LNPN is triggered. 2) Point *C* V_h is the hold voltage, which is mainly related to the body resistance. The device enters the *CD* section of ESD current conduction linear working area. 3) The *CD*

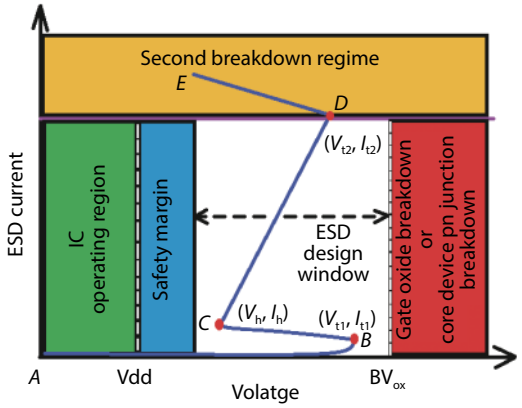

Fig. 4. (Color online) Typical discharge curve and design window of GGNMOS device in ESD event.

segment shows a positive resistance characteristic, and large current produces lattice heating. The *D* point V_{t2} and I_{t2} are the secondary breakdown voltage and current, which are the key parameters for characterizing the current carrying capacity of GGNMOS devices in the ESD process. 4) When going over the *D* point, the gate oxide leakage, PN junction leakage and even short circuit will appear in the damaged area of GGNMOS. It is found that I_{t2} is strongly affected by the factors of β, gate length, drain junction depth, total width (including multi index and single finger width), gate drain spacing, epitaxial layer concentration and thickness[7].

3. Parameter design and process TCAD simulation of GGNMOS

In contrast from the commercial 0.18 μm bulk silicon CMOS process, the radiation hardened 0.18 μm bulk silicon CMOS process increases the total dose performance, and introduces a high concentration p^+ substrate and a thin layer of p-epitaxial layer, which makes the longitudinal doping of MOSFET devices change correspondingly, and reduces the p-well resistance to inhibit the SCR single particle radiation induced latch-up. These changes affect the ESD discharge efficiency of GGNMOS devices. It is necessary to redesign the structure of GGNMOS devices to improve the robustness of devices and improve the ESD discharge ability.

In this paper, the multi-finger GGNMOS structure as shown in Fig. 5(a) below is adopted, in which AA' represents the position of 2D process simulation section, and Fig. 5(b) represents the enlarged diagram of 3D display area. On the layout, the width of single finger is *W*, the number of multiple fingers is *M*, and the gap between gate edge and drain contact is DCGS[8, 9]. The ESD ion implantation concentration is mainly controlled by the process flow, and other basic process characteristic parameters are shown in Table 1 as below.

In this work, TCAD simulation of polysilicon gate length, drain contact to gate-edge spacing (DCGS), ESD injection dose and TLP *I*–*V* curve in GGNMOS structure is carried out, as shown in Fig. 6. p^+ sub substrate, source end, body end and gate end are connected to the cathode, while drain end is used as anode. The following curve (show in Fig. 7) is used in the electrical simulation of TLP. The TLP waveform with 10 ns rising edge, 100 ns pulse width and 10 ns falling edge is used to simulate the HBM model. Avalanche and dynamic thermal model are added to the TCAD simulation. The ther-

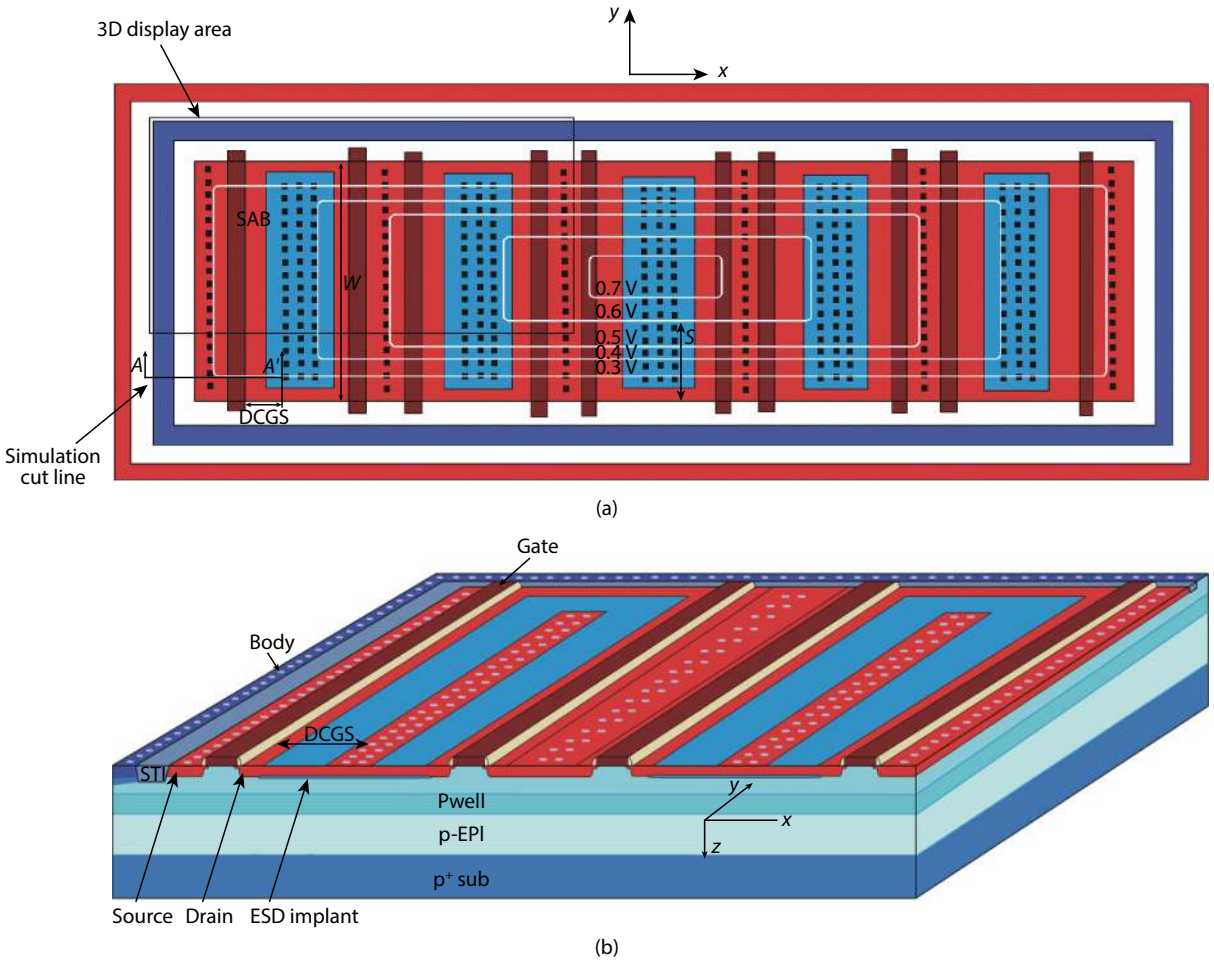

Fig. 5. (Color online) (a) Structure diagram of GGNMOS. (b) 3D display of GGNMOS device.

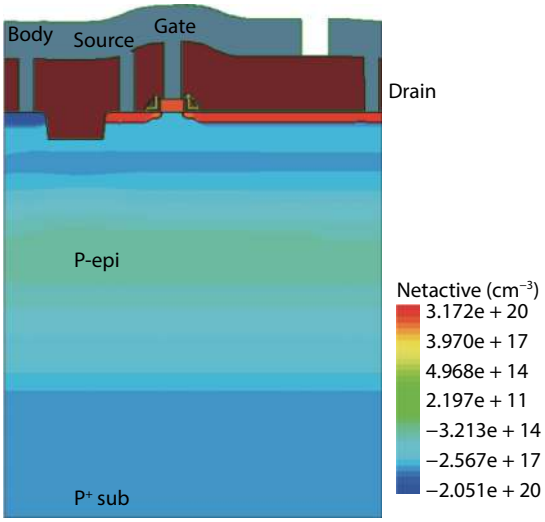

Fig. 6. (Color online) TCAD process simulation results of GGNMOS devices.

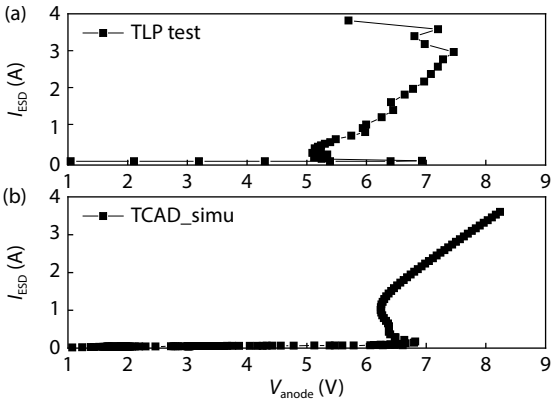

Fig. 7. Comparison of the TCAD and test structure GGNMOS TLP curve.

mal effect simulation of ESD high current stress in the protection device is realized[10]. In the thermodynamic model, Poisson's equation, electron and hole continuity equation and lattice heat flow equation need to be solved[11, 12].

The TLP curve of GGNMOS device simulated in Fig. 7 matches with the actual test TLP curve. The V_{t1} in 2D simulation is about 6.9 V, and it is similar to the measured TLP curve. the parasitic resistance of ESD discharge after LNPN startup is the same. It can be used for design and prediction of GGNMOS ESD performance.

In the TCAD simulation results shown in Fig. 8 below, the figures of three lines from top to bottom are the impact ionization, current density and lattice temperature diagrams, respectively. From left to right, it shows the situations before the *AB* line snap back, when the *BC* line snap back, after the *CD* line LNPN is turned on and when the *D* point reaches I_{t2} as described in Section 2.

According to the TLP simulation curve, it can be found that the trigger voltage V_{t1} increases with the increase of channel length (range 0.25–1.0 μm) (variation 0.8 V). The main reason is that with the increase of *L*, the base length of parasitic LNPN, the current gain decreases, and the trigger voltage in-

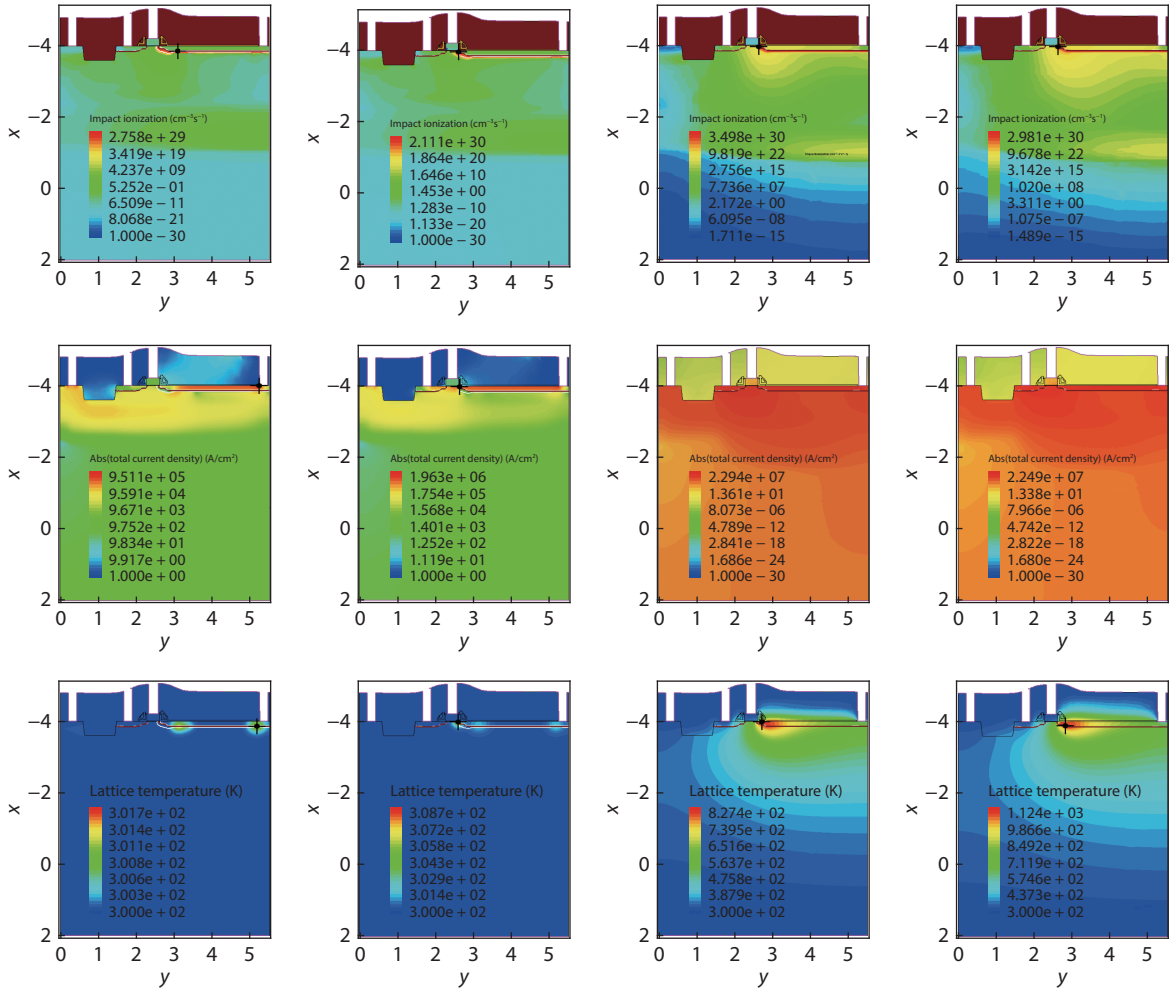

Fig. 8. (Color online) The impact ionization, current density and lattice temperature diagrams.

Table 1. The radiation-hardened 0.18 μm CMOS process characteristic parameters.

Item	Feature
Minimum feature size	0.18 μm undoped polysilicon gate
Operating voltage	Core device 1.8 V, IO device 3.3 V
Isolation technology	STI
Well structure	Double retrograded well
Spacer	Type LONO Spacer
Gate oxide	Dual gate oxide
Silicide	Fully self aligned $CoSi_2$ gate, source, drain
Interconnection	Aluminum interconnection with tungsten plug technology HDP low-K FSG IMD
Optional device	DN, HR, MIM optional
Reliability	$\geqslant$ 20 years
TID	$\geqslant$ 300 krad (Si)
SEL	$\geqslant$ 75 MeV·cm^2/mg
SEU	$\leqslant 1 \times 10^{-10}$ error /(bit·day) (with standard library)

creases. As the amplification coefficient of parasitic LNPN decreases, more impact ionization current is needed to maintain the collector current, which leads to the high power consumption and lattice temperature of ESD devices[13], which is not conducive to the release of ESD current.

In addition, when the size of DCGS increases with fixed channel length, the thermal volume is increased. Therefore when the same ESD current passes through the collector (drain), the lattice temperature is significantly reduced, which is conducive to bear more ESD current and improve the ESD performance. These results are shown in Fig. 9.

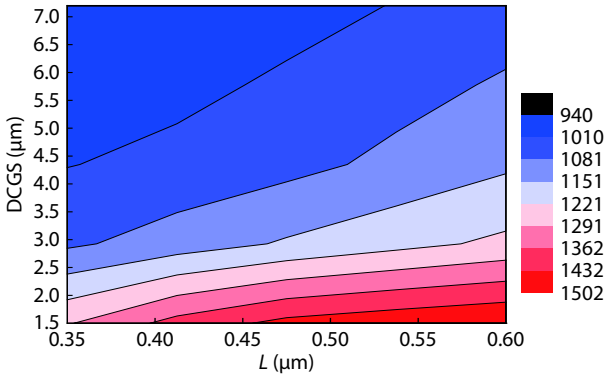

Fig. 9. (Color online) The influence of gate length and DCGS on the lattice temperature of GGNMOS.

4. Experimental result

The effects of different DCGS, number of multi finger and finger width on the ESD performance of GGNMOS devices are researched, and the different ESD ion implantation dose groups are compared. Finally, the ESD performance is veri-

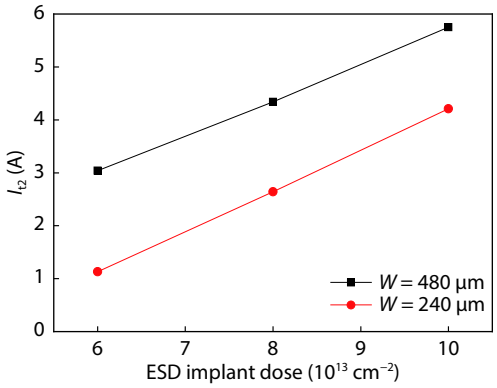

Fig. 10. (Color online) Effect of different ESD ion implantation dose on 3.3 V GGNMOS I_{t2}.

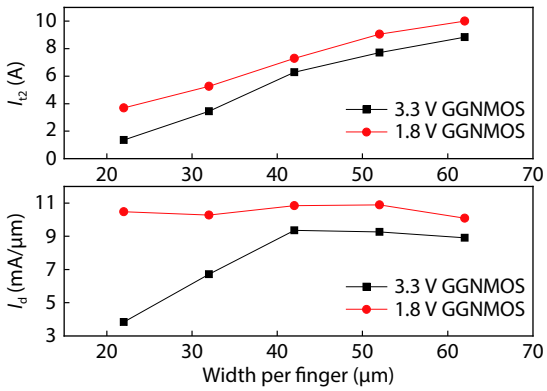

Fig. 11. (Color online) Influence of single finger width on ESD current.

fied by DSP circuit.

4.1. Effect of ESD ion implantation dose on the ESD performance of GGNMOS

In Fig. 10, 6 × 10^{13}, 8 × 10^{13}, and 1 × 10^{14} cm^{-2} dose of ESD ion implantation are used respectively. The test structure is 240 and 480 μm 3.3 V GGNMOS with the single finger width 40 μm and DCGS 1.9 μm. Different ion implantation doses significantly affected the discharge ability of GGNMOS in ESD events. For 240 μm test structure, I_{t2} was 1.13, 2.64, and 4.21 A, respectively, and for 480 μm test structure, I_{t2} was 3.04, 4.34, and 5.75 A, respectively. The overall width was doubled. It means that when the width was doubled, the magnification was 2.69, 1.64, and 1.36 for different ion implantation doses.

4.2. Influence of single finger width on ESD current

Fig. 11 shows core 1.8 V and IO 3.3 V GGNMOS devices with DCGS 1.9 μm, ESD ion implantation 8 × 10^{13} cm^{-2}, multi finger index 16. The value of I_{t2} in the figure above increases with the increase of width of single finger, which is mainly due to the increase of total width and ESD discharge path. In the figure below, the normalized discharge current per unit length of ESD is 4.5 mA/μm for 3.3 V GGNMOS device when the width of single finger is 22 μm, and the maximum discharge current is 9.36 mA/μm when the width of single finger is 42 μm. The normalized discharge current per unit length of 1.8 V GGNMOS devices are basically the same in the range of single finger width 22–62 μm. All of them are above 10.0 mA/μm. Therefore, when the single finger width of GGNMOS is 42 μm, the ESD release current efficiency is the best.

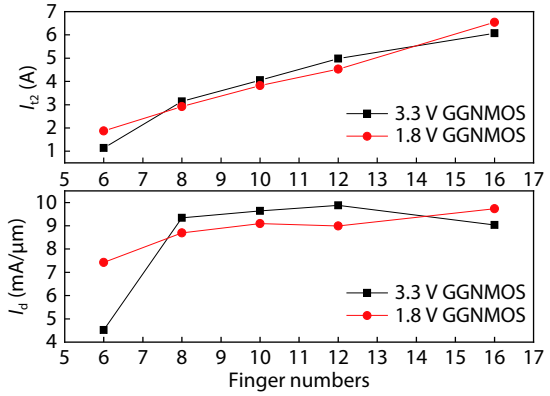

Fig. 12. (Color online) Influence of number of fingers on ESD current.

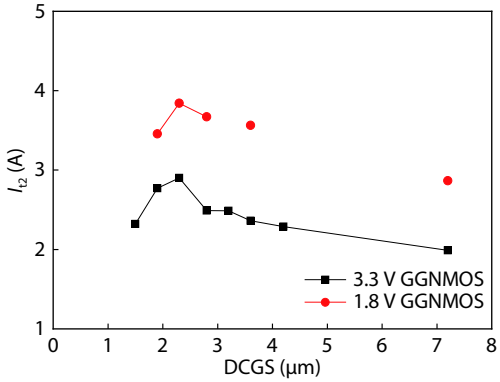

Fig. 13. (Color online) Effect of DCGS size on the ESD performance of GGNMOS.

4.3. Influence of multi finger number on the ESD performance of GGNMOS

The width of fixed single finger is 42 μm, ESD ion implantation of 6 × 10^{13} cm^{-2}, the number of fingers is changed from 6, 8, 10, 12, 16, and the total width is the product of the two. As shown in Fig. 12, the ESD current of 1.8 V GGNMOS device increases linearly with the increase of the total width, and the discharge efficiency per unit length also increases gradually, reaching a maximum of 9.73 mA/μm at 16 fingers. There is a difference between 3.3 V GGNMOS and 1.8 V. When the cross index is 6, the discharge efficiency is 4.52 mA/μm, and when the cross index is 12, the maximum discharge efficiency is 9.88 mA/μm.

4.4. Effect of DCGS size on the ESD performance of GGNMOS

In Fig. 13, the test structure adopts multi finger number of 6, single finger width of 40 μm, ESD ion implantation of 8 × 10^{13} cm^{-2}, and DCGS of different sizes. When the DCGS value is below 2.3 μm, the discharge current of GGNMOS increases with the increase of size. When the DCGS value is above 2.3 μm, the ESD discharge current decreases with the increase of the size. When the DCGS size is equal to 2.3 μm, the discharge current reaches the maximum value, the discharge efficiency of 3.3 V GGNMOS is 12.08 mA/μm, and 1.8 V GGNMOS is 16 mA/μm. The TLP curves are shown in Fig. 14.

4.5. Integrated circuit verification

Before GGNMOS device design optimization, the ESD capability of DSP circuit in HBM mode can only reach 1000 V, EMMI positioning of crystal input pin is conducted, and it is

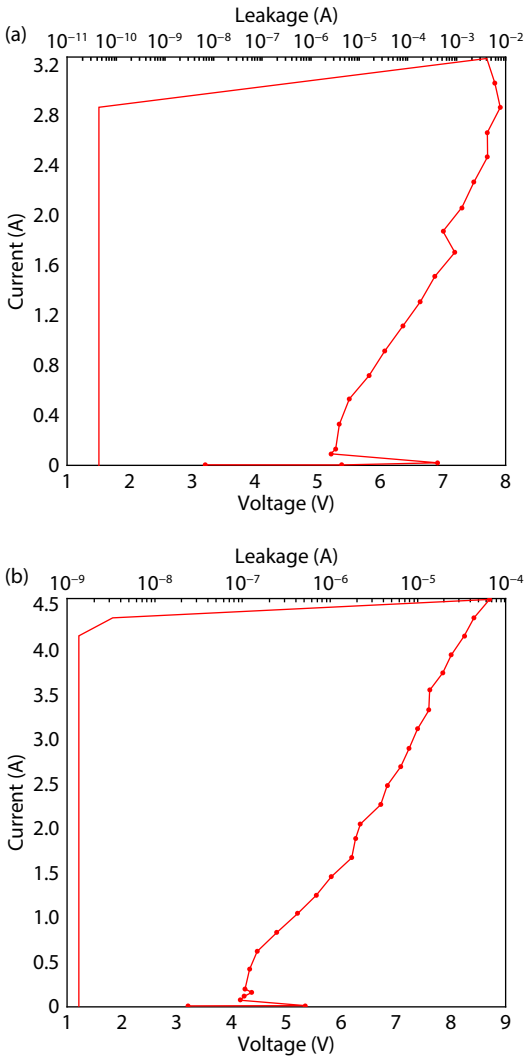

Fig. 14. (Color online) GGNMOS TLP curves with a total 240 μm width. (a) 3.3 V GGNMOS TLP I_{t2} = 2.9 A. (b) 1.8 V GGNMOS TLP I_{t2} = 3.84 A.

found that ESD current is short circuited to ground GGNMOS (the red area as shown in Fig. 15). The leakage current of other input and output pins increases. After GGNMOS optimization, the ESD capacity is increased to more than 3500 V.

The total ionization dose capacity of DSP circuit is verified by gamma ray, and the performance reaches 300 krad (Si). When the ESD performance is improved from 1000 to 3500 V, there is no TID degradation[14].

5. Analysis and discussion

With the increase of ESD ion implantation dose, the breakdown voltage of drain and body is reduced, which is conducive to the uniform opening of LNPN parasitic triode and the simultaneous opening of GGNMOS fingers[15, 16], which reduces the current density per unit area and keeps the lattice temperature lower under the same ESD current. In turn, more ESD current can be released under the same lattice temperature.

When the width of single finger is small, the ESD capacity increases linearly with the increase of width. When it reaches 42 μm, it basically reaches the maximum value of discharge efficiency per unit size. When the width of single finger continues to increase, the ESD discharge current can continue to increase, but the increased part cannot be effectively triggered, and the comprehensive discharge efficiency shows a downward trend. Therefore, a more effective method is to mirror a GGNMOS to increase the ESD discharge capacity.

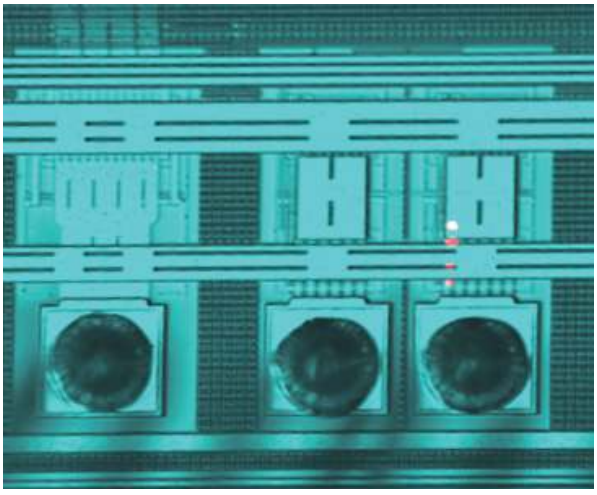

Fig. 15. (Color online) EMMI of DSP circuit pad ESD fails.

When the ESD implant dose is 6×10^{13} cm^{-2}, and the number of multi fingers is less than 8, the robustness of GGNMOS is poor, and its ESD discharge efficiency is at a low level. The main reason is that the body contact is relatively good. After large injection, the large area source body junction cannot be forwarded. The large ESD current in the central area causes lattice burnout. When the number of multi fingers is more than 8, the area of the triggered central area increases, the ESD current per unit area decreases and more current can be released before the lattice burns down.

In the same GGNMOS device layout, compared with the traditional bulk silicon CMOS technology, the introduction of epitaxial layer increases the state of body contact and leads to the degeneration of ESD performance. In the GGNMOS structure as shown in Fig. 5(b), when the ESD event comes, the drain end will generate PN junction breakdown, and a large number of hole carriers will be injected into the body region (pwell, p-epi, p$^+$ sub). Due to the introduction of p$^+$ sub, the current in the *z*-axis direction will increase, but due to the decrease of resistance, the body potential cannot reach the previous level under the same hole carrier injection condition. In addition, the introduction of p$^+$ sub reduces the transverse parasitic resistance, reduces the barrier voltage drop in the *x*-axis and *y*-axis direction to a range of 0.6–0.7 V (as shown in the ring area in Fig. 5(a)), and finally reduces the ability of the whole GGNMOS to release current in ESD events. By increasing the single finger width (*y*-axis direction), the hole carrier injection current is increased, the barrier voltage drop is increased to 0.6–0.7 V, the width near the contact area of the outer P$^+$ ring (body in Fig. 5(b)) that can not effectively start the LNPN (as shown in the letter S in Fig. 5(a)), and the discharge efficiency of GGNMOS device is increased.

When the DCGS value increases from 1.5 μm, the reverse biased drain junction capacitance at the drain end under the forward ESD stress will increase[6], and the parasitic resistance at the drain end will increase, which will help to expand the ESD current distribution along the single finger width more evenly, which is shown as the increase of the ESD

Table 2. Comparison with literature.

GGNMOS device	Single finger width (μm)	Multi finger number	Total width (μm)	V_{t2} (V)	I_{t2} (A)	Discharge efficiency I_{esd} (mA/μm)	Reference
3.3 V[a]	40	6	240	7.60	2.90	12.08	/
1.8 V[a]	40	6	240	8.61	3.84	16.0	/
1.8 V	40	8	320	20.27	4.55	14.2	[17]
3.3 V	60	6	360	/	3 (⩾ 4500 V)	8.33	[18]
3.3 V	30	12	360	/	1 (⩾ 1500 V)	2.78	[18]
3.3 V	60	12	720	/	3 (⩾ 8000 V)	7.4	[18]
3.3 V	90	8	720	5.24	5.17	7.18	[19]
1.8 V	/	/	/	/	/	9.1[b]	[1]
3.3 V	/	/	/	/	/	8.1[b]	[1]

[a] Indicate this work. [b] Published literature, Fig. 16.

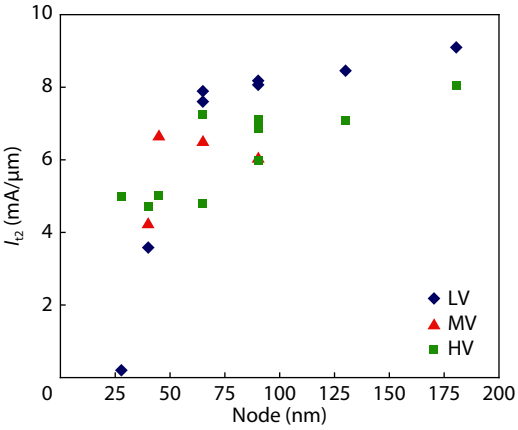

Fig. 16. (Color online) GGNMOS I_{t2} value versus process nodes.

discharge capacity. When the DCGS value reaches 2.3 μm, increasing the size will lead to the increase of the drain parasitic resistance, showing a significant voltage drop. As a result, the voltage on the gate oxide layer at the input is increased, and this trend becomes more obvious as the DCGS value continues to increase, resulting in the overall GGNMOS ESD capability decline.

Through these simulations and experimental TLP tests, it is necessary to combine the gate length, single finger width, multi finger number, DCGS, ESD ion implantation and other factors of GGNMOS. These factors are interactive and need further experimental design to optimize ESD performance. In addition, good ESD protection quality also includes several parameters that need to be considered in application, such as capacitance, leakage current, power sequencing and overvoltage conditioning etc. The ESD device or clamp should not have too much capacitance that it violates the loading limits of the I/O signaling specification. It must not draw excessive current at either high or low input or output levels. In addition, it must be compatible with normal sequence for applying power, and it can survive for a period of time under the condition of over voltage. Therefore, test structures for benchmarking the ESD robustness of different CMOS process, so as to get an excellent ESD capability.

Compared with the ESD performance of GGNMOS devices found in the relevant literature, the performance of GGNMOS devices finally achieved in this work has achieved a good level, the discharge efficiency of 3.3 V GGNMOS is 12.08 mA/μm, and 1.8 V GGNMOS is 16 mA/μm. The details are shown in Table 2.

6. Conclusion

The ESD performance of GGNMOS protection device is affected by many factors such as layout[20] and technology[21]. When determining the structure of GGNMOS, it is necessary to design and verify the key elements such as gate length, DCGS, multi finger index, single finger width, ESD ion implantation, etc. Through the process simulation, TLP test, circuit ESD verification, the radiation hardened 0.18 μm bulk silicon CMOS process platform adopts the optimized GGNMOS structure ESD protection device. The HBM mode reaches the level of 3500 V.

Acknowledgements

This work was supported by the Military Quality Engineering of China (No. 1807WR0002).

References

[1] Kepens B. On-chip ESD solutions seminar. SOFICS, Shanghai, 2015
[2] Xie R B, Ji X M, Wu J W. Research on ESD performance of devices in radiation hardening process. Microprocessors, 2019, 40, 1
[3] Wang A Z H. On-chip ESD protection for integrated circuits: An IC design perspective. Springer Science & Business Media, 2006
[4] Zhang L Z, Wang Y, Wang Y Z, et al. Insight into multiple-triggering effect in DTSCRs for ESD protection. J Semicond, 2017, 38, 075001
[5] Bi X W, Liang H L, Gu X F, et al. Design of novel DDSCR with embedded PNP structure for ESD protection. J Semicond, 2015, 36, 124007
[6] Mohan N, Kumar A. ESD protection design methodology in deep sub-micron CMOS technologies. Project Report, Course E&CE 730 (Topic 9), 2003, 5
[7] Jiang Y X, Li J, Ran F, et al. Influence of layout parameters on snapback characteristic for a gate-grounded NMOS device in 0.13-μm silicide CMOS technology. J Semicond, 2009, 30, 084007
[8] Chen T Y, Ker M D. Analysis on the dependence of layout parameters on ESD robustness of CMOS devices for manufacturing in deep-submicron CMOS process. IEEE Trans Semicond Manuf, 2003, 16, 486
[9] Do K I, Park J G, Kwon M J, et al. Analysis of GGNMOS-based ESD protection device using DCGS variation with robustness. Academic Conference of Korean Institute of Electronic Engineering, 2016, 6, 74
[10] Krabbenborg B, Beltman R, Wolbert P, et al. Physics of electrothermal effects in ESD protection devices. J Electrost, 1992, 28, 285
[11] Chen J Z, Zhang X Y, Amerasekera A, et al. Design and layout of a

high ESD performance NPN structure for submicron BiCMOS/bipolar circuits. Proceedings of International Reliability Physics Symposium, 1996

[12] Ker M D, Chen T Y. Substrate-triggered technique for on-chip ESD protection design in a 0.18-μm salicided CMOS process. IEEE Trans Electron Devices, 2003, 50, 1050

[13] Wu D X, Jiang L L, Fan H, et al. Analysis on the positive dependence of channel length on ESD failure current of a GGNMOS in a 5 V CMOS. J Semicond, 2013, 34, 024004

[14] Wu J W, Yu Z G, Hong G S, et al. A method for strengthening the total ionizing dose of 0.18 μm bulk CMOS process. 2018 International Conference on Radiation Effects of Electronic Devices, 2018

[15] Paul M, Russ C, Kumar B S, et al. Physics of current filamentation in ggNMOS devices under ESD condition revisited. IEEE Trans Electron Devices, 2018, 65, 2981

[16] Wang Y, Lu G Y, Wang Y Z, et al. Power-rail ESD clamp circuit with parasitic-BJT and channel parallel shunt paths to achieve enhanced robustness. IEICE Trans Electron, 2017, E100.C, 344

[17] Li L, Zhu K H. ESD performance analysis of gate grounded NMOS devices. Electron Pack, 2011, 11, 18

[18] Li Z G, Yue S G, Sun Y Z. Research on ESD device design of deep submicron IC. The 16th National Conference on Silicon Materials for Semiconductor Integrated circuits, 2009

[19] Li Z G, Yue S G, Sun Y S. GDNMOS design for ESD protection in submicron CMOS VLSI. 2009 Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics, 2009, 432

[20] Shi J. Deep sub-micron ESD GGNMOS layout design and optimization. MATEC Web Conf, 2018, 198, 04009

[21] Boschke R, Chen S H, Scholz M, et al. ESD ballasting of Ge FinFET ggNMOS devices. 2017 IEEE International Reliability Physics Symposium (IRPS) – Monterey, 2017