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A 16-bit 1 MSPS SAR ADC with foreground calibration and residual voltage shift strategy

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Abstract: In this paper, a 16-bit 1MSPS foreground calibration successive approximation register analog-to-digital converter (SAR ADC) is developed by the CMOS 0.25 μm process. An on-chip all-digital foreground weights calibration technique integrating self-calibration weight measurement with PN port auto-balance technique is designed to improve the performance and lower the costs of the developed SAR ADC. The SAR ADC has a chip area of 2.7 × 2.4 mm^2, and consumes only 100 μW at the 2.5 V supply voltage with 100 KSPS. The INL and DNL are both less than 0.5 LSB.

Key words: foreground all-digital calibration; RS strategy; RS-based dither; auto-zero comparator; SAR ADC

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1. Introduction

With the increasing application of biological and wireless sensing techniques, the 16-bit 1 MSPS SAR ADC has a huge market with big potential and wide prospects. Due to the rapid development of CMOS process technology, SAR ADC has become a hot spot in the ADC design field[1]. Since a large number of sensor nodes are embedded in the environment, the chip must be cheap enough[2]. Currently, ADCs with the effective number of bits (ENOBs) less than 10 meet the application requirements of basic sensors, while ADCs with resolution exceeding 10 bits are necessary for more complex sensor systems, such as EEG and ECG monitoring in biological applications, and temperature, pressure and humidity monitoring in environmental applications[3]. The on-chip self-calibration and automatic adjustment technique can improve the ENOBs and lower the costs of the SAR ADC, while fault tolerance strategies such as redundant CDAC and the voltage shift (RS) strategy can ensure the robustness of the final design in the conversion process. In this paper, the RS strategy is proposed to further improve the ADC performance, such as promoting the noise floor and correcting the linearity errors.

The second part of this paper introduces the ADC system and detailed circuit implementation. The RS strategy and RS-based dither are described in the third part. The on-chip all-digital foreground weights calibration technique is illustrated in detail in the fourth part. The layout and simulation results are shown in the fifth part.

2. System and circuits implementation

The system architecture of the all-digital foreground self-calibration 16-bit 1 MSPS SAR ADC is shown in Fig. 1, which consists of a carefully designed sample-and-hold capacitor digital-to-analog converter (S/H CDAC), a high-performance comparator, and an innovative digital logic circuit. The digital logic circuit consists of a SAR logic circuit, a calibration logic circuit, and a serial peripheral interface (SPI) circuit. The analog part and digital part of the SAR ADC can cooperate seamlessly as a whole. To meet the requirements of wide input voltage range, low power consumption, ease-of-use and small area, three power supplies are used in this design. The reference voltage (V_{ref}) is from 2.5 to 5 V. The logic circuits are supplied at 2.5 V (V_{dd}). The interface supply voltage (V_{io}) is from 1.8 to 3.3 V. In the design, the Gnd of V_{ref}, V_{dd} and V_{io} is strictly separated to reduce the interaction between the digital module and the analog module. The variable V_{ref} can deliver a more flexible signal input range. Similarly, the variable V_{io} is convenient for users to choose the operating voltage of digital logic without a complex level conversion structure. Internally, the digital logic, the SAR logic and the control logic of the analog parts use V_{dd} (2.5 V) for power supply; thus, these circuits can be designed with the smallest

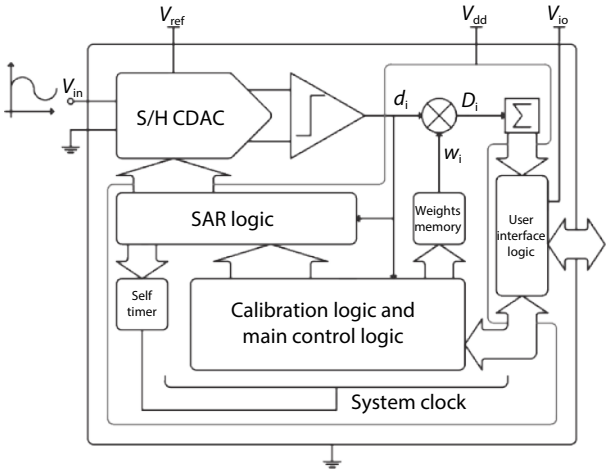

Fig. 1. The ADC system architecture.

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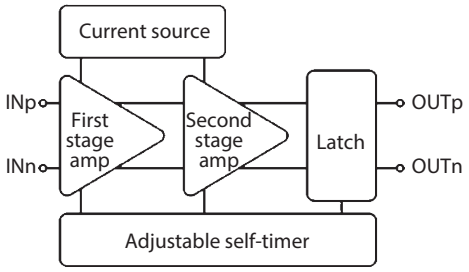

Fig. 2. Comparator block diagram.

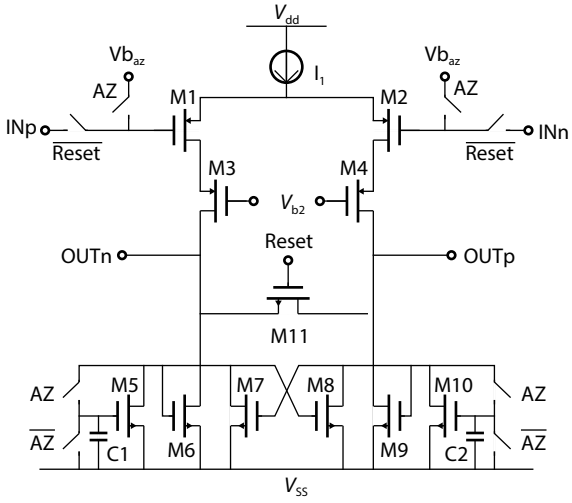

Fig. 3. Preamplifier.

size of the process. V_{dd} and V_{io} are used in digital modules, so the performances of V_{dd} or V_{io} do not affect the conversion accuracy. In utilization, users can choose to provide three different power supplies to get the best performance, or they can use only 2.5 V power supply to simply drive this design. The calibration process starts automatically and the results are saved in the weight memory when the ADC is powered on. Then, the input signal can be converted correctly by using the weight values in the memory, and the final converted digital values are sent out to the following device through SPI. The high-performance self-timer comparator, SAR control logic, CDAC, and dither are introduced in detail in the following section.

2.1. High-performance self-timer comparator

The conversion result depends on the accuracy of the comparator, which is influenced by many factors, such as area, power consumption, noise, offset, and settling time[4–6]. The comparator of this design consists of a bias current source, a two-stage preamplifier, a dynamic latch, and an adjustable clock generator. The adjustable self-timer generates the clock with variable frequencies and variable duty cycles to drive the comparator and SAR logic circuits. The main structure of the comparator is shown in Fig. 2.

In the designed SAR ADC, an auto-zero[7] two-stage preamplifier[8] is applied, which provides the enough gain for the comparator, and thereby renders high resolution to the comparator. The structures of the first preamplifier stage and the second preamplifier stage are the same, as shown in Fig. 3. In the 16-bit SAR ADC, it is important to achieve a high-resolution comparator. Therefore, a two-stage preamplifier is used to provide enough gains to improve the resolution of the comparator. When a two-stage preamplifier is used,

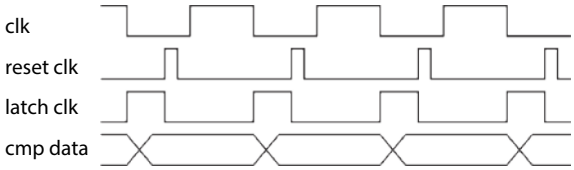

Fig. 4. Multiphase clock of the self-timer.

the offset of the first-stage amplifier is amplified by the second-stage. The offset voltage of the comparator varies with the change of the operating temperature and voltage, which affects the calibration process and conversion process. During the conversion process, an offset voltage that is too high reduces the dynamic range and increases the misjudgment. During the calibration process, an offset voltage that is too high causes failures of calibration. As a rule of thumb, the auto-zero technique allows the comparator to considerably reduce the offset to the order of a few microvolts and the offset drift to the order of a few tenths of microvolts per degree centigrade. Switches AZ and $\overline{AZ}$ are turned on to store Vb_{az} in capacitors C1 and C2 at first. At the end of the auto-zero process, AZ and $\overline{AZ}$ are turned off, and the comparator enters normal working conditions. To reduce the offset error, the top plates of C1 and C2 are connected to the gates of M5 and M10 respectively to maintain the potential of the output nodes OUT_n and OUT_p. As shown in Fig. 4, the comparator compares two inputs INp and INn at the rising edge of the clock (clk). The stable output of the two-stage amplifier is latched at the end of the comparison. Before a new round of comparison, the comparator is reset in the reset phase.

2.2. S/H CDAC

Ref. [9] elaborates on the advantages of a split CDAC, and the three-segment CDAC applied in Ref. [8] is reported to have great advantages in SAR ADCs with 12 bits or more. The proposed design adopts a differential three-segment CDAC, which effectively optimizes the area and setting time of the capacitor. The half structure is shown in Fig. 5. Considering KT/C_{in} noise[10] and linearity limits[11], the sampling capacitor value, sampling time and sampling transmission gate size are selected carefully. The high-segment capacitor sampling technique is used in this design to tradeoff between the sampling capacitor area and noise performance. A sub-min-unit capacitor array is added to the lower part of the capacitor array to enhance the accuracy of calibration digital weights. The output voltage of the CDAC can be expressed by Eq. (1)[12].

$$V_{out} = \sum_{i=0}^{N} W_i D_i + V_{com} - V_{in}. \tag{1}$$

All of the capacitors except C_{B1} and C_{B2} are weights capacitors. C_{B1} and C_{B2} are the bridge capacitors. The output voltage is the sum of the weighted voltages which are set to V_{ref}. The weights w_i are calculated by using Eq. (2) and Table 1. The subscript *H*, *M*, and *L* represent the serial number of the weight capacitor segments. $R_{[H,M,L]}$ is the proportion coefficient in each segment. The $C_{eq[H,M,L]}$ is the equivalent capacitance induced by the bridge capacitor. The $C_{t[H,M,L]}$ is the total capacitance in segments *H*, *M*, and *L*.

$$w_i = R_{[H,M,L]} \frac{C_i}{C_{t[H,M,L]} - C_i + C_{eq[H,M,L]}} V_{ref}. \tag{2}$$

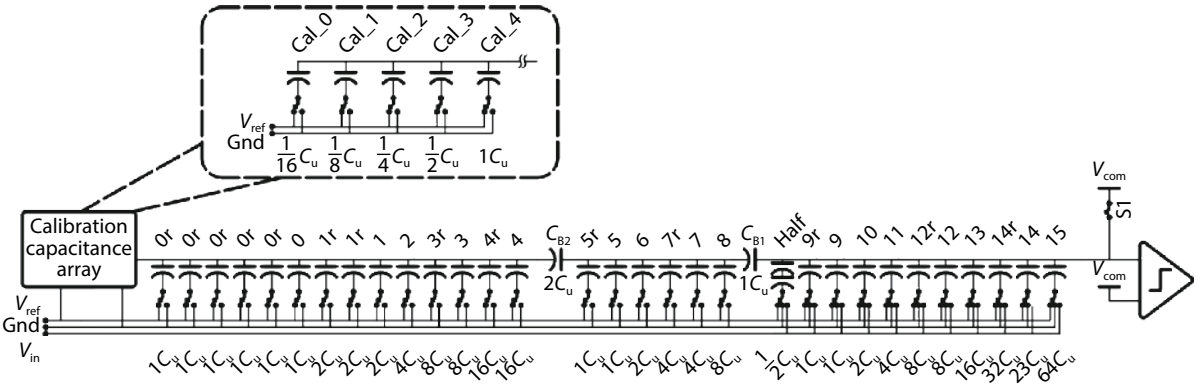

Fig. 5. The schematic of half CDAC.

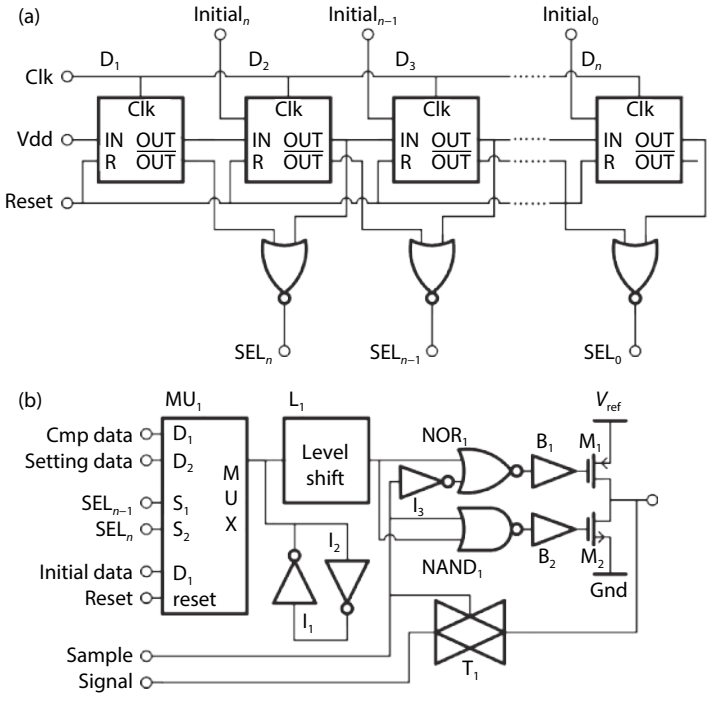

Fig. 6. (a) Control logic circuit. (b) High-segment MUX switch circuit.

Table 1. Weight calculation.

$R_{[H,M,L]}$	$C_{eq[H,M,L]}$
$R_H = 1$	$C_{eq[H]} = \dfrac{C_{B1} + C_{t[M]}}{C_{B1}C_{t[M]}}$
$R_{[M]} = R_H \dfrac{C_{B1}}{C_{t[H]}}$	$C_{eq[M]} = \dfrac{C_{B1} + C_{t[H]}}{C_{B1}C_{t[H]}} + \dfrac{C_{B2} + C_{t[L]}}{C_{B2}C_{t[L]}}$
$R_{[L]} = R_{[M]} \dfrac{C_{B2}}{C_{t[M]}}$	$C_{eq[L]} = \dfrac{C_{B2} + C_{t[L]}}{C_{B2}C_{t[L]}}$

2.3. SAR control logic

Fig. 6(a) illustrates the simplified SAR control logic circuits[13–15], which are mainly composed of a traditional selection logic circuit and a MUX switch circuit in this design. The selection logic circuit and the MUX switch circuit requiring a tradeoff between the speed and the power consumption are carefully designed.

During the conversion process, SEL_n outputs high potentials one by one to control the corresponding MUX switch circuit to set and latch the comparison results. The high-segment MUX switches are implemented, as shown in Fig. 6(b). When preparing for the on-chip calibration, the MU_1 module is set to its initial value (1 or 0). The initial values, the setting state, and the comparison results are saved in the latch that consists of inverters I_1 and I_2. During the sampling phase, M_1 and M_2 are turned off while T_1 is turned on. At the end of the sampling phase, the input signal is saved in the top plate of the sampling capacitors. Delay circuits B_1 and B_2 are used for generating dead time to avoid simultaneous conduction of M_1 and M_2.

3. Residual voltage shift strategy and RS-based dither

3.1. Residual voltage shift strategy

The conversion errors are induced by clock jitter, comparator misjudgment, setting errors, and reference voltage noises. The conversion fault tolerance can be effectively improved by adding appropriate redundant bits in the CDAC[16, 17]. However, the redundant bits technique cannot

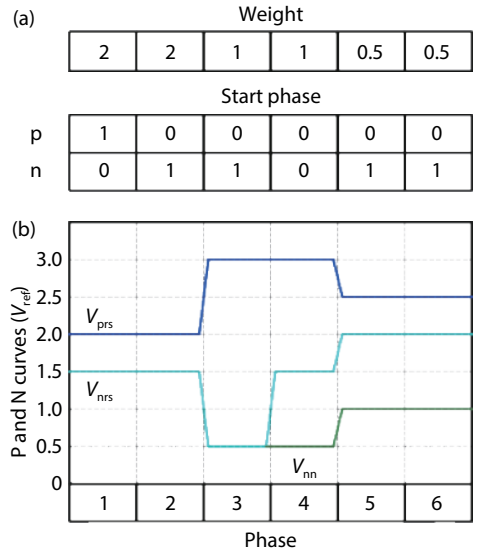

Fig. 7. (a) Weights of a 6 phase SAR ADC and the start phase. (b) Residual voltage curves of P and N curves.

resolve all of the above errors completely. For example, some reasons cause the residual voltage to rise, even if all the remaining bits are set to a state where the residual voltage drops, the residual voltage cannot return to the correct state. So, the residual voltage shift strategy (RS) is used to improve fault tolerance. Fig. 7(a) illustrates the weights of a 6 phase SAR ADC that is used to analyze the RS strategy. In the startup state of the conservative switch method, except the MSB, all other bits are set to a state that the P terminal is 0 (connected to Gnd) and the n terminal is 1 (connected to V_{ref}). The startup state after the RS strategy is added as shown in Fig. 7(a). Both P and N of those bits that are selected as the RS bits are set to 0 (connected to Gnd). In the conversion process, the RS bit is used in the same way as the normal bit.

Three redundant bits and an RS bit are added to improve the fault tolerance of the 6 phase SAR ADC. Fig. 7(a) shows the start phase of the conversion process, and the 4th bit of the 6 phase SAR ADC is selected to work as RS bit. In the Fig. 7(a), 1 represents that this bit is set to V_{ref}, and 0 represents that this bit is set to Gnd. Fig. 7(b) shows the P terminal voltage curve V_{prs} and N terminal voltage curve V_{nrs} of the CDAC. V_{nn} is the voltage curve of the CDAC without RS strategy. After the 4th bit, the voltage difference between V_{nrs} and V_{nn} is the pre-offset voltage which is generated by the RS bit. At the end of the conversion process, the RS strategy helps the 6 phase SAR ADC to reduce the residual voltage. Figs. 8(a) and 8(b) show the endpoint residue voltage of the 6 phase SAR ADC with RS strategy (the RS values) and without RS strategy (normal values). In Fig. 8(a), the error decision occurs in the third bit. In Fig. 8(b), the error decision occurs in the second bit. It can be seen that the RS strategy helps to correct residual voltage errors and no new errors are introduced.

Fig. 9 shows the relationship between the number of the RS bits and the noise floor level with10 kHz sine signal input. The noise floor level can be optimized effectively by adding an appropriate RS bit during the conversion process.

The four residual voltage curves of the same input signal are shown in Fig. 10(a). The error resident curve 1 is the

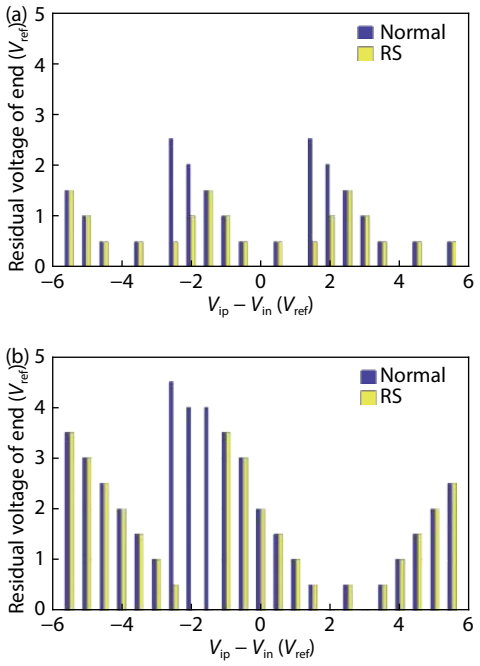

Fig. 8. (Color online) (a) Simulation residual voltage with third bit error. (b) Simulation residual voltage with second bit error.

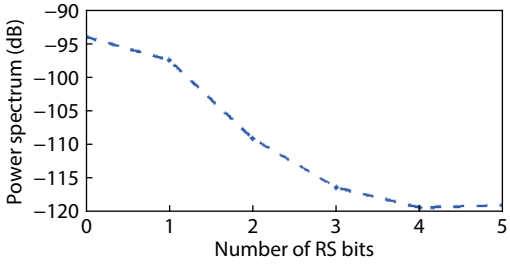

Fig. 9. Simulated noise floor level versus number of RS bits.

nonideal case with RS strategy and the error happens in the 13th bit. The error resident curve 2 is the case with misjudgment due to the insufficient residual voltage and the error happens in the 9th bit. After point P_1, the error residual curve 1 emerges an erroneous rise because an error decision is produced in 13th bit. The RS bits help the error residual curve 1 to drop to the ideal residual voltage curve when the 12R bit decision is over. This additional falling portion is the pre-offset voltage of the 12th bit. These additional drops help the residual curve return to a correct range that is close to the ideal residual curve. Actually, the error resident curve 1 returns back to a correct range when the 11th bit trial is complete, which means the previous mentioned error is resolved. The error residual curve 2 shows the residual curve without RS strategy. The error residual curve 2 shows a continuous drop after the error point P_2, but the continuous drop still cannot correct the residual voltage. In fact, the error like P_2 may occur not only in the 9th bit but also in the 9R bit. The 9th weight is the same as the weight of 9R bit. So, the location of the residual curve remains unchanged when the 9th bit is compared with 9R bit. Though the residual curve remains unchanged, the weight capacitors are still charged and discharged with the potential errors.

The first function of the RS strategy is used to correct the error caused by the insufficient rise of the residual curve dur-

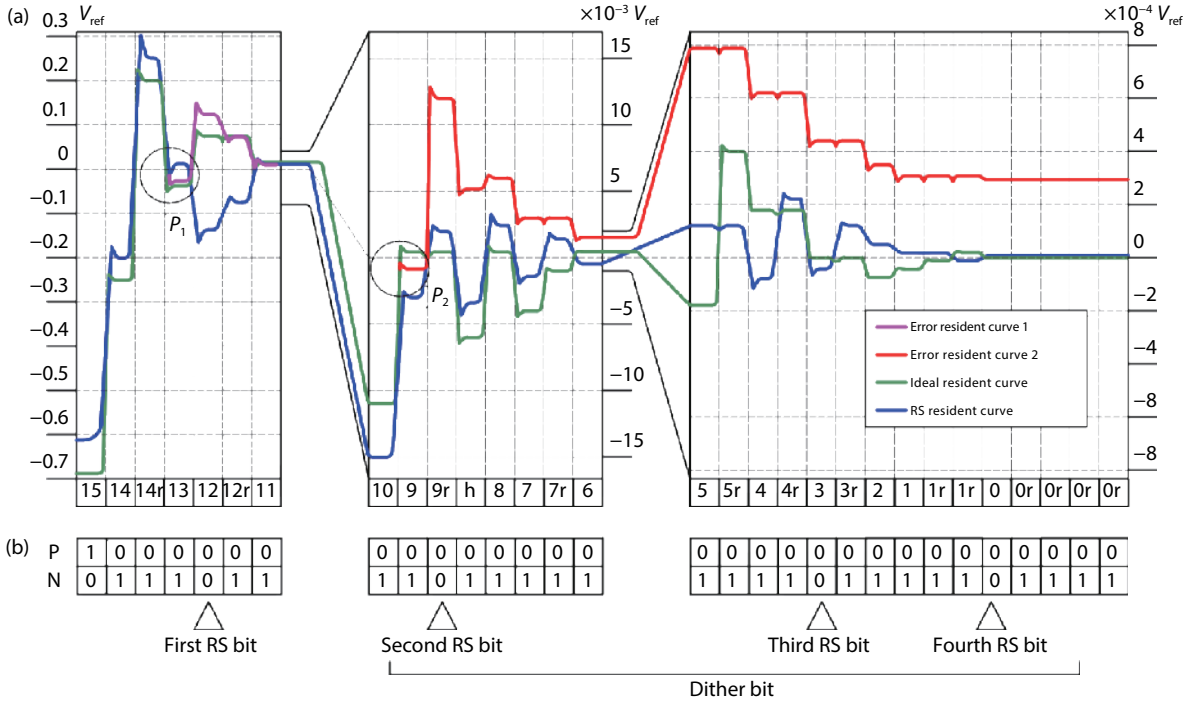

Fig. 10. (Color online) (a) Residual voltage curves. (b) Start phase and RS bits.

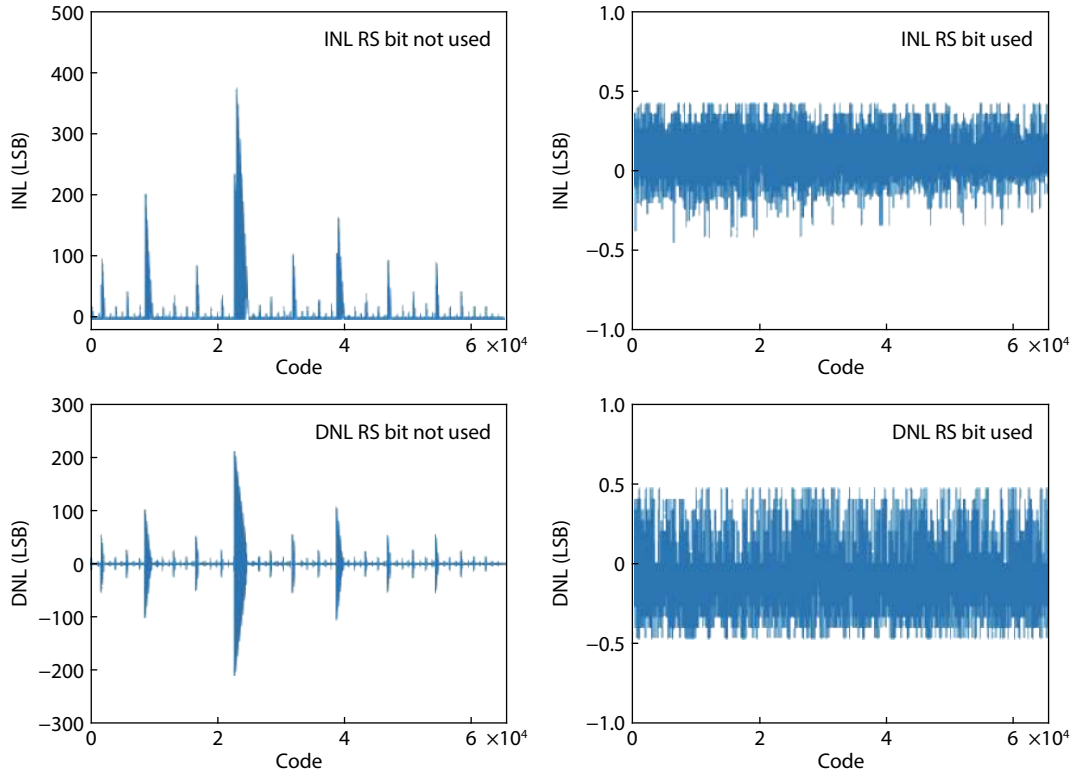

Fig. 11. (Color online) Simulated INL and DNL with/without RS strategy.

ing the setting phase. The second function of the RS strategy is used to dynamically change the residual voltage to reduce the comparator decision error. During the conversion process, the irrevocable mistake decision emerges easily in the first previous bits because the first previous bits decision time and setting time are shorter than the later bits. Since the decision error caused by the insufficient rise of the residual curve is proportional to weight error, an earlier insufficient rise error may cause a larger conversion error. The position and weight of redundant bits are obtained after detailed analysis, so better results can be achieved when the RS bit is added to the redundant bit. On the other hand, the situation that the comparator repeats the decision of the small and indistinguishable input voltage is reduced when the RS bit is added to the redundant bit. The start-up state after adding the RS bit is shown in Fig. 10(b). Fig. 11 shows the INL

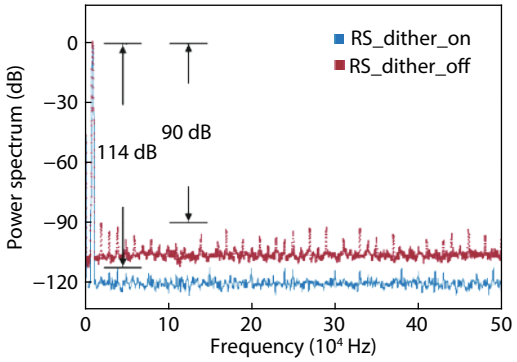

Fig. 12. (Color online) Simulated noise floor with/without RS-based dither.

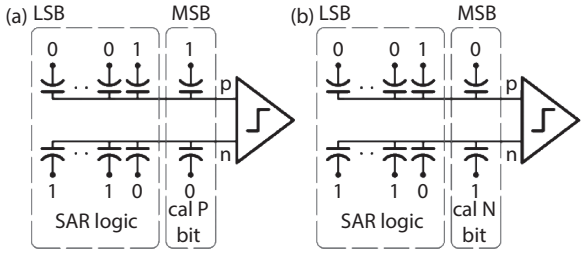

Fig. 13. (a) Calibration start phase of the P bits (b) Calibration start phase of the N bits.

and DNL with/without RS bits. It can be seen that the RS strategy reduces INL errors and DNL errors effectively in the unideal environment.

3.2. RS-based dither

Nonlinearity error caused by capacitance mismatch of the CDAC degrades SNDR and SFDR, because the error appears as spurs of ADC output spectrum[18, 19]. Dither technology allows a particular offset to affect all inputs on average. Traditionally, dither technique using a pseudo-random sequence drives the dither signal bit to add dither signal in the analog domain and then the dither value is subtracted in the digital domain to affect the transfer function of the converter[20]. When the dither bit is driven by a pseudo-random sequence, the time-domain stability of the SAR ADC transfer function is broken by the dither bit. Therefore, during simultaneous sampling, the dither technology can optimize the SFDR and SNR performance of the SAR ADC [21].

An all-analog dither technique is proposed in this paper. The second RS bit, third RS bit, and fourth RS bit are used to work as the dither bits in this design. The pseudo-random sequence drives the dither bits to affect the transfer function. In the conversion process, dither bits can be set to the RS bits value when the previous RS dither bit is settled to the comparison result. The conversion results are influenced by the RS dither bits. The RS dither bits are used like normal bits throughout the conversion process, so the digital result does not need to subtract the weights of dither bits. The non-ideal factors such as noise and comparator offset are added in the simulation. As shown in Fig. 12, it can be seen that the noise floor of the SAR ADC with RS-based dither is better than that without RS-based dither.

4. Calibration

Refs. [8, 22, 23] employ an all-digital foreground calibration technique, which uses the less significant bits to measure more significant bits. The 5th bit is the first calibration bit in this design. The detailed calibration process of P and N terminals of the 5th bit is as follows. Firstly, the P terminal of the 5th bit is set to V_{ref} and then measured by the 5R bit to LSB. Secondly, the N terminal of the 5th bit is measured as the P terminal of the 5th bit. After single-ended weights $W_{[i]p}$ and $W_{[i]n}$ are calculated according to Eqs. (3) and (4), $W_{cal[i]}$ is computed and taken as the final weight used in the conversion process. Taking the MSB as an example, the weight of the MSB is measured by the second MSB to the LSB. The initial phase of the calibration process is shown in Figs. 13(a) and 13(b). After obtaining the single-ended results of the MSB on the P and N sides by Eqs. (3) and (4), the MSB weight is calculated according to Eq. (5).

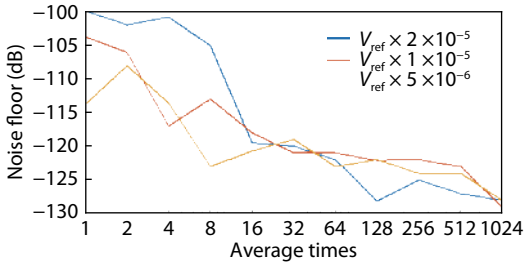

Fig. 14. (Color online) Simulated noise floor level versus average number.

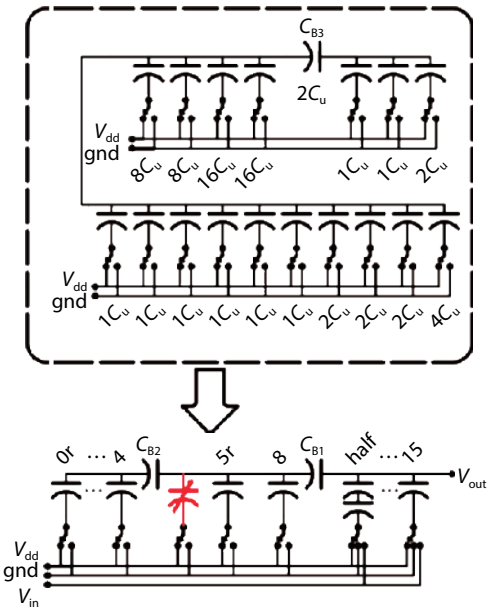

Fig. 15. Auto-balance circuit.

$$W_{[i]p} = \sum_{j=0}^{i-1} Dp_j W_j + os, \tag{3}$$

$$W_{[i]n} = -\sum_{j=0}^{i-1} Dn_j W_j + os, \tag{4}$$

$$W_{cal[i]} = \frac{W_{[i]p} - W_{[i]n}}{2} = \frac{\sum_{j=0}^{i-1} Dp_j W_j + \sum_{j=0}^{i-1} Dn_j W_j}{2}. \tag{5}$$

Affected by the noise, the single calibration result may be hard to meet the requirements of a 16-bit resolution. Therefore, it is necessary to make multiple measurements and take

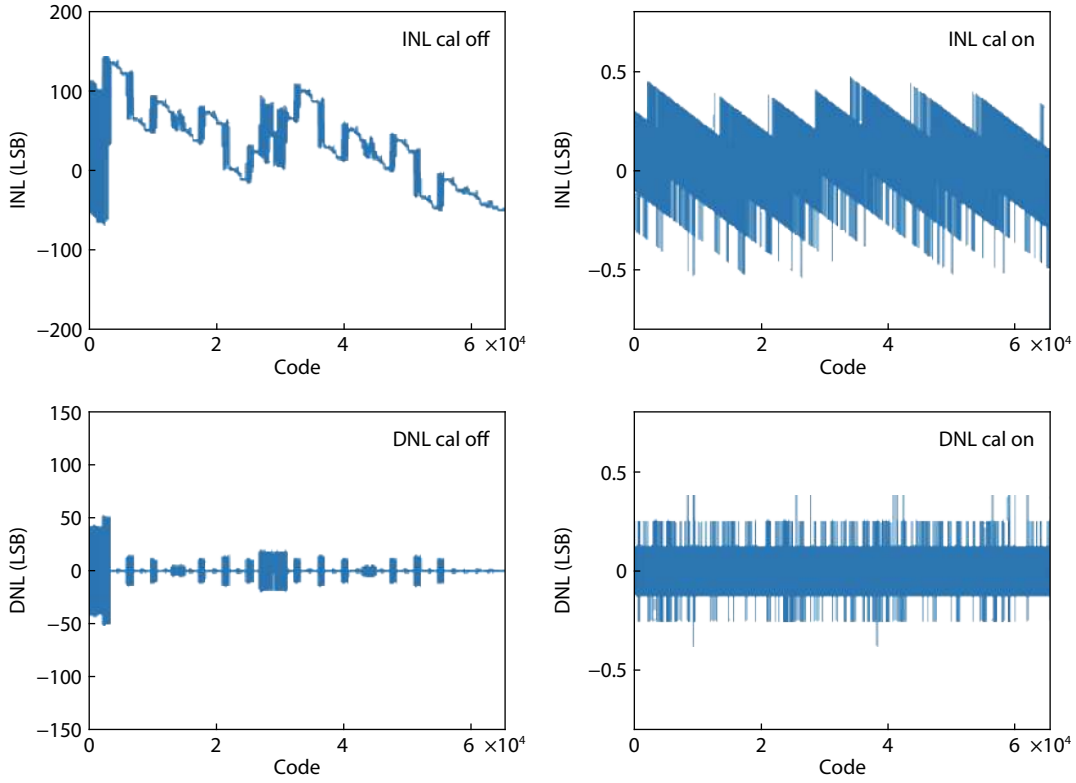

Fig. 16. (Color online) Simulated results of INL and DNL with/without calibration.

the average as the final result to reduce the influence of noise. Multiple measurements are made for each weight to reduce the effects of the noise[8]. Fig. 14 shows the relationship between calibration accuracy and the number of average times with 10 kHz sine signal input. When the average times are 32, the calibrated result meets the requirement of the noise floor at –120 dB in different noise environments.

In practice, the mismatch causes a mismatch voltage of CDAC between the P and N terminals, and when the mismatch voltage is greater than the sum of weights of 5th bits to LSB, the calibration process fails. Therefore, an auto-balance strategy is added in the second segment of the CDAC to remove the mismatch voltage in this design. The simplified automatic balance CDAC is shown in Fig. 15. The auto-balance strategy adjusts the mismatch voltage between P and N terminals of the CDAC to less than 1 LSB before the calibration process.

In the self-measurement calibration technique, the digital weights of lower six bits are specified, so the calibrated digital weights fluctuate with the capacitance mismatch. This phenomenon causes serious gain errors. Therefore, the automatic gain adjustment is required to reduce the gain error. Eq. (6) gives the calculation method of the automatic gain adjustment. When the weights are calibrated, the ADC measures V_{ref} and gnd voltages, and the value of (primitive_{Vref}–primitive_{gnd}) is calculated. The primitive_{data} is the result that is obtained in the conversion process.

$$\text{out}_{data} = \frac{\text{primitive}_{data} \cdot 2^{16}}{\text{primitive}_{vref} - \text{primitive}_{gnd}}. \quad (6)$$

In this SAR ADC, a total of 28 data (24 bits) are generated during the calibration process, including weight data of each bit and automatic gain adjustment data. Figs. 16 and 17 show the INL, DNL, and the noise floor level of this SAR ADC with/without being calibrated. The simulation results reveal that auto-balance, self-measurement weight calibration and automatic gain adjustment strategies well correct INL and DNL errors, and improve the noise floor performance. During the calibration process, the operating temperature is the key factor that affects the accuracy of the calibration. Fig. 18 shows the relationship between the average absolute value of the weight errors and the temperature.

5. Layout and result

The final performance of the SAR ADC can be directly affected by the layout. The layout of the SAR ADC needs to be carefully designed, such as the interference of the comparator, self-timer, digital logic and CDAC. The self-timer and the clock trees of digital logic generate significant jitters on the power supply. The random jitters are coupled into the output of the CDAC through the bulk, parasitic capacitors, and comparator circuits. When the outputs of the CDAC are contaminated, the performances of the SAR ADC are degraded severely. So, the interference barrier structures are necessary for the layout. On the other hand, the transmission distances of key signals need to be shorter. Therefore, the layout needs to tradeoff between the interference and the signal transmission distance. The final layout is shown in Fig. 19. The switch array of the CDAC in the layout is used as a barrier to shield against the interference of digital logic and self-timer. The comparator is placed near the output of the CDAC. The layout skills are employed to improve the design performances and the simulation results prove that the design performance is guaranteed by a reasonable layout. The post-layout simulation result is shown in Fig. 20. At the end of the conversion, the residual voltage is less than 20 μV.

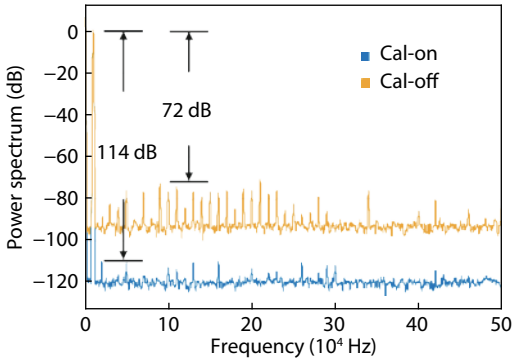

Fig. 17. (Color online) Simulated results of noise floor with/without calibration.

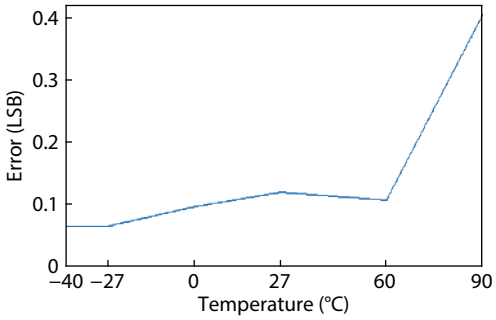

Fig. 18. Simulated results of the average absolute value of weight errors versus temperature.

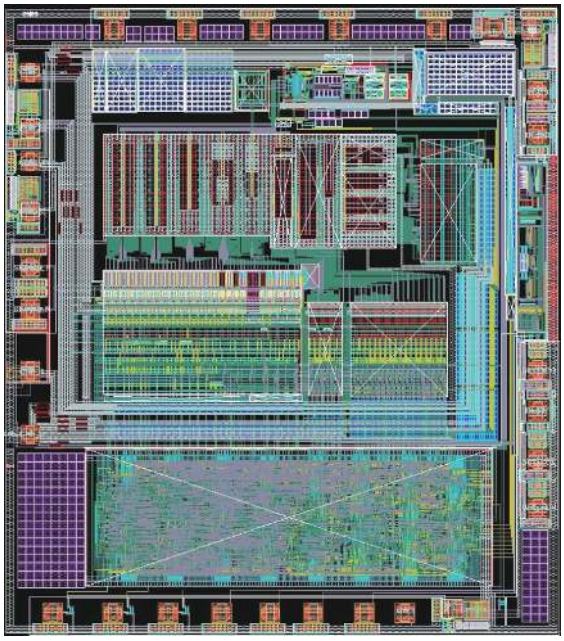

Fig. 19. (Color online) The layout of the 16bit 1MSPS SAR ADC with on-chip calibration.

The final simulation results are given in Table 2. Table 2 shows the comparison between the recent excellent medium-speed high-precision SAR ADCs and this design. This work has a great market in cheap applications of medium-speed high-precision SAR ADCs.

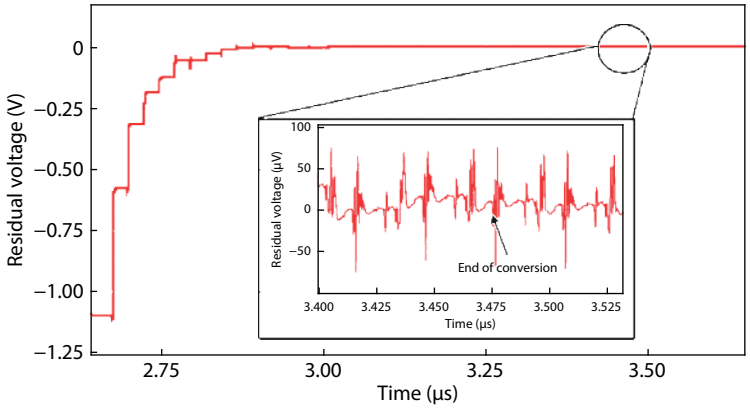

Fig. 20. (Color online) The post-layout simulated result of the residual voltage.

Table 2. The comparison with high-resolution and medium-speed SAR ADCs.

Parameter	Shen[8]	Maddox[24]	Mc Neill[10]	This work
Type	SAR	SAR	SAR	SAR
Resolution (bit)	16-bit	16-bit	16-bit	16-bit
Speed (MS/s)	16	1	1	1
INL (LSB)	−1.9/+2.3	−0.8/0.8	−0.5/+0.5	−0.5/0.5
DNL (LSB)	−0.8/+0.8	−0.3/0.3	−0.5/+0.5	−0.8/0.8
SFDR (dB)/ SNDR (dB)	98/78	100/81	NA	110/101
Power (mW)	16	6.95	NA	11
FOM (dB)	138	129	NA	127
Area (mm^2)	0.55	4.1	1.92	6.48
Calibration	On-chip	Off-chip	On-chip	On-chip
Process (nm)	55	55	180	250

6. Conclusion

A 16-bit 1MSPS SAR ADC with digital foreground calibration is developed in this paper. In this design, the self-measurement weight calibration, auto-balance, and automatic gain strategies are employed to guarantee that the SAR ADC achieves a 16-bit resolution. RS strategy and RS-based dither strategy are presented for optimizing the conversion stability effectively. A high-performance self-timer auto-zero comparator is applied to lower the power cost and optimize the decision time. The ADC is implemented with 0.25 μm CMOS process and the simulation results show the ADC meets 16-bit 1MSPS requirements.

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