Journal of Semiconductors
(2020) 41, 122102
doi: 10.1088/1674-4926/41/12/122102

ARTICLES

The influence of total ionizing dose on the hot carrier injection of 22 nm bulk nFinFET

Baoshun Wang[1, 2], Jiangwei Cui[1, 2, †], Qi Guo[1, 2], Qiwen Zheng[1, 2], Ying Wei[1, 2], and Shanxue Xi[1, 2]

[1]Key Laboratory of Functional Materials and Devices under Special Environment, Chinese Academy of Sciences, Xinjiang Key Laboratory of Electric Information Materials and Devices, Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences, Urumqi 830011, China

[2]University of Chinese Academy of Sciences, Beijing 100049, China

Abstract: We investigate the hot carrier injection effect (HCI) and how X-ray radiation impacts the HCI of 22-nm nFinFETs as a function of device geometry and irradiation bias conditions in this paper. In the HCI test, the degradation of threshold voltage and saturation current decreases with the increase of fin number, which means that HCI weakens when the fin number increases. The reason is attributed to the coupling effect between fins. Moreover, irradiation is shown to weaken the degradation during the subsequent hot carrier test. The influence of irradiation on HCI is more obvious with ON bias than that of OFF bias and transmission gate bias. It is supposed that the Si–H bonds can be broken by irradiation before the HCI test, which is one reason for the irradiation influence on HCI. Besides, trapped charges are generated in the shallow trench isolation by the radiation, which could reduce the channel electric field, and then weaken the HCI.

Key words: FinFET; TID; HCI

Citation: B S Wang, J W Cui, Q Guo, Q W Zheng, Y Wei, and S X Xi, The influence of total ionizing dose on the hot carrier injection of 22 nm bulk nFinFET[J]. *J. Semicond.*, 2020, 41(12), 122102. http://doi.org/10.1088/1674-4926/41/12/122102

1. Introduction

Nowadays, the complementary metal-oxide semiconductor (CMOS) chips' feature size has commercially developed to 5 nm. FinFETs are promising to extend CMOS scaling owing to reduced short-channel effects[1]. Compared with planar devices, FinFET has the following advantages, such as near-ideal subthreshold slope, excellent gate control over the body potential, low leakage current and higher mobility[2]. On behalf of the high-performance device, FinFET also attracts the attention of applications in radiation environment, such as in space.

However, there are some serious reliability problems for aerospace devices, such as HCI and radiation damages. Channel hot carriers are generated by impact ionization under the action of a strong electric field near the drain. When these carriers are launched to the gate, oxide layer trap charges and interface states will be generated, which will affect the performance parameters of the devices, such as threshold voltage, subthreshold swing, saturation current and trans-conductance, etc[3]. The FinFET with a small feature size has a strong internal electric field, thus the HCI can be significant. Some studies show that HCI is dependent on fin width[4]. Ma pointed out that parameter degradation caused by 14 nm FinFET HCI is mainly attributed to interface states, and the distribution of interface states on the top of FinFET fins is significantly less than that on the lateral wall of fins[5]. After studying the HCI of 90 nm SOI FinFET with different channel lengths, Jiang pointed out that the degradation mechanism of long-channel devices and short-channel devices is different[6]. Yeh pointed out that 20 nm bulk FinFET with fewer fins show better device characteristics, but the degradation of device parameters caused by hot carriers is more serious[7]. Moreover, different evolutions of the threshold voltage and the saturation current of the UTBB nMOSFETs may be due to the slow border traps[8].

For devices used in a radiation environment, not only the conventional reliability problems should be considered, but also the influence of radiation effects on the conventional reliability of devices should be paid attention to. Silvestri pointed out that, for 130 nm NMOSFETs, the parameter degradation of the un-irradiated nMOSFETs is smaller than that of the irradiated sample after applying hot carrier stress[9]. The larger the bias, the smaller the degradation of device parameters. Zheng pointed out that hot carrier degradation of irradiated 65 nm nMOSFETs is greater than those without irradiation due to radiation-induced charge trapping in the STI[10]. The influence of TID (total ionizing dose effect) on HCI of short channel UTBB FD-SOI nMOSFETs is significant, which is due to irradiation generated defects in buried oxide (BOX)[11]. For nMOSFET, the synergistic effect of total dose irradiation and hot carriers exceeds the simple superposition of the two effects. It considers that the combination of holes in the oxide trap induced by the total dose irradiation and hot electrons reduces the positive charge in the oxide trap. The irradiation-induced interface state captures the hot electrons to form negative interface trap charges[12]. But, to the best of our knowledge, no studies have shown how total ionizing dose radiation affects HCI in 22 nm FinFETs.

The HCI of nFinFET with different fin numbers and the influence of total ionizing dose irradiation with different bias conditions on the HCI of nFinFET are studied in the paper. We demonstrate that the smaller the fin number, the more ob-

Correspondence to: J W Cui, cuijw@ms.xjb.ac.cn
Received 7 MARCH 2020; Revised 17 JUNE 2020.
©2020 Chinese Institute of Electronics

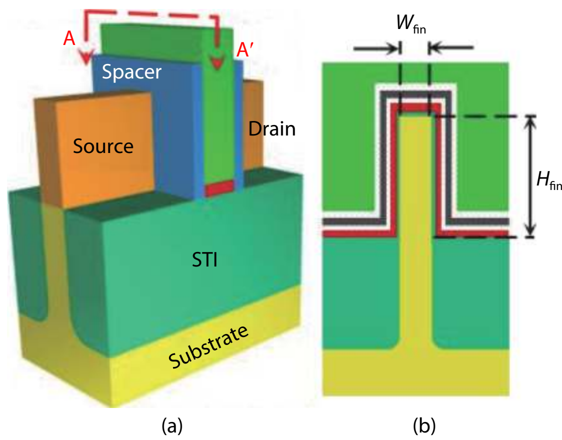

Fig. 1. (Color online) The structure diagram of nFinFET. (a) A 3D model of bulk FinFET. (b) A cross-section view along A–A' direction[13].

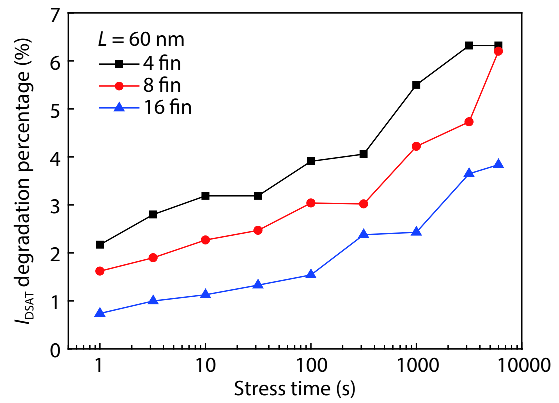

Fig. 3. (Color online) Degradation of saturation current (I_{DSAT}) for nFinFETs with different numbers of fins under HCI stress for samples with a 60 nm gate length.

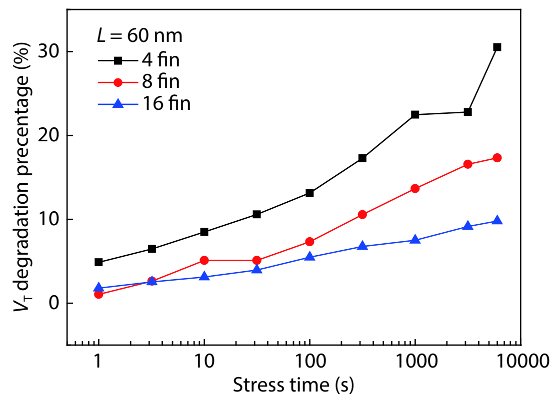

Fig. 2. (Color online) Degradation of V_T for nFinFETs with different numbers of fins under HCI stress for samples with a 60 nm gate length.

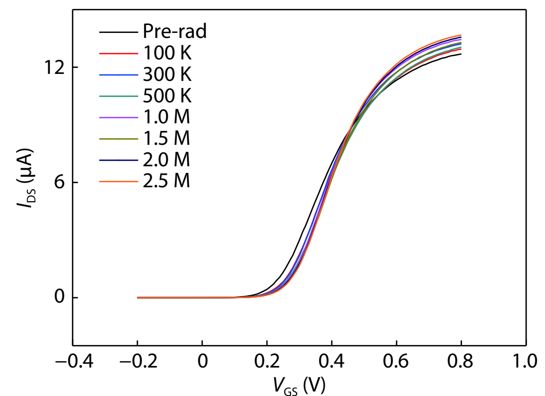

Fig. 4. (Color online) I_{DS}– V_{GS} curves as a function of the irradiation dose for nFinFET with 8 fins and a 60 nm gate length biased at the ON state.

vious the HCI of nFinFETs. What is more, compared with un-irradiated nFinFET, the HCI of irradiated nFinFET is weakened, which is different from the experimental phenomena of planar devices.

2. Experiment and devices

The devices used in this test are bulk nFinFETs produced by the process of 22 nm. The gate length of devices is 60 nm. Fig. 1 shows the structure diagram of the device. The channel of the device is a parallel fin-like structure with various fin numbers, 2, 4, 8 and 16, the effective width of single fin $2H_{fin} + W_{fin}$ = 80 nm, and the effective fin width of the device $W_{eff} = N(2H_{fin} + W_{fin})$, where N is the fin number and working voltage V_{DD} = 0.8 V. HfO_2 and SiO_2 are employed as the gate oxide. The devices are divided into two groups, while samples in group A are un-irradiated before hot-carrier stress and samples in group B are radiated before hot-carrier stress with different bias conditions during irradiation. There are some samples failed during the experiment because of ESD damage. The samples in group A were tested on a Keithley 4200 semiconductor parameter analyzer to conduct the hot carrier stress test. The stress condition used in this test was $V_{GS} = V_{DS}$ = 1.2 V with the body and the source grounded. The total stress time was 6000 s. The I_{DS}–V_{GS} characteristics were obtained at the stress time of 1, 3.2, 10, 31.6, 100, 316.2, 1000, 3162.3, and 6000 s, respectively. When testing the I_{DS}–V_{GS} curve of the device, the drain voltage was set to 0.1 V, the body and source were grounded, and the gate voltage was increased from 0 to 0.8 V.

In addition, samples in group B were taken for the pre-irradiation test. The dose rate used for irradiation was 425.26 rad(Si)/s, and the total ionizing dose for 60 nm gate length samples was 2.5 Mrad(Si). There were three bias conditions: ON, OFF and TG, during irradiation for all the samples in group B. The ON bias condition was carried out with the gate applied with 0.8 V and other electrodes 0 V. The OFF bias condition was carried out with the drain applied with 0.8 V and other electrodes 0 V. The TG bias condition was carried out with the source and drain applied with 0.8 V and other electrodes 0 V. The floating annealing was carried on at room temperature for one week after irradiation. After annealing, the hot carrier stress test was carried out. The test conditions and process are the same as above.

3. Experimental results

Fig. 2 shows the degradation of V_T for un-irradiated nFinFETs in group A with different fin numbers and gate length of 60nm under HCI stress. It is shown that as the stress time increases, the V_T degradation percentage of 4 fin devices is significantly higher than the latter two with 8 fin and 16 fin.

Fig. 3 shows the degradation of I_{DSAT} for nFinFETs with different numbers of fins under HCI stress. We can see that there is also more degradation on devices with fewer fins. Fig. 4 shows I_{DS}–V_{GS} curves as a function of the irradiation dose for nFinFET with 8 fins and 60 nm gate length biased at

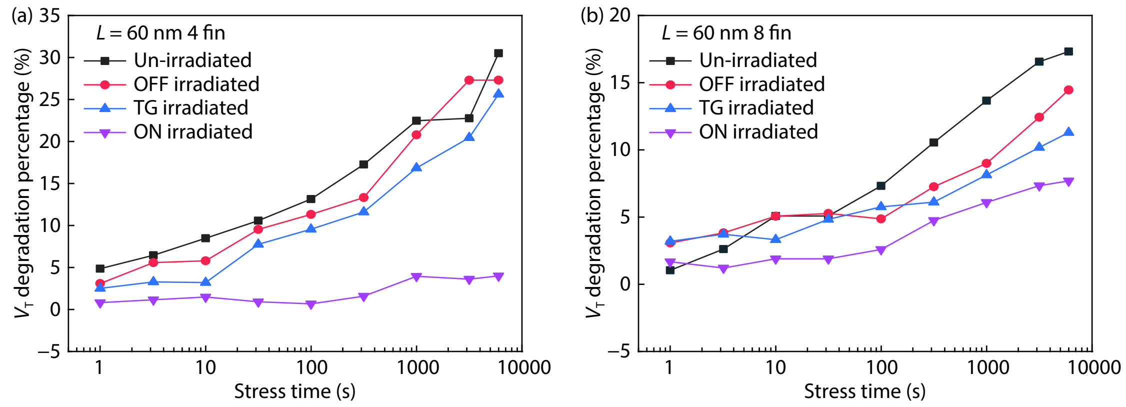

Fig. 5. (Color online) Degradation of V_T as a function of stress time for un-irradiated nFinFETs and for irradiated nFinFETs in different bias conditions during irradiation. (a) For 4 fin samples with a 60 nm gate length. (b) For 8 fin samples with a 60 nm gate length.

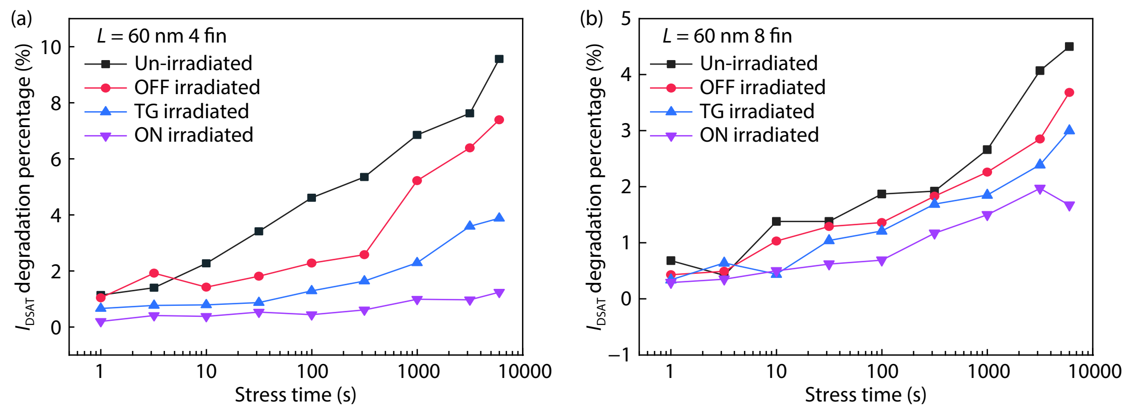

Fig. 6. (Color online) Degradation of I_{DSAT} as a function of stress time for un-irradiated nFinFETs and for irradiated nFinFETs in different bias condition during irradiation. (a) For 4 fin samples with a 60 nm gate length. (b) For 8 fin samples with a 60 nm gate length.

Table 1. V_T degradation percentage of un-irradiated devices, OFF-bias irradiated devices, TG-bias irradiated devices, and ON-bias irradiated devices in different groups after 6000 s hot carrier stress.

Device	Un-irradiated	OFF irradiated	TG irradiated	ON irradiated
L_{gate} = 60 nm, 4 fin	30.15%	27.31%	25.63%	4.00%
L_{gate} = 60 nm, 8 fin	17.32%	14.46%	11.29%	7.69%

Table 2. I_{DSAT} degradation percentage of un-irradiated devices, OFF-bias irradiated devices, TG-bias irradiated devices, and ON-bias irradiated devices in different groups after 6000 s hot carrier stress.

Device	Un-irradiated	OFF irradiated	TG irradiated	ON irradiated
L_{gate} = 60 nm, 4 fin	9.56%	7.39%	3.88%	1.24%
L_{gate} = 60 nm, 8 fin	4.5%	3.68%	3%	1.67%

ON state. As the dose increases, the I_{DS}–V_{GS} curve shifts positively, and V_T and I_{DSAT} increase.

Fig. 5 shows the degradation of V_T as a function of stress time for un-irradiated nFinFETs and irradiated nFinFETs in different bias conditions during irradiation. Table 1 shows the threshold voltage degradation percentage of un-irradiated and irradiated samples. The figure and the table indicate that the V_T degradation of all devices under the hot carrier test decreases a lot, and the HCI of the irradiated devices weakens.

Fig. 6 shows the degradation of I_{DSAT} as a function of stress time for un-irradiated nFinFETs and irradiated nFinFETs in different bias conditions during irradiation. Table 2 shows the I_{DSAT} degradation percentage of un-irradiated and irradiated samples. The figure and the table indicate that the channel I_{DSAT} degradation of the four devices in the hot carrier test decreases successively, and the HCI of the irradiated devices weakens.

4. Discussion and analysis

In a FinFET, all fins share one gate. As the gate voltage is positive, negative inversion charges are generated in the fins. Because the same charges repel each other, inversion charge density decreases in the adjacent fins. When the number of fins increases, the coupling effect between fins is more signific-

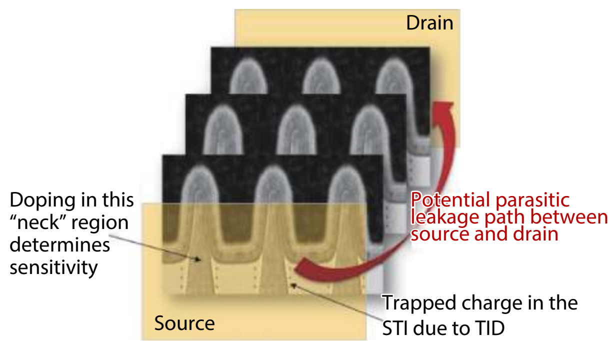

Fig. 7. (Color online) A schematic diagram showing that total dose irradiation causes trap holes in STI[15].

ant[7], the charge density of the inversion layer in the fins decreases, and the channel hot carrier density decreases. And under the effect of the electric field, the impact ionization induced by the hot carrier near the drain is weakened, and the oxide trapped charge and interface state are reduced. Thus, for samples with more fin numbers, HCI weakens, as shown in Figs. 2 and 3.

The Si–H bond exists at the interface between the gate oxide layer and silicon of FinFET[14], and the Si–H bond can be broken by total dose irradiation and hot carriers, generating oxide trap charge and interface state, and degrading the device performance. Pre-irradiation makes part of Si–H bond rupture and device parameters degrade. The HCI experiment carried out after irradiation will make the rest of the Si–H bond rupture. The fracture of the Si–H bond caused by HCI is reduced compared with that without irradiation, resulting in the reduction of the degradation of device parameters caused by HCI.

For another reason, under the action of hot carrier stress, the hot electrons generated by the impact ionization at the drain end will be injected into the gate oxide layer and form oxide trap charges, which is why the V_T drifts positively as the stress time increases[7]. Total dose irradiation causes trap holes in the shallow trench isolation (STI) region of the FinFET, and the bottom region of the fin generates an additional electric field introduced by irradiation[13]. Fig. 7 shows the schematic diagram of total dose irradiation causes trap holes. The direction of the electric field is opposite to the original electric field at the bottom of the fin. Therefore, the electric field in the bottom region of the fin is weakened, and the channel electric field strength is weakened. During the application of hot carrier stress, the hot carrier generation is reduced and the HCI is weakened due to the weakening of the channel electric field. The total ionizing dose effect of bulk FinFET is affected by the irradiation bias conditions. For the three irradiation bias conditions, the ON state bias is the worst bias condition, followed by the TG state, and the total dose irradiation under the OFF state bias has the least impact on the device[16]. During the total dose irradiation, trapped charges will be generated in the STI region of the bulk FinFET. Therefore, the bulk FinFET HCI is weakened by total dose irradiation. While at ON bias, there are most traps, and the channel electric field strength decreases most.

5. Conclusion

For bulk nFinFET produced by the 22 nm process, as the fin number increases, the charge density of the inversion layer inside the fin decreases due to the charge coupling between fins. In the hot carrier test, the more the fin number, the more the impact ionization weakened, the V_T and channel I_{DSAT} degradation are reduced, and thus the HCI is weakened. In the total dose irradiated device, the radiation has broken some Si-H bonds. In the subsequent HCI test, compared with the un-irradiated devices, the number of Si–H bonds affected by hot carriers decreases, and the degradation of device performance decreases. Moreover, the trapped charges generated by the radiation in the STI reduce the channel electric field. Therefore, HCI is weakened by total dose irradiation in nFinFET. Further investigation needs to be carried out for deeply mechanism analysis.

Acknowledgements

This work was supported by Youth Innovation Promotion Association CAS (2018473), the National Natural Science Foundation of China under Grant NO. 12075313, and the West Light Foundation of The Chinese Academy of Sciences (Grant No.2019-XBQNXZ-A-003).

References

[1] Zhang E X, Fleetwood D M, Hachtel J A, et al. Total ionizing dose effects on strained Ge pMOS FinFETs on bulk Si. IEEE Trans Nucl Sci, 2017, 64, 226

[2] Chatterjee I, Zhang E X, Bhuva B L, et al. Bias dependence of total-dose effects in bulk FinFETs. IEEE Trans Nucl Sci, 2013, 60, 4476

[3] Chung E A, Nam K J, Nakanishi T, et al. Investigation of hot carrier degradation in bulk FinFET. 2017 IEEE International Reliability Physics Symposium, 2017

[4] Chang W T, Cin L G, Yeh W K. Impact of fin width and back bias under hot carrier injection on double-gate FinFETs. IEEE Trans Device Mater Reliab, 2015, 15, 86

[5] Ma C Y, Li B, Wei Y Q, et al. FinFET reliability study by forward gated-diode method. 2008 9th International Conference on Solid-State and Integrated-Circuit Technology, 2008, 644

[6] Jiang H, Yin L X, Li Y, et al. Comprehensive understanding of hot carrier degradation in multiple-fin SOI FinFETs. 2015 IEEE International Reliability Physics Symposium, 2015

[7] Yeh W K, Chen P Y, Shih C H, et al. The impact of fin number on device's performance and reliability in tri-gate FinFETs. 2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM), 2017

[8] Tang X Y, Lu J W, Zhang R, et al. Positive bias temperature instability and hot carrier injection of back gate ultra-thin-body $In_{0.53}Ga_{0.47}As$-on-insulator n-channel metal–oxide–semiconductor field-effect transistor. Chin Phys Lett, 2015, 32, 117302

[9] Silvestri M, Gerardin S, Paccagnella A, et al. Channel hot carrier stress on irradiated 130-nm NMOSFETs: Impact of bias conditions during X-ray exposure. 2007 9th European Conference on Radiation and Its Effects on Components and Systems, 2007, 1

[10] Zheng Q W, Cui J W, Zhou H, et al. Hot-carrier effects on total dose irradiated 65 nm n-type metal–oxide–semiconductor field-effect transistors. Chin Phys Lett, 2016, 33, 076102

[11] Cui J W, Zheng Q W, Ning B X, et al. Hot-carrier effect on TID irradiated short-channel UTTB FD-SOI n-MOSFETs. IEEE Radiation Effects Data Workshop, 2018

[12] Das N C, Nathan V, Dacus S, et al. Combined effects of hot-carrier stressing and ionizing radiation in SiO_2, NO, and ONO MOSFETs. IEEE Electron Device Lett, 1993, 14, 40

[13] Yang L, Zhang Q Z, Huang Y B, et al. Total ionizing dose response and annealing behavior of bulk nFinFETs with ON-state bias irradi-

aiton. IEEE Trans Nucl Sci, 2018, 65, 1503

[14] Chen Z, Ong P. Direct evidence for multiple vibrational excitation of Si-H/D bonds for hot-carrier degradation of MOS transistors. 60th DRC Conference Digest Device Research Conference, 2002

[15] Zhang H, Jiang H, Fan X, et al. Effects of total-ionizing-dose irradiation on single-event response for flip-flop designs at 14-/16-nm bulk FinFET technology node. IEEE Trans Nucl Sci, 2018, 65, 1928

[16] King M P, Wu X, Eller M, et al. Analysis of TID process, geometry, and bias condition dependence in 14-nm FinFETs and implications for RF and SRAM performance. IEEE Trans Nucl Sci, 2017, 64, 285