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A 12-bit 30-MS/s VCO-based SAR ADC with NOC-assisted multiple adaptive bypass windows

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Abstract: This paper proposes a technique that uses the number of oscillation cycles (NOC) of a VCO-based comparator to set multiple adaptive bypass windows in a 12-bit successive approximation register (SAR) analog-to-digital converter (ADC). The analysis of the number of bit cycles, power and static performance shows that three adaptive bypass windows reduce power consumption, and decrease DNL and have similar INL, compared with the SAR ADC without bypass windows. In addition, a 1-bit split-and-recombination redundancy technique and a general bypass logic digital error correction method are proposed to address the settling issues and optimize the size of the bypass window. This design is implemented in 40 nm CMOS technology. The conversion frequency of the ADC reaches up to 30 MS/s. The ADC achieves an SFDR of 85.35 dB and 11.12-bit ENOB with Nyquist input, consuming 380 μW, down from 427 μW without multiple adaptive bypass windows, at a 1.1 V supply, resulting in a figure of merit (FoM) of 5.69 fJ/conversion-step.

Key words: adaptive bypass window; number of oscillation cycles (NOC); offset; split-and-recombination redundancy; SAR ADC; VCO-based comparator

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1. Introduction

Low power and high resolution analog-to-digital converters (ADCs) are widely used in mobile, wearable and implantable devices, the internet of things (IoT) and so on. Successive approximation register (SAR) ADC exhibits excellent energy efficiency and has attracted much attention due to its digital-like nature and adaptability to advanced CMOS technology. Much work is occuring to reduce the logic power consumption, such as a variety of switching schemes to save part of the energy of CDAC[1–6]. From a systematic perspective, the bypass logic shown in Fig. 1, can not only save energy from CDAC but also greatly reduce the energy from the comparator and digital logic[7]. When the input voltage is within the range called the bypass window, the intermediate bit cycles can be skipped completely and does not influence the correct output. However, the bypass window comes at the cost of two additional coarse comparators and an external reference, which increases design complexity and makes the precision partially dependent on the reference voltage.

The comparator is a fundamental consideration in SAR ADC, which is an indispensable but power-hungry block. The input-referred noise constrains the power consumed by the comparator. For a voltage-domain comparator such as a double-tail comparator or strong-arm comparator, whose noise reduction relies on brute-force analog scaling, it requires four times the power to halve the input-referred noise[8]. Alternatively, time-domain comparators, which show good potential in power efficiency and scalability, attract attention due to their digital nature and more choices for lower noise such as VTC-based[9], VCDL-based[10], oscillator collapse-based[11] and VCO-based[12, 13]. The last type gains much favor under its noise-adaptive characteristic. It can generate output signal without oscillation if the input voltage is large. When the input voltage is small enough, it will oscillate until the decision is made. In other words, there is a relationship between the input voltage and the oscillation number, which shows that the oscillation number indicates an inherent coarse quantization.

Apart from making decisions and employing the decisions to reduce the comparator noise[14–16], a VCO-based comparator offers extra information, known as the number of oscillation cycles (NOC)[17], to detect whether the input signal of the comparator is in the vicinity of common-mode voltage. This information can be utilized to trigger bypass logic, which avoids the use of additional comparators and reference. It can be triggered at any bit as long as NOC reaches a specific number. Furthermore, multiple bypass windows can be constructed by NOC, which provide more power reduction and static performance improvement. The windows size can be adaptively adjusted to PVT variations on the basis of the NOC and window detection logic.

This design takes full advantage of the potential of a VCO-based comparator as a bypass detector served, which can be used for higher resolution (12 bit) and higher speed (30 MS/s) SAR ADC[18]. The structure of the VCO-based comparator and the consideration of the offset caused by different NOC are presented. The design of core digital circuits is described thoroughly. The benefits of bit cycles decrease, power reduction and static linearity improvement from adaptive multiple bypass windows are analyzed. For compensating the settling error from DAC and reference because of high resolution and speed, a 1-bit split-and-recombination re-

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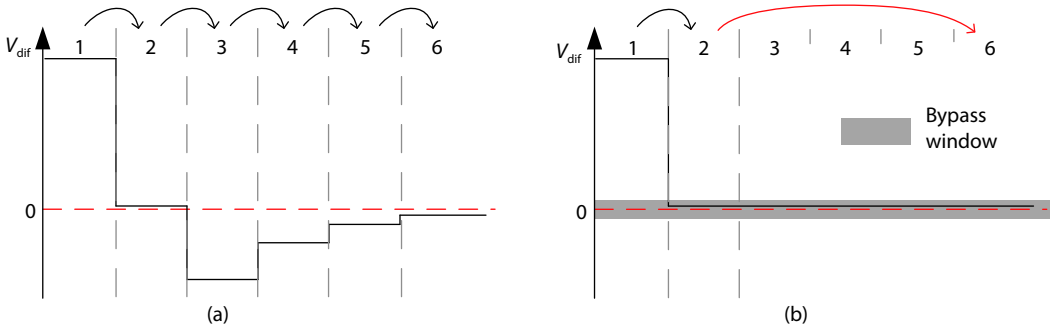

Fig. 1. Conversion process of 6-bit SAR ADC. (a) Conventional SAR ADC. (b) SAR ADC with bypass window.

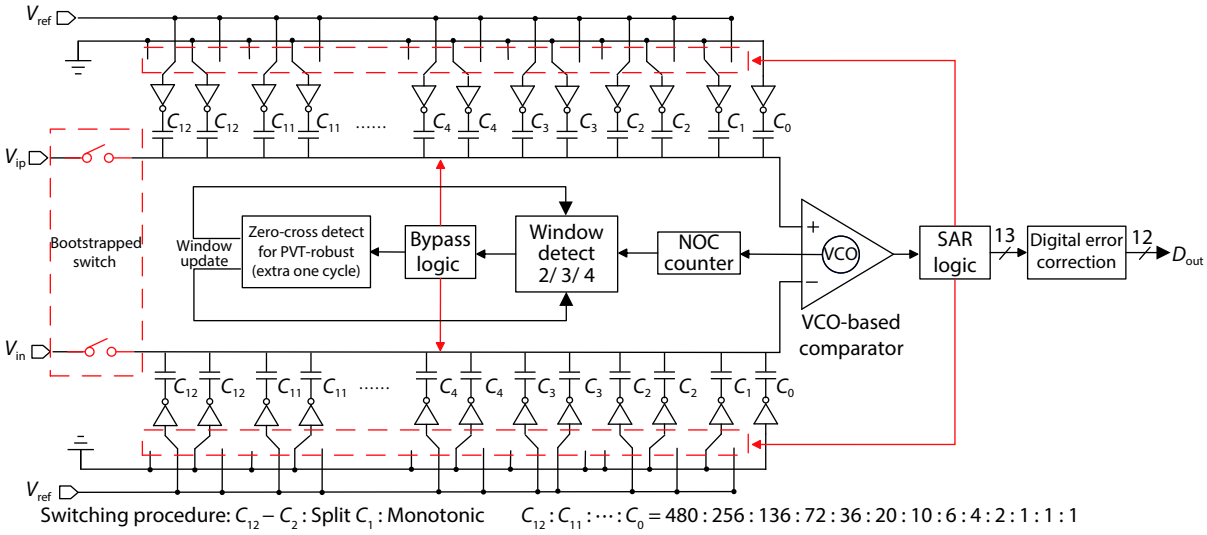

Fig. 2. Architecture of the proposed SAR ADC.

dundancy[19] and a general method to correct digital errors for bypass logic are proposed, which circumvents the use of complex or off-chip calibration circuits.

This paper is organized as follows. Section 2 describes the overall ADC architecture, operation principle and building blocks. Section 3 analyzes the bit cycle decrease, power reduction and static performances with multiple adaptive bypass windows, and derives the maximum DNL and INL of it, while section 4 explains split-and-recombination based redundancy and a general digital error correction method for bypass logic. Section 5 presents simulation results and comparison with the state-of-the-arts, and section 6 draws the conclusions.

2. Architecture and design considerations

The architecture of the proposed SAR ADC is shown in Fig. 2 including two bootstrapped sampling switches[20], a differential capacitive DAC (with 1-bit redundancy), VCO-based comparator, NOC counter, SAR logic, bypass logic, window detection logic (three adaptive bypass windows), window update logic, and digital error correction logic.

2.1. Operation principle

During the sampling phase, the input differential voltage is sampled onto the top plates of CDAC by two bootstrapped switches. If the input signal is large enough, the comparator makes the decision directly without oscillation. Otherwise, if the input signal is relatively small (within several LSBs), VCO will oscillate several times to increase the delay until the time difference between two VCO loops exceeds the dead zone of the phase detector. To take advantage of the oscillation information, three bypass windows W_2, W_3 and W_4 are used for the standing of the oscillation numbers of 2, 3 and 4, respectively. For example, if the NOC is 4, the bypass window W_4 is triggered for the first time and bit cycles will move to the LSB cycle. Due to the impact of noise and PVT variation, even if the same voltage inputs into the comparator, the oscillation number might be different. The signal must be detected to determine whether it can be digitized with the remaining capacitor weights in case the result is not convergent.

Window update logic, shown in Fig. 3, can implement the window-size detection. V_x and V_y are the differential inputs. V_B stands for the current bypass window size of W_4, and its initial value is 1 LSB. If differential signals cannot cross zero (common-mode voltage), the bypass window is too small and this process of the bypass is wrong[17]. The cycle must be back to where the bypass begins and W_4 is updated. The next time when the NOC is 4, the conversion process will be bypassed to the cycle of LSB + 1 and V_B will become the voltage of 2 LSB. This update process also applies to W_2 and W_3. It is worth noting that the size of the bypass window is updated following the weights of CDAC and carried out in the background. So smaller low-weight capacitors achieves more precision bypass window sizes and the adaptive bypass windows are PVT-robust. Bypass logic cannot be triggered for more than one time in one conversion period under the con-

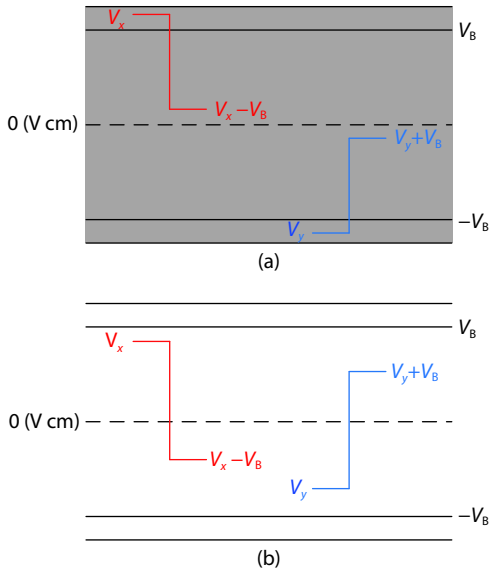

Fig. 3. Window update logic. (a) Not cross zero. (b) Cross zero.

sideration of conversion speed and complexity of the logic design.

2.2. VCO-based comparator design and offset consideration

Compared with voltage-domain comparator, whose input-referred noise is often dominated by sizes of input and tail transistors[21], designing a low-noise VCO-based comparator is more flexible[17]. The more stages it uses, the lower input referred noise but lower speed for the large input voltage it possesses. For delay cells, the topologies, the sizes of transistors, the threshold voltages of transistors and filtering capacitors all influence the noise and speed[22]. It is a hard trade-off that influences the bypass window sizes. Two common different delay cells are shown in Fig. 4. When input voltage is low, the pulling down of cell II will be slow. Compared with the delay cell II[12], the inserted inverter in delay cell I increases the reset speed. The option is that four stages of the delay cell I are to be used in the proposed scheme for quicker comparison.

Some works[23, 24] utilized multiple comparators to achieve lower power consumption or higher speed[25, 26]. All these designs have the matching problem of different input-referred offset voltages, which can be solved well by the calibration method[27] or introducing redundant capacitors into the DAC[28]. Actually, a VCO-based comparator operates like multiple comparators as it oscillates for a different number of cycles while it does not need extra calibration circuit or redundant cycle. The offset problem must be analyzed very carefully.

The delay time of the unit delay stage is given by

$$t_{\mathrm{d}} = \frac{C_{\mathrm{L}} V_{\mathrm{dd}}}{2 I_{\mathrm{DS}}}, \tag{1}$$

where C_{L} and I_{DS} are the load capacitance and average current of the current-starving stage, respectively. And the differential voltage-to-time gain of the VCO for one oscillation cycle is given by

$$G_{\mathrm{VCO\_1}} = \frac{2 C_{\mathrm{L}} V_{\mathrm{dif}} g_{\mathrm{m}}}{I_{\mathrm{DS}}^2}, \tag{2}$$

where g_{m} is the trans-conductance of the tail NMOS, and V_{dif} is the differential input voltage of the VCO comparator.

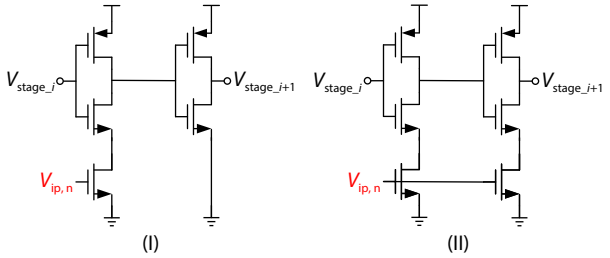

Fig. 4. Schematic of two common delay cells.

The dead zone of the PD (t_{dz}) represents the minimum detectable delay difference. The difference input voltage has the following relationship with the number of oscillations n[17],

$$\left|(n-1) G_{\mathrm{VCO\_1}} V_{\mathrm{dif}}\right| \leqslant t_{\mathrm{dz}} < \left|n G_{\mathrm{VCO\_1}} V_{\mathrm{dif}}\right|. \tag{3}$$

According to Eq. (2), Eq. (3) can be rewritten as

$$\frac{t_{\mathrm{dz}} I_{\mathrm{DS}}^2}{2 n g_{\mathrm{m}} C_{\mathrm{L}} V_{\mathrm{DD}}} < |V_{\mathrm{dif}}| \leqslant \frac{t_{\mathrm{dz}} I_{\mathrm{DS}}^2}{2(n-1) g_{\mathrm{m}} C_{\mathrm{L}} V_{\mathrm{DD}}}. \tag{4}$$

Eq. (4) means that the number of oscillaitons is the coarse quantization of the input signal, i.e., each NOC value corresponds to an input range.

Since the current of the unbiased circuit is much larger than that of the biased transistor, the offset voltage caused by the unbiased circuit can be ignored. For one oscillation cycle, the VCO in Fig. 5 can be considered as a four-stage VCDL. Hence, according to Ref. [10], the standard deviation of the offset time due to one oscillation cycle can be written as

$$\Delta t_{\mathrm{dVCO\_1}} = \frac{g_{\mathrm{m}} \Delta V_{\mathrm{os}} C_{\mathrm{L}} V_{\mathrm{dd}}}{I_{\mathrm{DS}}^2}, \tag{5}$$

where ΔV_{os} is the standard deviation of the input-referred offset voltage of one delay stage. And the standard deviation of the input-referred offset voltage induced by single oscillation becomes

$$\Delta V_{\mathrm{osVCO\_1}} = \frac{\Delta t_{\mathrm{dVCO\_1}}}{G_{\mathrm{VCO\_1}}} = \frac{\Delta V_{\mathrm{os}}}{2}. \tag{6}$$

No matter how many cycles are needed in the oscillation loop, signals oscillate in the same circuit paths. The offset delay time of a fabricated chip remains unchanged for each oscillation cycle. Hence, the standard deviation of the offset time caused by n oscillation cycles is $n \cdot \Delta V_{\mathrm{osVCO\_}n}$. So the input-referred offset voltage for n oscillation cycles is

$$\Delta V_{\mathrm{osVCO\_}n} = \frac{n \cdot \Delta t_{\mathrm{dVCO\_1}}}{G_{\mathrm{VCO\_}n}} = \frac{\Delta V_{\mathrm{os}}}{2}. \tag{7}$$

Eqs. (6) and (7) show that the input-referred offset voltage of the VCO-based comparator for one oscillation cycle is the same as that of n oscillation cycles.

The NAND-based phase detector (PD) is shown in Fig. 5. Compared with the DFF-based PD in Ref. [12], it needn't wait for a slower edge. Therefore, it increases the speed of the comparator. The size of the dead zone and bypass window can be tuned via load capacitors.

The dead zone of the PD can be derived as

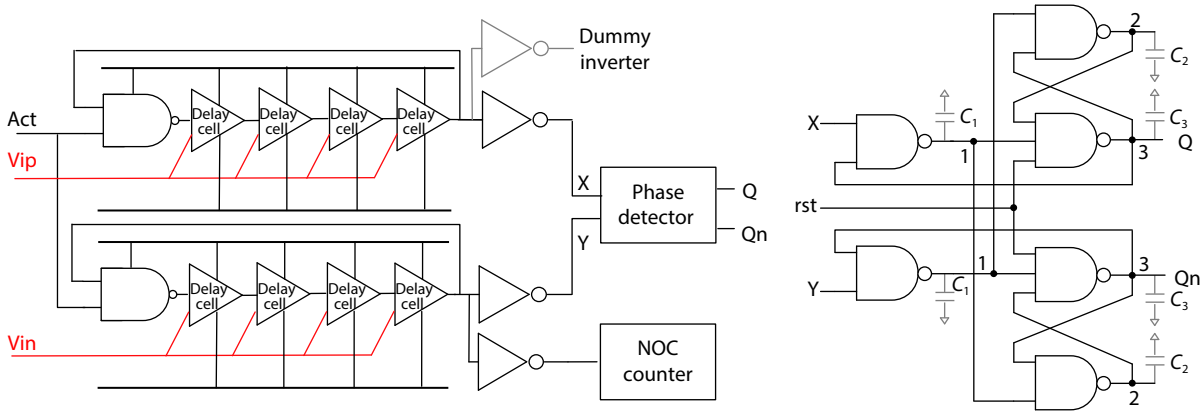

Fig. 5. Schematic of VCO-based comparator and phase detector.

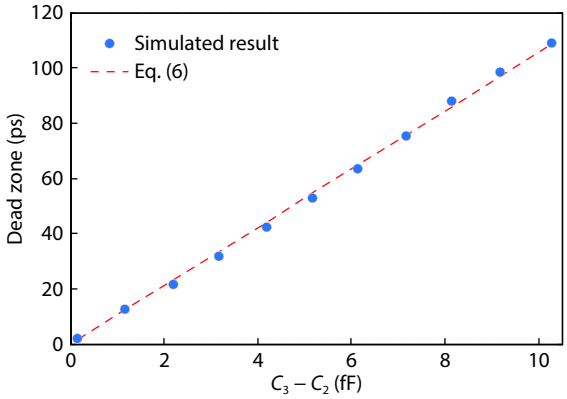

Fig. 6. Comparison of simulated result and Eq. (6) of the dead zone of PD.

$$t_{dz} = \frac{(C_3 - C_2)V_{dd}}{2I_{NAND}}, \tag{8}$$

where C_2 and C_3 are the load capacitors at the output terminals in PD, V_{dd} is the supply voltage and I_{NAND} is the average switching current of NAND. The simulated results of the dead zone of PD are shown in Fig. 6, which is accorded with Eq. (8).

2.3. Capacitive DAC

This work employs a split capacitor switching scheme[29] from MSB to LSB + 1. Compared with many other switching schemes, it not only keeps the input common-mode voltage of comparator stable, which avoids the deterioration of linearity of ADC, but also eliminates the need of extra common-mode voltage. For the LSB, the design uses the monotonic switching procedure[30]. It can halve the total capacitance with a fixed unit capacitor. Moreover, the change of common-mode voltage caused by it is negligible. To meet the requirements of KT/C noise and matching, this design chooses the unit capacitor as 1fF. The weight of the capacitor is shown in Fig. 1.

2.4. Bit-cycle control logic

In this design, the order of bit cycles is controlled by NOC. Bit cycles are not executed in the order of the conventional SAR ADC because of the bypass and window update logic. Registers should record the current cycle number, cycle number after bypass and the window size after window updating.

Fig. 7(a) shows the schematic and timing diagram of bit cycle control logic. It employs three window registers to record the sizes of three predefined bypass windows. Because of the relatively small size of the window, a 5-bit register can implement every window. **CLR** is the reset signal to reset window registers at power-up. The signal W_flag consists of W_2_flag, W_3_flag, and W_4_flag. The rising edges of them mean that differential input voltage V_{dif} triggers the corresponding window. The bypass cycle register is utilized to record the bit cycle after the process of the bypass. The decision of the comparator is indicated by the signal ready, and ready_d is the delay signal of ready. The normal cycle register is used to record the current bit cycle in the normal SA process. Enabling the bypass cycle register or normal cycle register is selected by the signal **SEL**. And Samp_n is the inverted sampling signal and en < 12 : 1 > is used to control the state of CDAC.

Fig. 7(b) shows the timing diagram of the bit cycle control logic for two conversion periods. Initial **CLR** is low to reset the window registers. When samp_n is low, both the bypass cycle register and the normal cycle register are reset. A low SEL means that normal cycle register is enabled. Cycle < 12 > is set high when the next ready_d rises meaning that the 12th bit is being converted. If the bypass logic is not triggered, the SA cycle will convert the 11th cycle. However, the rising edge of W_4_flag means that the bypass window W_4 is triggered. A high SEL enables the bypass cycle register and disables the normal cycle register. At the same time, the high SEL makes cycle < 6 : 1 > connect to byps < 6 : 1 >, and it is set to high. Cycle < 1 > becomes high on the next rising edge, meaning that the conversion from the 11th to the 2nd bit cycle is skipped and the conversion of the 1st bit starts. The rising edge of error indicates that V_{dif} is outside the bypass window *i.g.* and the window W_4 is too small. So the value of the window register increases by one. Then SEL is set to low to disable the bypass cycle register and enable the normal cycle register. At the same time, cycle < 12 : 1 > is reconnected to norm < 12 : 1 >. Therefore, the bit cycles previously bypassed is reconverted, and the 11th bit will be converted in the next cycle.

At the beginning of next sampling period, **SEL** is low and it is a conventional SA process. The rising edge of W_4_flag triggers the bypass logic. Since W_4 < 5 : 1 > has increased from '00000' to '00001'. Then the cycles from the 11th to the 3rd are bypassed. Missing the window size error detection during this cycle, cycle < 1 > is set to high on the next rising edge of

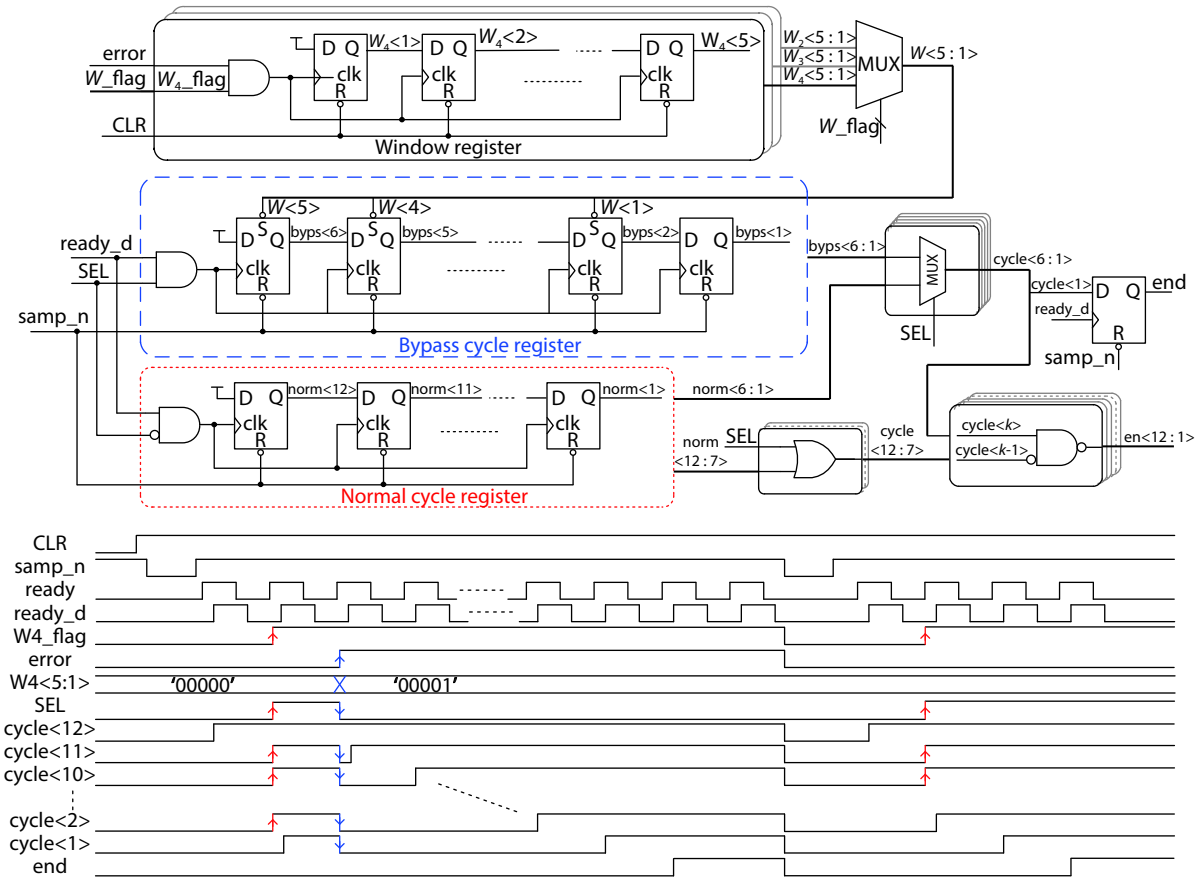

Fig. 7. Bit cycle control circuits. (a) Schematic. (b) Timing diagram.

ready_d.

2.5. CDAC driving circuits

In this design, the CDAC needs to be recovered after the detection of the wrong window size sometimes. The driving circuits of CDAC are shown in Fig. 8. Data_d and Datan_d are delay signals of the comparator output. $\overline{Dp}$ and $\overline{Dn}$ are inverted signals of Dp and Dn, respectively. When rst is low, Dn is set to high and Dp is set to low. If en is high, high data_d can set Dp to high and low $\overline{Dp}$ can lock all outputs until the next effective rst. Similarly, if en is high, high data_d can set Dn to high and low $\overline{Dn}$ can lock all outputs until the next effective rst.

In the upper block in Fig. 8(a), samp_n can be used as a reset signal to reset this block in the sampling phase. Cycle < 6 : 1 > can work as the reset signal in the lower block to recover the wrong switches due to the wrong bypass window size. For example, in Fig. 7, in the first sampling period, after the rising edge of W_4_flag, the output of the comparator is locked in Dp < 1 > and Dn < 1 >. At this moment, the window size is wrong. So the rising edge of error set cycle < 1 > to low, so Dp < 1 > and Dn < 1 > are reset directly. Therefore, these circuits do not need extra blocks to complete the recovery from the wrong switches in CDAC.

3. Multiple adaptive bypass windows

The NOC of the VCO-based comparator can be used to construct multiple bypass windows without additional references and comparators. The power reduction and static performances with multiple bypass windows are discussed in detail.

3.1. Power reduction with multiple adaptive bypass windows

Fig. 9 shows two conversion periods of a 6-bit SAR ADC without and with different bypass windows, respectively. In Fig. 9(a), 6 SA cycles are needed in every conversion period for conventional SAR ADC no matter how much the input signal is. For the SAR ADC with a wide bypass window, shown in Fig. 9(b), the differential signal is likely located in the range of the bypass window. But the bypass logic can only bypass a few SA cycles, and hence the power efficiency improvement is limited. For the SAR ADC with a narrow bypass window, shown in Fig. 9(c), V_{dif} has fewer opportunities to be detected within the bypass window. However, the bypass logic can bypass more numbers of SA cycles for the detected signal. The conversion process in Fig. 9(d) shows that the SAR ADC with multiple adaptive bypass windows will improve conversion efficiency extremely.

For general signals with uniform input, Fig. 10 shows the number of SA cycles per sample of a 12-bit SAR ADC with different bypass windows. The voltage range of a single wide or narrow bypass windows is ±16 LSB or ±2 LSB, respectively. For the wide bypass window, the bypass logic can reduce the number of SA cycles within a large input signal range, which achieves 11.06 SA cycles per sample on average. For the narrow bypass window, though the bypass logic can be employed to deal with the smaller input signal range, it can reduce more SA cycles for the signal meeting the size of the bypass window (indicated by the red line in Fig. 10), leading to 11.69 SA cycles per sample on average.

For the SAR ADC with multiple adaptive bypass windows,

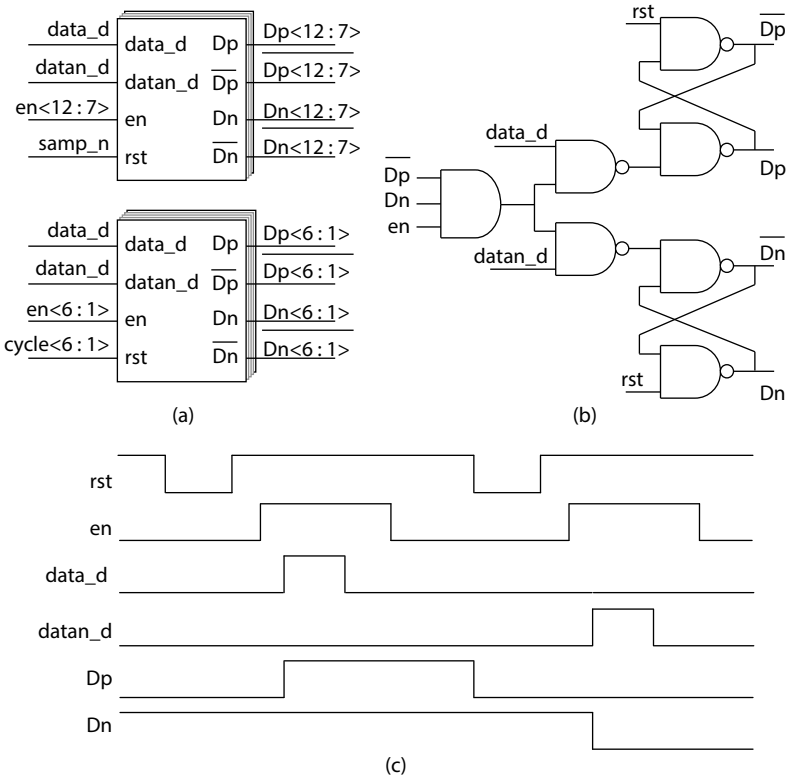

Fig. 8. CDAC driving circuits. (a) Blocks. (b) Schematic. (c) Timing diagram.

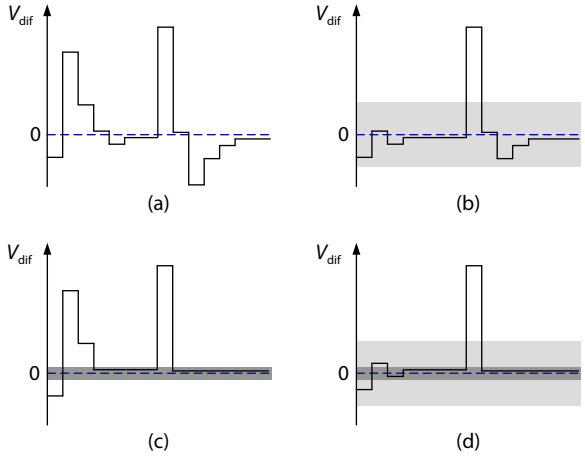

Fig. 9. Conversion processes of 6-b SAR ADCs. (a) Without bypass window. (b) Wide bypass window. (c) Narrow bypass window. (d) Multiple adaptive bypass windows.

this design uses three bypass windows. The simulation result shows that the SAR ADC with multiple adaptive bypass windows responds to large input signal range. Additionally, for small input voltage, the bypass logic can save more SA cycles. In other words, the SAR ADC with multiple adaptive bypass windows takes advantage of both the wide and narrow bypass windows. The size of the three bypass windows is initialized to 1 LSB, when the circuit starts to work. The window size has a correction process, and the three windows corresponding to NOC = 2, 3 and 4 will eventually stabilize on a certain size[17]. The convergence results are related to the design of the VCO comparator. In this design, the sizes of the three windows converge to ±16 LSB, ±4 LSB and ±2 LSB. And the SAR ADC with three bypass windows achieves 10.75 cycles per sample on average. The power consumption of the SAR

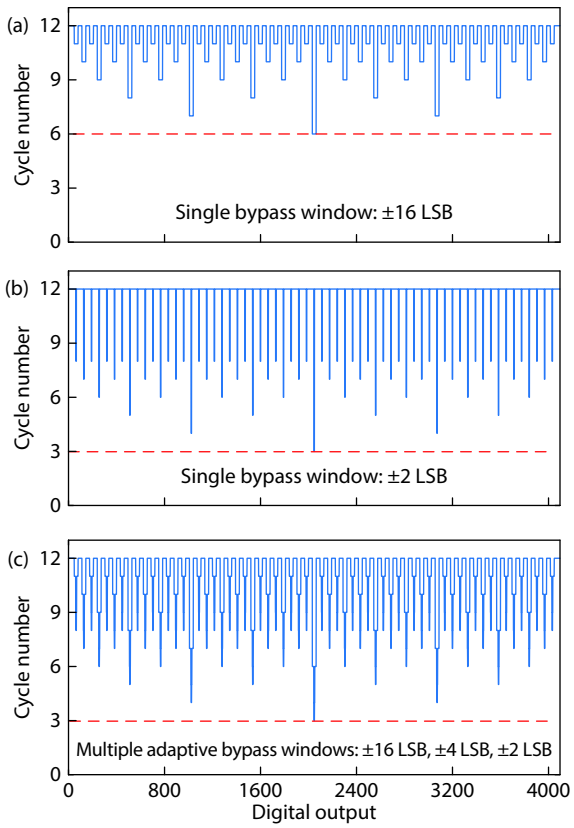

Fig. 10. (Color online) SA cycles per sample. (a) Wide bypass window. (b) Narrow bypass window. (c) Multiple adaptive bypass windows.

ADC mainly consists of the power of DAC, comparator and control logic. Reducing the SA cycle can reduce the power of the DAC, comparator and control logic at the same time. There is a case worth mentioning: where the clock cycles should be

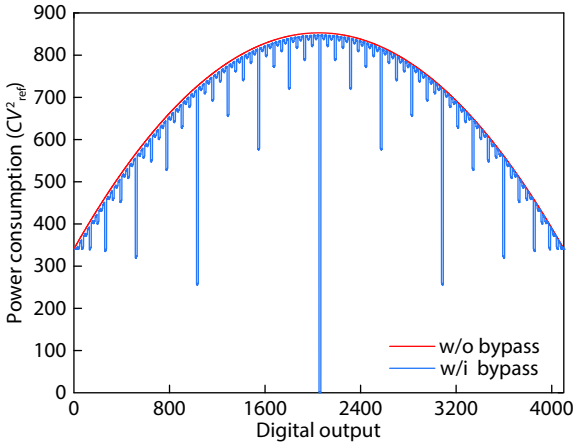

Fig. 11. Switching power consumption with/without bypass logic.

beyond 12 when the size of bypass window is wrong. However, because the change of window size is mainly caused by PVT change, the correct bypass window can be used in subsequent ADC conversion, without the need to detect the wrong bypass window every cycle and waste power. Consequently, the SAR ADC with multiple adaptive bypass windows can save more power than that with a single bypass window.

When three bypass windows sizes are assumed as ±16 LSB, ±4 LSB and ±2 LSB respectively, and the probability density function of the output code is assumed as a uniform distribution, Fig. 11 shows the power consumption by switching with and without bypass logic. The average switching energy with bypass logic is 602.92 CV^2_{ref}, which is 11.62% lower than the switching energy without bypass logic (682.17 CV^2_{ref}). If there is only one bypass window used, the switching energy is 605.89, 654.89 and 666.63 CV^2_{ref} for W_2, W_3, and W_4, respectively.

It is worth noting that the narrow window like W_4 failing to decrease too much bit cycles and switching power comes as no surprise. This is because the input signal is assumed as uniform here and the power efficiency of bypass logic is tied to the characteristics of signals. For many biomedical signals concentrating on the adjacent of common-mode voltage, this shows small variations in magnitude can save much power with bypass logic[7, 31]. In contrast with the single bypass window of prior works, the technique of multiple adaptive bypass windows is more versatile for different characteristics of input signals.

3.2. Static performance analysis of SAR ADC with multiple adaptive bypass windows

The state of capacitors in a split capacitor array is illustrated in Fig. 12. When the control code is changed from 'X' to '1', C_{up} is switched; when the control code is changed from 'X' to '0', C_{dn} is switched. Considering the mismatch of capacitors, different error voltages are introduced into the system by C_{up} and C_{dn} if the control codes are different.

The output voltage of the proposed SAR ADC is given by

$$V(S) = \frac{\sum_{i=1}^{N-1}(C_{up\_i}b_{up\_i} - C_{dn\_i}b_{dn\_i}) + C_0 b_{up\_0}}{C_{total}} V_{ref}, \tag{9}$$

$$\mathrm{DNL} = \left[C_{dn\_N-1} - \sum_{i=M+1}^{N-2} C_{up\_i} - (C_{up\_M} + C_{dn\_M}) + (C_{up\_M-1} + C_{cn\_M-1}) - \sum_{i=i}^{M-2}(C_{up\_i} + C_{dn\_i}) - C_0\right] \cdot \frac{V_{ref}}{C_{total}}. \tag{10}$$

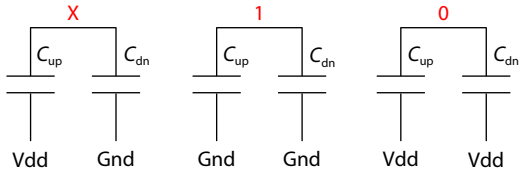

Fig. 12. The state of capacitors in split capacitor array.

If the control code of the DAC $S[i]$ = 1, b_{up_i} = 1 and b_{dn_i} = 0; if $S[i]$ = 0, b_{up_i} = 0 and b_{dn_i} = 1; if $S[i]$ = X, b_{up_i} = 0 and b_{dn_i} = 0. C_{up_i} and C_{dn_i} are the actual values (with mismatch errors) of the corresponding capacitors. C_0 is the unit capacitance. Since the mismatch errors of high-weighted capacitors influence the conversion results, much more greatly than that of the low-weighted capacitors, the maximum DNL occurs at the minimum code with the largest bypass window. Assuming the maximum bypass window W_2 = 5 (±16 LSB), the maximum DNL will occurs at S = '$XXXXXX$010000', which can be decoded into the standard binary code as D_{out} = '011111110000' by the state of capacitor array. The control code for D_{out} = '011111110000' –' 1' is S = '011111101111'. So the voltage difference can be written as

$$\mathrm{DNL} = V(XXXXXX010000) - V(011111101111). \tag{11}$$

Assuming σ_0 is the standard deviation of the random error of a unit capacitor, from Eqs. (9) and (11), the DNL can be written in LSB as $\sqrt{1040}\sigma_0/C_0$. If $W_2 = M$ and the resolution is N-bit, Eq. (10) can be derived. So the maximum DNL can be calculated in LSB as

$$\mathrm{DNL}_{max} \approx \frac{\sigma_0\sqrt{2^{N-2} + 2^{M-1}}}{C_0}. \tag{12}$$

Fig. 13 illustrates the DNL performance of a conventional SAR ADC with split capacitor array and the proposed ADC with multiple adaptive bypass windows. The DNL curves are the root-mean-square (RMS) value of 10 000 simulations and each unit capacitor cell has a Gaussian random error with a standard deviation of 1%. The simulation shows the ADC with multiple adaptive bypass windows achieves a better DNL performance than the conventional one.

The definition of INL at bin k is often defined as $\mathrm{INL}(k) = V(k) - V_{ideal}(k)$. However, in actual applications, $V(0)$ is used as the starting point of INL to eliminate the error caused by offset. So the formula of INL is

$$\mathrm{INL}(k) = V(k) - V(0) - V_{ideal}(k). \tag{13}$$

If the minimum bypass window W_4 = 2 (±2 LSB), the control code at D_{out} = '011111111111' is S = '$XXXXXXXXX$011'. The INL at D_{out} = '011111111111' is

$$\mathrm{INL} = V(XXXXXXXXX011) - V(000000000000) - V_{ideal}. \tag{14}$$

So the INL at D_{out} = '011111111111' can be calculated in LSB as $32\sigma_0/C_0$. Similarly, if the minimum bypass window $W_4 = K$, the INL at D_{out} = '011111111111' is

$$\mathrm{INL} = \left[\sum_{i=K+1}^{N-1} C_{dn\_i} + \sum_{i=1}^{K-1}(C_{up\_i} + C_{dn\_i}) + C_0\right] \frac{V_{ref}}{C_{total}} - V_{ideal}. \tag{15}$$

Since C_{up_i} and C_{dn_i} are different in split capacitor array be-

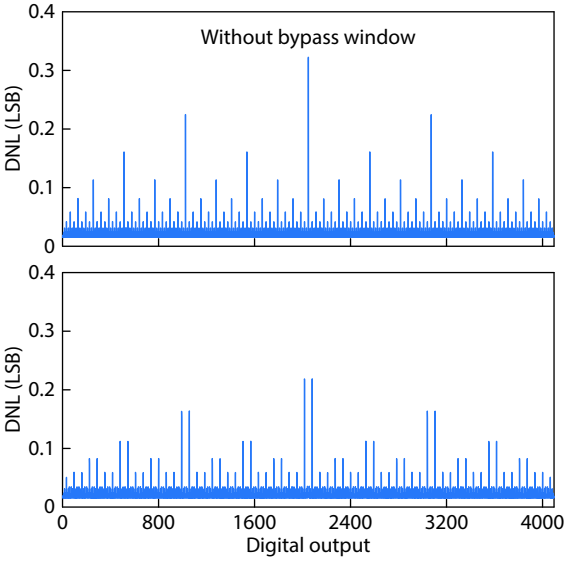

Fig. 13. (Color online) DNL performances of SAR ADC without bypass window and with multiple adaptive bypass windows.

cause of mismatch, Eq. (14) cannot be simplified. So the maximum INL can be calculated in LSB as

$$\mathrm{INL}_{\max} \approx \frac{\sigma_0\sqrt{2^{N-2}}}{C_0}, \tag{16}$$

which shows that the maximum INL is independent of the bypass window parameter K. The INL performance of the SAR ADC with multiple bypass windows (the standard deviation of the Gaussian error of the unit capacitor is 1%) is shown in Fig. 14, and it is the same with the INL performance of a conventional SAR ADC with the split capacitor array[29].

4. Split-and-recombination-based redundancy with adaptive bypass windows

In a high-resolution ADC with relatively high speed, variations on reference voltage lead to wrong decisions. The design avoids the large-area on-chip decoupling capacitor for stabilizing the reference by redundancy. The solution corrects the errors, and it is also favorable for the speed because the requirement for DAC settling is relaxed. Although the bypass logic offers redundancy since there are multiple output presentations for one identical input voltage[7], it is not enough for a 12-bit 30 M/s SAR ADC.

Compared with the binary-scaled error compensation redundancy[32], the split-and-recombination redundancy[19] does not need extra compensation capacitors and the sampling capacitance and input range remains unchanged. The main idea of split-and-recombination redundancy is to split MSB into two groups and make the smaller group recombine with LSB capacitors. The most critical point is that each capacitor is not larger than the sum of capacitors smaller than it so that multiple output codes are assigned to one same input signal. A split-and-recombination method (1-bit) shown in Fig. 15 is chosen under the consideration of speed. For designing the digital error correction circuit, it is necessary to derive the expression of D_{out} first.

4.1. Without bypass logic

If the bypass logic is not applied, the D_{out} can be written as Fig. 16. And D_{out} also can be expressed as Fig. 17. The digital error correction logic can be designed according to this expression similar to the implementation in Ref. [19].

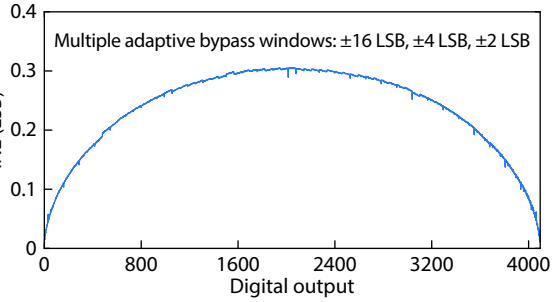

Fig. 14. INL performance of SAR ADC with multiple adaptive bypass windows.

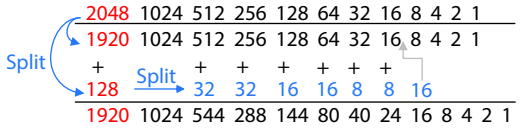

Fig. 15. Split-and-recombination method.

$$\begin{aligned}
&2^{10}+2^9+2^8+2^7\\
&\quad\shortparallel\\
D_{\mathrm{out}} &= B_{12}\times(2^{11}-2^7)+B_{11}\times 2^{10}+B_{10}\times(2^9+2^5)\\
&\quad+B_9\times(2^8+2^5)+B_8\times(2^7+2^4)+B_7\times(2^6+2^4)\\
&\quad+B_6\times(2^5+2^3)+B_5\times(2^4+2^3)+B_4\times 2^4+B_3\times 2^3\\
&\quad+B_2\times 2^2+B_1\times 2^1+B_0\times 2^0\\
&=2^{10}\times(B_{12}+B_{11})+2^9\times(B_{12}+B_{10})+2^8\times(B_{12}+B_9)\\
&\quad+2^7\times(B_{12}+B_8)+2^6\times B_7+2^5\times(B_{10}+B_9+B_6)\\
&\quad+2^4\times(B_8+B_7+B_5+B_4)+2^3\times(B_6+B_5+B_3)\\
&\quad+2^2\times B_2+2^1\times B_1+2^0\times B_0
\end{aligned}$$

Fig. 16. Expression of D_{out} without bypass logic.

w/o bypass

							B_8					
						B_{10}	B_7	B_6				
	B_{12}	B_{12}	B_{12}	B_{12}		B_9	B_5	B_5				
+	B_{11}	B_{10}	B_9	B_8	B_7	B_6	B_4	B_3	B_2	B_1	B_0	
D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	

Fig. 17. Expression of D_{out} without bypass logic.

4.2. With bypass logic

The proposed bypass logic requires us to know the weights of the bypassed cycles. For example, it needs to search four times without bypass logic for V_{in} = 8 as shown in Fig. 18. The weight of every bit is 8, 4, 2 and 1, respectively. So the output is obtained by $8\times1+4\times0+2\times0+1\times0=8$. For V_{in} = 8 with bypass logic, the first and second cycles are bypassed. So V_{in} must be located in areas I and II. The third and fourth comparison results are 1 and 0, respectively. So the output is $XX10$ (X stands for the bit bypassed). In this way, the output can be expressed as $4\times1+2\times1+2\times1+1\times0=8$.

In short, bypassing one bit requires the addition of half weight of this bit to the output regardless of binary or non-binary weight. In accordance with this general conclusion for bypass logic, the D_{out} can be expressed as shown in Fig. 19 and

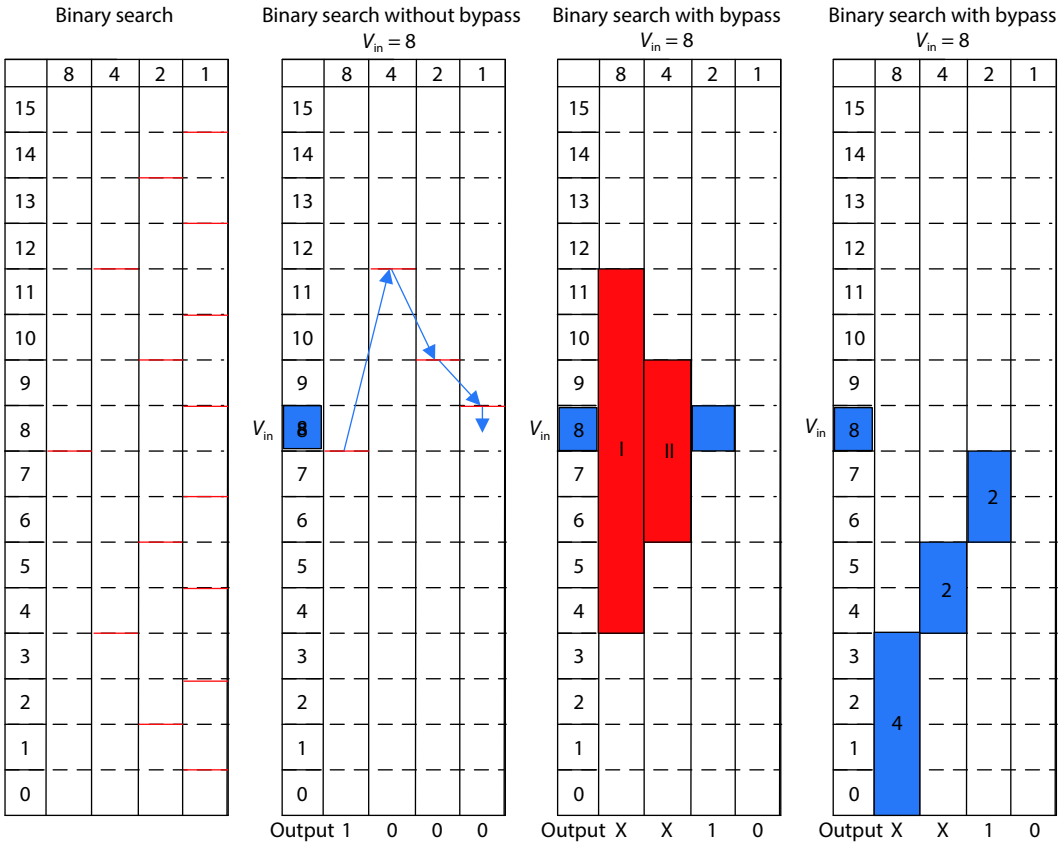

Fig. 18. (Color online) Binary search with and without bypass logic.

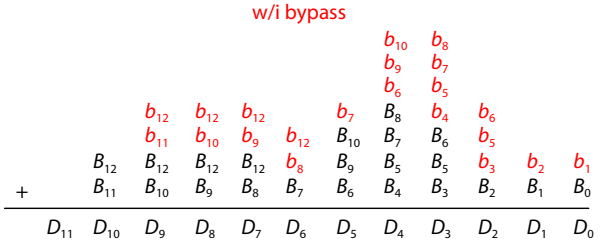

Fig. 19. Expression of D_{out} with bypass logic.

red b_n represents the nth bypassed cycle. According to the expression of D_{out}, digital error correction as shown in Fig. 20 rather than ROM[33] or off-chip correction can be implemented by full adders, DFFs and XORs.

Adding the redundancy decreases weights of LSBs as well, e.g., the weights of C_6 and C_5 change from 16 and 8 to 10 and 6. Because the window sizes are updated along with capacitors, smaller weights of LSBs refine the step size of the update, which makes the bypass logic more power-efficient.

5. Simulation results and comparisons

The proposed 12-bit SAR ADC is designed in 40 nm CMOS technology. Fig. 21 shows the FFT plot of the ADC output at transistor-level simulation with a pad model. At a sampling rate of 30 MS/s, the ADC achieves an ENOB of 11.12-bit with 14.30 MHz input. The SNDR and SFDR are 68.72 and 85.35 dB, respectively. Fig. 22 shows the stable SNDR and SFDR versus different input frequency.

The total power consumption at Nyquist frequency is 380 μW. It can be broken down as shown in Fig. 23: 63% from capacitor switching and DAC buffers; 26% from digital logic; 9% from comparator and 2% from bootstrapped switches. According to the Walden FoM equation

$$\text{FoM} = \frac{\text{Power}}{2^{\text{ENOB}} \times f_s}, \tag{17}$$

the resultant FoM of the ADC is 5.69 fJ/conversion-step. If the bypass logic is shut down, the total power consumption increases 12.4% to 427 μW.

Table 1 summarizes the simulated performance with a comparison to state-of-the-art SAR ADCs with time-domain comparators. This design achieves a competitive position, suggesting that the performance of SAR ADCs assisted with NOC of the VCO-based comparator can be significantly enhanced with the proposed techniques.

6. Conclusion

This paper proposes a technique to set multiple adaptive bypass windows by using the number of oscillation cycles (NOC) of the VCO-based comparator, which is applied in a 30 MS/s 12-bit SAR ADC. The decrease of bit cycles, power consumption and improvement of the static performance with multiple adaptive bypass windows are analyzed in detail respectively. Enabling multiple adaptive bypass windows saves power by 12.4%. Besides, a 1-bit split-and-recombination redundancy and a general digital error correction method in bypass logic for correcting settling errors are proposed. The redundancy contributes to the overall speed and refines bypass windows as well. The proposed ADC achieves an ENOB of 11.12-bit and 85.35 SFDR at transistor level simulation, achieving a FoM of 5.69 fJ/conversion-step at 1.1 V supply with Nyquist input.

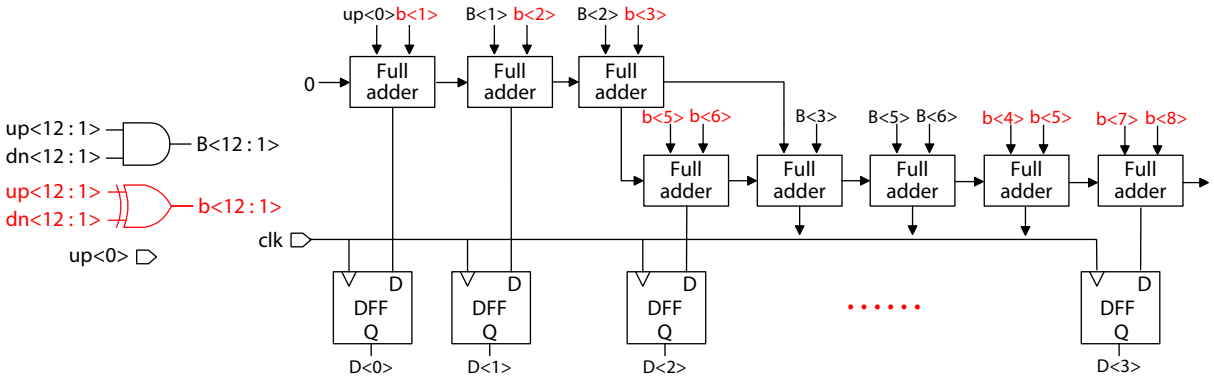

Fig. 20. Part of implementation of digital error correction logic.

Table 1. Performance comparison of SAR ADCS with time-domain comparators.

Parameter	JSSC 2011[10]	TCAS-I 2013[33]	JSSC 2014[34]	ESSCIRC 2014[12]	JSSC 2016[24]	JSSC 2017[11]	JSSC 2019[17]	This Work
Technology (nm)	180	130	180	65	90	65	40	40
Comparator type	VCDL	VCDL	VCDL hybrid	VCO	TDC hybrid	Edge-pursuit	VCO	VCO
Calibration	No	Yes	No	Yes	Yes	Yes	No	No
Supply voltage (V)	0.6	0.5	0.6	0.85	0.7	N/A	1.1	1.1
Conversion rate (MS/s)	0.1	0.01	0.1	1.024	4	0.02	10	30
Resolution (bit)	10	11	10	13	10	15	10	12
SFDR (dB)	64	78	64.2	85.2	71.5	95.1	68.84	85.35
SNDR (dB)	57.5	61.6	56.5	66.4	54.8	74.12	58.57	68.72
ENOB (bit)	9.3	9.93	9.2	10.4	8.81	12.02	9.44	11.12
Powe (μW)	1.3	0.73	0.39	45.2	9.25	1.17	47.6	380
FoM (fJ/Conv.-step)	21	74.8	6.7	33	5.16	14.06	6.85	5.69

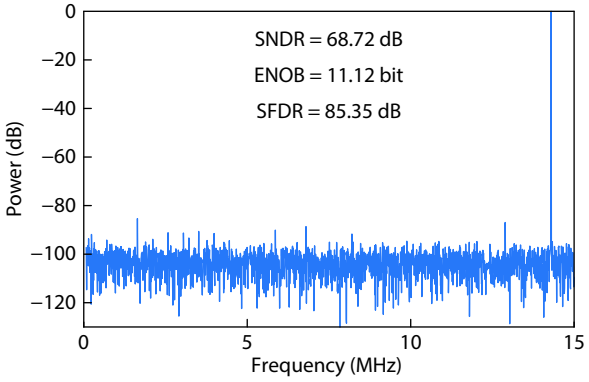

Fig. 21. (Color online) FFT plot with Nyquist input at 30 MS/s.

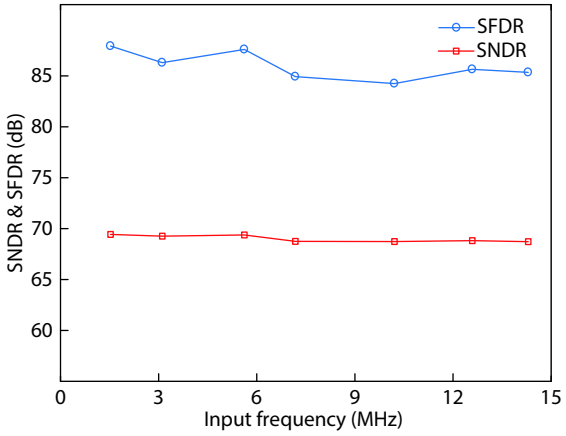

Fig. 22. Dynamic performance versus input frequency.

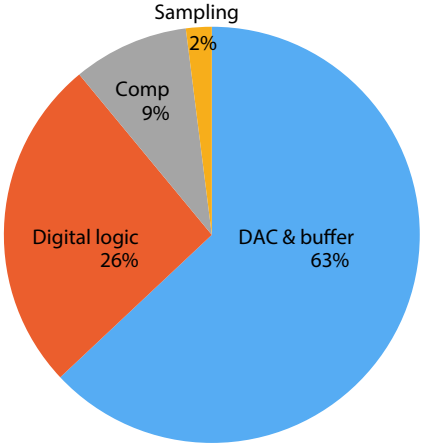

Fig. 23. (Color online) Power breakdown at Nyquist frequency.

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