REVIEWS

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CMOS analog and mixed-signal phase-locked loops: An overview

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Abstract: CMOS analog and mixed-signal phase-locked loops (PLL) are widely used in varies of the system-on-chips (SoC) as the clock generator or frequency synthesizer. This paper presents an overview of the AMS-PLL, including: 1) a brief introduction of the basics of the charge-pump based PLL, which is the most widely used AMS-PLL architecture due to its simplicity and robustness; 2) a summary of the design issues of the basic CPPLL architecture; 3) a systematic introduction of the techniques for the performance enhancement of the CPPLL; 4) a brief overview of ultra-low-jitter AMS-PLL architectures which can achieve lower jitter (< 100 fs) with lower power consumption compared with the CPPLL, including the injection-locked PLL (ILPLL), sub-sampling (SSPLL) and sampling PLL (SPLL); 5) a discussion about the consideration of the AMS-PLL architecture selection, which could help designers meet their performance requirements.

Key words: phase-locked loop (PLL); charge-pump based PLL (CPPLL); ultra-low-jitter PLL; injection-locked PLL (ILPLL); sub-sampling PLL (SSPLL); sampling PLL (SPLL)

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1. Introduction

CMOS phase-locked loops (PLL) are widely used in most of the system-on-chips (SoC) as the clock generator for digital circuits and wireline transceivers, or the frequency synthesizer for the wireless transceivers. Recently, with the continuous scaling of the CMOS technology, the all-digital PLL (ADPLL) becomes popular mainly because of the advantages of the scalability in advanced CMOS technology and the design portability across technologies[1]. However, compared to the widely used analog and mixed-signal PLL (AMS-PLL)[2], the ADPLL usually suffers from the issues of higher jitter due to the quantization noise and higher sensitivity to power supply noise[2]. This makes the AMS-PLL still be a desirable choice even at the 10-nm technology node and beyond[2].

In this paper, an overview of the AMS-PLL is presented. The rest of this paper is organized as follows. Section 2 presents a brief introduction of the basics and the design issues of the CPPLL, which is the most widely used AMS-PLL architecture due to its simplicity and robustness. Section 3 presents a systematic introduction of the techniques for the performance enhancement of the CPPLL. Section 4 briefly introduces the ultra-low-jitter AMS-PLL architectures, including the injection-locked PLL (ILPLL), sub-sampling PLL (SSPLL) and sampling PLL (SPLL), which can generate the clock with sub-100-fs jitter and lower power consumption compared with the CPPLL to meet the strict jitter requirement of some applications such as the local oscillation (LO) generator for millimeter-wave (mm-wave) 5G communication. Section 5 shows the discussion about the consideration of the AMS-PLL architecture selection, which could help designers meet their performance requirements. Section 6 concludes this work.

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2. Basics and design issues of the CPPLL

2.1. Basics

Fig. 1(a) shows the block diagram of the basic CPPLL[3, 4]. It consists of a tri-state phase/frequency detector (PFD), a charge pump, a low-pass filter (LPF), a voltage-controlled oscillator (VCO) and a divide-by-*N* frequency divider (div_*N*). The ratio between the VCO output frequency (f_{VCO}) and the reference frequency (f_{REF}) is *N*. The delta–sigma modulator (DSM) is used to modulate the division ration of the divider so as to obtain a fractional division ratio to achieve the function of the fractional-*N* PLL[3]. For the integer-*N* PLL, of which *N* is an integer number, the DSM is not required.

The operation principle of the CPPLL is presented by the timing diagram shown in Fig. 1(c). The division ratio shown in Fig. 1(c) is 2 as an example. Φ_{IN} shown in Fig. 1(c) is the input phase error between the reference clock (REF) and the divider feedback clock (DIV). When the PLL is unlocked and Φ_{IN} is positive, Φ_{IN} is detected by the PFD and CP generates a positive current pulse I_{CP} to charge the LPF so as to increase f_{VCO} to reduce Φ_{IN}. If Φ_{IN} is negative, CP generates a negative current pulse I_{CP} to discharge the LPF so as to decrease f_{VCO} to reduce $|\Phi_{IN}|$. At the locking state, Φ_{IN} keeps zero so that the VCO tuning voltage V_C (see Fig. 1(a)) keeps stable. As a result, $f_{VCO} = N f_{REF}$ (*N* shown in Fig. 1(c) is 2).

As indicated in Fig. 1(c), the pulse width of I_{CP} equals to $|\Phi_{IN}|$. Hence, the average CP output current is proportional to the Φ_{IN}, as the PFD/CP transfer curve shown in Fig. 1(b). As we can see, the gain of PFD/CP, K_{PFD}, is $I_{CP}/(2\pi)$. Unlike the PLLs with other types of the phase detector (PD) such the XOR gate and mixer, which suffer from the issue of limited frequency lock range due to the limited monotonic Φ_{IN} range of these PDs[5], the lock range of the PFD-based PLL is unlim-

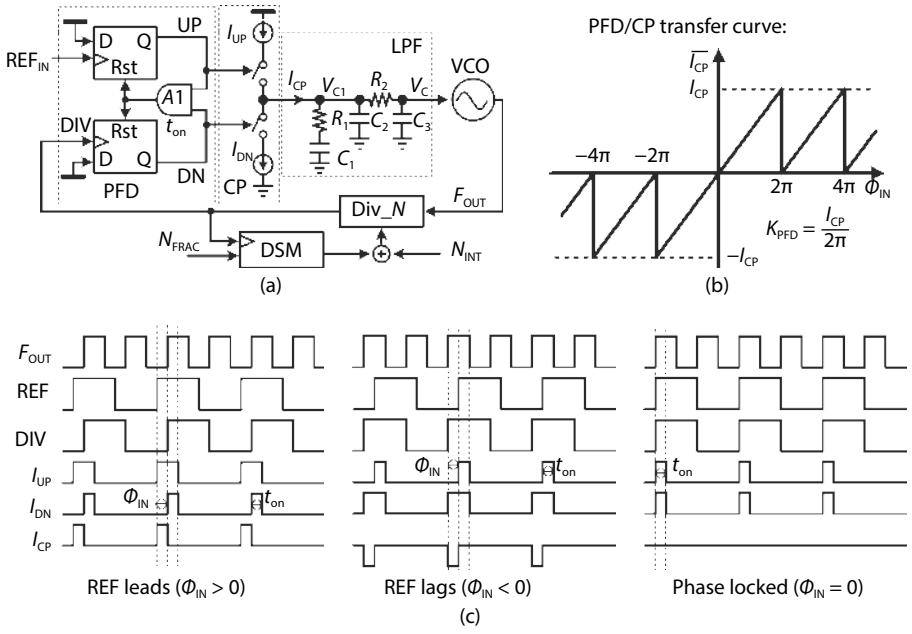
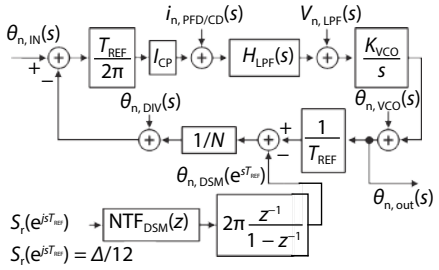


Fig. 1. (a). Block diagram of the basic CPPLL. (b) Transfer curve of PFD and CP. (c) Timing diagram.

Linear phase noise model:



$\theta_{n,IN}(s)$: Input phase noise
$i_{n,PFD/CP}(s)$: PFD/CP noise
$V_{n,LPF}(s)$: LPF voltage noise
$\theta_{n,VCO}(s)$: VCO phase noise
$S_r(e^{jsT_{REF}})$: DSM quantization noise
Δ : DSM quantization step
$NTF_{DSM}(z)$: NTF of DSM
$H_{LPF}(s)$: Transfer function of LPF
T_{REF} : Reference period
$\theta_{n,out}(s)$: PLL total phase noise

Loop dynamics:

Open-loop gain: $G_{ol}(s) = I_{CP}H_{LPF}(S)K_{VCO}/(2\pi sN)$ Closed-loop gain: $H_{cl}(s) = G_{ol}(s)/(1 + G_{ol}(s))$

Loop bandwidth: $\omega_{BW} \approx I_{CP}R_1K_{VCO}/(2\pi N) \times C_1/(C_1 + C_2 + C_3)$, $C_1 \gg C_2, C_3$

Phase margin: $\varphi_m \approx \tan^{-1}(\omega_{BW}/\omega_Z) - \tan^{-1}(\omega_{BW}/\omega_{p1}) - \tan^{-1}(\omega_{BW}/\omega_{p2})$

$\omega_{BW} = 1/(R_1C_1)$, $\omega_{p1} = 1/(R_1(C_2+C_3))$, $\omega_{p2} = 1/(R_1(C_2+C_3)/(C_2+C_3))$

NTF of each building block:

Noise source	Noise transfer function (NTF)		
Input phase noise	$\theta_{n,out}(s)/\theta_{n,IN}(s)$	$\lvert N \times H_{cl}(s)\rvert^2$	Low-pass
PFD/CP noise	$\theta_{n,out}(s)/i_{n,PFD/CP}(s)$	$\lvert(2\pi N/I_{CP}) \times H_{cl}(s)\rvert^2$	Low-pass
LPF noise	$\theta_{n,out}(s)/V_{n,LPF}(s)$	$\lvert(K_{VCO}/s) \times (1/(1 + G_{ol}))\rvert^2$	Band-pass
VCO phase noise	$\theta_{n,out}(s)/\theta_{n,VCO}(s)$	$\lvert1/(1 + G_{ol})\rvert^2$	High-pass
Divider phase noise	$\theta_{n,out}(s)/\theta_{n,DIV}(s)$	$\lvert N \times H_{cl}(s)\rvert^2$	Low-pass
DSM phase noise	$\theta_{n,out}(s)/\theta_{n,DSM}(e^{sT_{REF}})$	$(1/T_{REF}) \times \lvert T_{REF}H_{cl}(s)\rvert^2$	Low-pass

Fig. 2. Linear phase noise model, CPPLL loop dynamics, and noise transfer functions of each building blocks.

ited because the linear Φ_{IN} range of the tri-state PFD is from -2π to 2π (see Fig. 1(b)), and the PFD output polarity keeps positive or negative when $\Phi_{IN} > 2\pi$ ($f_{REF} > f_{VCO}/N$) or $\Phi_{IN} < -2\pi$ ($f_{REF} < f_{VCO}/N$), respectively. This makes the PFD be able to distinguish the polarity of the frequency difference between f_{REF} and (f_{VCO}/N) so that an additional frequency-locked loop with a separated frequency detector for initial frequency acquisition is not required. Hence, the CPPLL architecture is simple and robust, and thus, the CPPLL becomes the most widely used AMS-PLL architecture.

Fig. 2 shows linear phase domain model of the CPPLL[5, 6]. The noise transfer functions (NTF) of all the building blocks, and the expressions of loop bandwidth and phase margin are illustrated in Fig. 2 according to the analysis presented in Refs. [5, 6].

2.2. Design issues

As introduced in Section 2.1, the CPPLL is a simple and robust PLL architecture. However, it suffers from several design issues, which limit the CPPLL performances. In this subsection, six main design issues of the CPPLL are briefly introduced and discussed as follows.

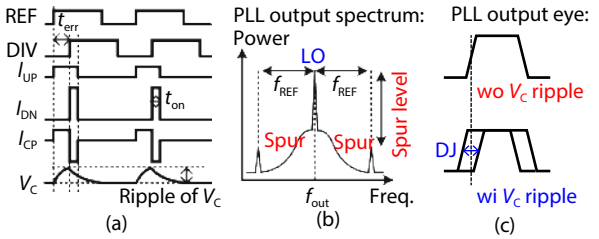


Fig. 3. (Color online) (a) Timing diagram of the CPPLL with CP current mismatch. (b) V_C-ripple-induced reference spur on the PLL output spectrum. (c) V_C-ripple-induced deterministic jitter (DJ) on the PLL output clock eye.

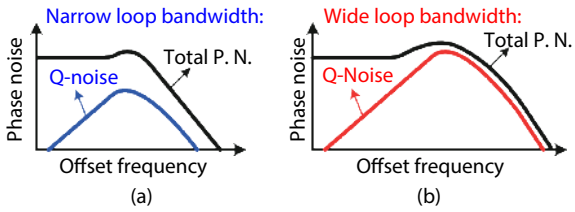


Fig. 4. (Color online) Quantization noise effect with (a) narrow and (b) wide loop bandwidth, respectively.

First, as shown in Fig. 3(a), at the locking state of the CPPLL, the CP current mismatch causes a voltage ripple on the VCO tuning voltage (see V_C in Fig. 1(a)). Such voltage ripple causes a periodic frequency disturbance, and thus, induces spurious tones (reference spur) at the offset frequency of $\pm f_{REF}$ in the PLL output spectrum (see Fig. 3(b)) or deterministic jitter (DJ) in the PLL output clock eye (see Fig. 3(c)). For the wireless transceiver, the spurious tones around LO induce reciprocal mixing in a wireless transceiver. This causes emission mask violation on the transmitter side and degraded signal-to-noise ratio (SNR) on the receiver side[7]. For the high-speed wireline transceiver, the DJ degrades the eye quality of the transmitted data at the transmitter side, and thus, causes degradation of the bit error rate (BER) at the receiver side[7]. A narrow loop bandwidth ω_{BW} with small poles (ω_{p1} and ω_{p2}) can be selected to suppress the reference spur but comes with the penalty of longer PLL locking time and less suppression of VCO phase noise because the characteristic of the VCO NTF is high-pass, as indicated in Fig. 2.

Second, as the phase margin formula illustrated in Fig. 2, the zero ω_Z should be adequately smaller than the loop bandwidth ω_{BW}. This necessitates a large integral capacitor C_1 (see Fig. 1(a)), which occupies large area, especially in the case of small loop bandwidth. C_1 can be reduced with the same loop bandwidth by choosing a large R_1 and small CP output current I_{CP}, as indicated by the loop bandwidth formula shown in Fig. 2. However, this raises the level of the phase noise induced by the CP and LPF, as indicated by the NTFs shown in Fig. 2.

Third, as discussed above, a large I_{CP} is required to suppress the in-band phase noise so as to reduce the integrated jitter of the PLL output clock. But this comes with the penalty of large power consumption.

Fourth, in the fractional-N PLL, a small loop bandwidth is required to suppress the quantization noise (Q-noise) induced by the DSM, as indicated in Fig. 4. This also slows down the PLL settling process and degrades the VCO phase noise suppression.

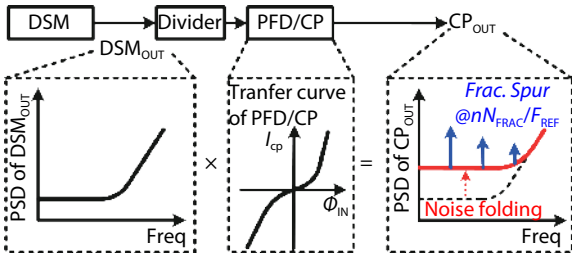


Fig. 5. (Color online) Degradation of the in-band phase noise and fractional spur due to the PFD/CP nonlinearity.

Fifth, in the fractional-N PLL, since the range of the input phase error is usually more than one VCO period at locking state because the division ratio of the divider is modulated by the DSM, the nonlinearity of the PFD/CP I/O characteristics, which are induced by the CP current mismatch and the PFD non-ideality, degrade the in-band phase noise due to the DSM quantization noise folding[8–13], as illustrated in Fig. 5. Furthermore, such nonlinearity also degrades the fractional spur level[9–13], which is at the offset frequency of $N_{Frac}f_{REF}$ (N_{Frac} is the fractional part of the division ratio) and its harmonics (see Fig. 5). The fractional spur is difficult to be suppressed by the LPF if the spur frequency is lower than the loop bandwidth (in-band fractional spur).

Last, if a long divider chain is required to obtain a large division ratio, the divider noise may significantly degrade the PLL in-band phase noise. Furthermore, in the fractional-N PLL, since the division ratio is modulated by the DSM, the divider delay as well as the transition edge of the divider output is also modulated by the DSM. This further degrades the PLL in-band phase noise[3].

3. Techniques for CPPLL performance enhancement

This section gives a systematic introduction of the CPPLL performance enhancement techniques which were proposed to mitigate the CPPLL design issues presented in Section 2.2, including (1) reference spur suppression techniques, (2) area reduction technique, (3) in-band phase noise suppression technique, (4) power reduction technique, (5) fast settling techniques, (6) CP linearization techniques, and (7) quantization noise reduction techniques.

3.1. Reference spur suppression technique

As discussed in Section 2, to reduce the reference spur level, it is essential to reduce the CP current mismatch. This can be achieved by adopting the CP with current mismatch suppression techniques[14–27] or the CP current mismatch calibration techniques[28–31].

Fig. 6(a) shows the CP using an op amp to suppression the current mismatch, which was firstly proposed in Ref. [14] and is now widely used in the CPPLLs[15–20]. The key idea is to using an op amp based negative feedback loop to keep the drain voltage V_R (see Fig. 6(a)) almost equals to the CP output voltage V_{OUT} so as to make the source–drain voltages of M1 and M2 equal to those of M3 and M4, respectively. This makes I_{UP} and I_{DN} approximately equal to $AI_{replica}$ (A and $I_{replica}$ are shown in Fig. 6(a)) so that the current mismatch can be effectively suppressed. However, nodes N and P share charge with the LPF (node V_{OUT}) at the off-state. This is the

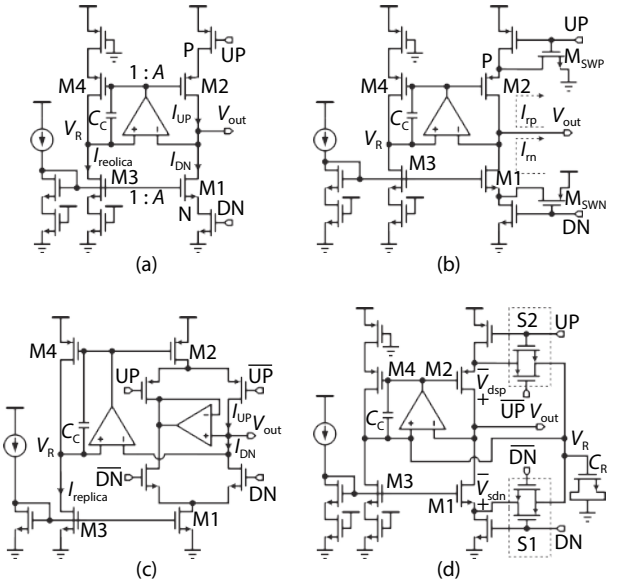


Fig. 6. Schematics of CPs with current mismatch suppression techniques.

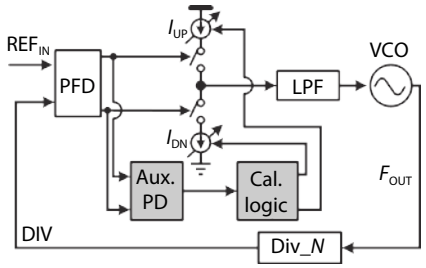


Fig. 7. Conceptual block diagram of the CPPLL with CP current mismatch calibration technique.

charge sharing effect[21], which causes long switch-off time of the CP[22]. To alleviate this issue, Ref. [22] proposed a modified version shown in Fig. 6(b). Two additional switches M_{SWP} and M_{SWN} are added to remove the charge shored on the nodes P and N respectively so as to mitigate the charge sharing effect. However, as analyzed in Ref. [23], it suffers from the issue of reversed sub-threshold leakage at the off-state (see I_{rp} and I_{rn} in Fig. 6(b)), especially if the circuit is implemented in nanometer CMOS technology and V_{OUT} is near supply or ground. Although this issue can be avoided by combining the current mismatch suppression technique with the current-steering CP circuit[24–27] (see Fig. 6(c)), which is also widely used due to its fast switching speed, it is power hungry. To solve this problem, Ref. [32] reported a source-switched CP with reverse leakage compensation technique, as shown in Fig. 6(d), which combines the advantages of the CPs shown in Figs. 6(b) and 6(c). The op amp in this CP is used not only to suppress the current mismatch but also to compensate the reverse leakage by keeping V_{sdn} and V_{sdp} (see Fig. 6(d)) to be zero at off-state.

Besides the current mismatch suppression techniques of CP, the current mismatch calibration techniques[28–31] are also wide used to reduce the current mismatch. The conceptual block diagram of the PLL with the current mismatch calibration technique is shown in Fig. 7. Compared with the basic CP-PLL, an auxiliary phase detector is added to detect the input phase error for the calibration logic to adjust the I_{UP} or I_{DN} of

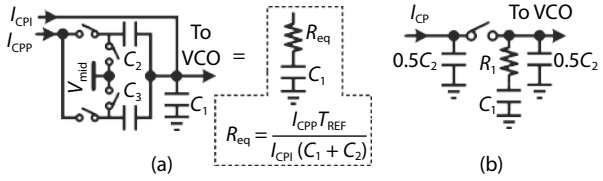


Fig. 8. Examples of (a) SC-LPF[33] and (b) SC-LPF with RC-LPF (sampling loop filter)[3].

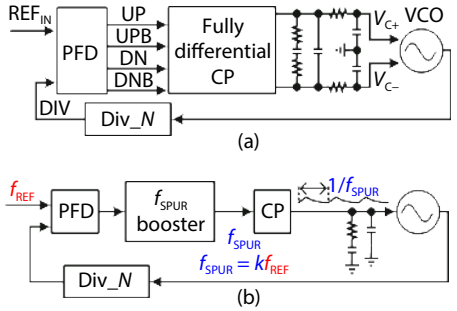


Fig. 9. (Color online) Conceptual block diagram of (a) fully differential CPPLL and (b) CPPLL with spur frequency boosting technique.

the CP accordingly so as to make the input static phase error close to zero at locking state (this means $I_{UP} \approx I_{DN}$). The lock detector is used to judge if the PLL is locked or not. The CP calibration logic is enabled only when the PLL is locked, which is controlled by a lock detector (LD). Using the current mismatch calibration technique, the CP design challenges can be mitigated. But it requires additional calibration time, which causes longer PLL settling process.

The spur level can also be reduced by using the switched-capacitor based loop filter (SC-LPF)[3, 33–35] or combine the SC-LPF with the widely used RC-LPF. Fig. 8 shows two examples. Using the SC-LPF, the ripple due to the CP current mismatch can be blocked by the switches so as to reduce the spur level without the penalty of settling time.

The fully-differential PLL architecture[19, 36–39] can reduce the spur level induced by the PFD mismatch and common-mode interference induced by the supply and ground, as the simplified block diagram shown in Fig. 9(a). The fully-differential tuned VCO and fully-differential CP are used in such PLL.

If the frequency of the spur is boosted with the same LPF, the spur level can be reduced. Hence, Refs. [40, 41] proposed to boost the spur frequency by boosting the frequency of the CP turns-on pulse with an f_{SPUR} booster, as the conceptual block diagram shown in Fig. 9(b).

3.2. Area reduction techniques

As discussed before in Section 2.2, the integral capacitor of the basic CPPLL (see C_1 in Fig. 1(a)) usually occupies large area, especially in the case of large I_{CP} or a small loop bandwidth. Hence, the key point for the CPPLL area reduction is to shrink the area of the integral capacitor.

The first technique is the capacitance multiplication technique. Ref. [5] shows several active capacitance multipliers using the op amp to boost the equivalent capacitance. Fig. 10(a) shows two examples, which are used in Refs. [42, 43]. The main design challenge of these capacitance multipliers is that the op amp requires low noise and large output voltage range simultaneously. This usually results in high power consumption.

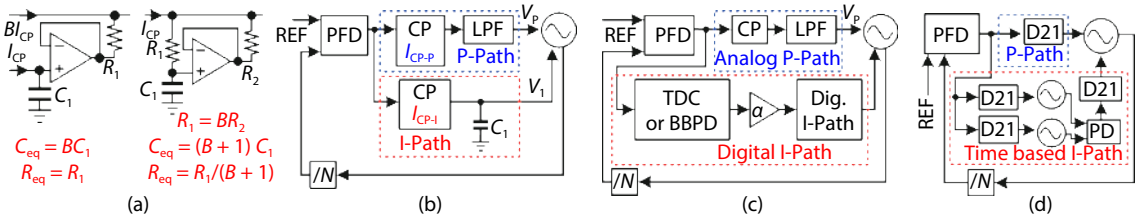


Fig. 10. (Color online) Area reduction techniques: (a) capacitance multiplier, (b) dual-path loop CPPLL, (c) hybrid digital PLL, and (d) time-based PLL.

A more effective way is to split the single loop path of the basic CPPLL (see Fig. 1(a)) into a proportional path (P-Path) and an integral path (I-Path), as the dual-path loop CP-PLL[44–46] shown in Fig. 10(b). By setting a small I_{CP_I} ($I_{CP\_I} \ll I_{CP\_P}$, see Fig. 10(b)), the capacitance of the integral capacitor C_1 can be reduced without changing the loop dynamics[45], and no additional op amp is required. Furthermore, the loop parameters are more flexible to be designed since the loop bandwidth selection is decoupled from the capacitance of the integral capacitor C_1[45]. To further reduce area, the analog integral path shown in Fig. 10(b) can be replaced by a digital integral path, as the hybrid digital PLL[47–51] shown in Fig. 10(c). The integral path consists of a bang-bang phase detector[47–50] or a time-to-digital converter (TDC)[51] and a digital accumulator. By setting the gain of the accumulator (see α in Fig. 10(c)) sufficiently small, the quantization noise induced by the integral path can be negligible, and the loop dynamics is still dominated by the analog proportional path. Hence, such architecture can combine the advantages of low noise of the CPPLL and small area of the ADPLL.

If a very compact area is required, the time-based PLL architecture[52, 53] can be adopted, as shown in Fig. 10(d). Since only two ring oscillators (RO) are used as the time-domain integrator, the area can be very tiny, even compared with the area of the hybrid digital PLL. However, the additional noise induced by the two ROs worsens the PLL jitter, and any mismatch between the two ROs significantly degrades the reference spur[53].

3.3. In-band phase noise reduction techniques

The main source of the in-band phase noise is the CP current noise. Besides the straightforward way of increasing I_{CP}, as mentioned before, the pulse width of dead-zone mitigation pulse (see t_{on} in Fig. 1) is also required to be minimized, as indicated by the NTF of PFD/CP illustrated in Fig. 2. To achieve this, the true single-phase clocking (TSPC) PFD are desirable due to its simple logic and short delay path[54]. In addition, the source degeneration technique can also be used to reduce the current noises of current sources in the CP[55, 56], and the ratio between the CP bias current and the CP output cannot be too small.

To further reduce the CP-induced in-band phase noise, increasing the phase detector (PD) gain is required. Due to the advantage of the equivalent high PD gain at low input jitter, the BBPD, which is popular for ADPLL design, has also been proposed for the CPPLL to suppress the CP noise[57]. But it suffers from the issue of poor gain control of the BBPD. Due to the absence of the CP in the type-I PLL proposed in Ref. [58], low in-band phase noise is achieved. But the PD gain of the PLL reported in Ref. [58] varies with the VCO tuning voltage[58].

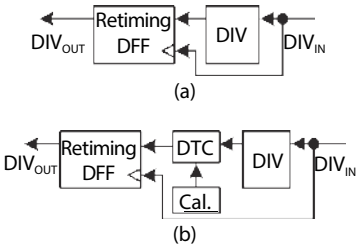


Fig. 11. (a) Divider with retiming DFF. (b) Divider with retiming DFF and calibration circuit for preventing metastability issue.

As discussed in Section 2.2, the divider noise also degrades the PLL in-band phase noise. To mitigate the effect of divider noise, a retiming D-flip-flop is usually used to remove the jitter accumulation of the divider[59], as shown in Fig. 11(a). Hence, the output noise of the divider only contains the retiming DFF noise, and thus, the divider noise is significantly suppressed. However, in the case of long divider chain, the delay of the divider varies much with process, voltage and temperature (PVT) variation. This may cause metastability issue of the retiming DFF. To solve this problem, a digital-to-time converter (DTC) and calibration logic circuits (see Fig. 11(d)) are used to control the delay of the DTC automatically so as to avoid the metastability issue[60].

3.4. Power reduction techniques

As discussed in Section 3.2, increasing the CP output current as well as the CP bias current can reduce the CP-induced noise. This increases CP power consumption. To reduce CP dc power without in-band phase degradation, the gated CP[61] can be used, in which the replica bias branch is turned-off when the CP is at the off-state, as shown in Fig. 12(a). To achieve gating operation while maintain adequate CP current matching performance, an improved gated CP reported by Ref. [62] can be used, as shown in Fig. 12(b).

The prescaler of the divider chain is usually power hungry, especially in the case of high VCO frequency. Hence, several low-power prescaler circuits can be used, including the injection-locked frequency divider[63–66] and dynamic latch based divider[67–69]. For the multi-modulus divider (MMD), which is required to generate multiple division ratios, the TSPC logic[70] instead of the current-mode logic (CML) are recommended if f_T of the process is high enough to achieve the required operation speed. The retiming DFF is also power hungry if the VCO frequency is high. So, it can operate at the frequency of the prescaler output instead of the VCO frequency to save power[37], as shown in Fig. 12(c). But the low-noise prescaler is required[66] because its noise is not removed by the retiming DFF.

In some case, if the divider operation frequency is not so

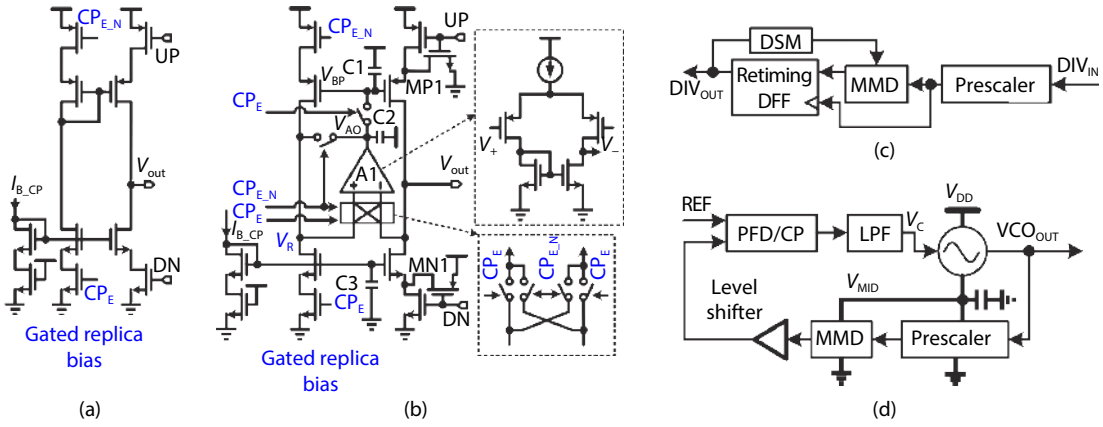


Fig. 12. (Color online) (a) Gated CP. (b) Gated CP with current mismatch suppression technique. (c) Retiming DFF operates at prescaler output frequency. (d) PLL with current reuse technique.

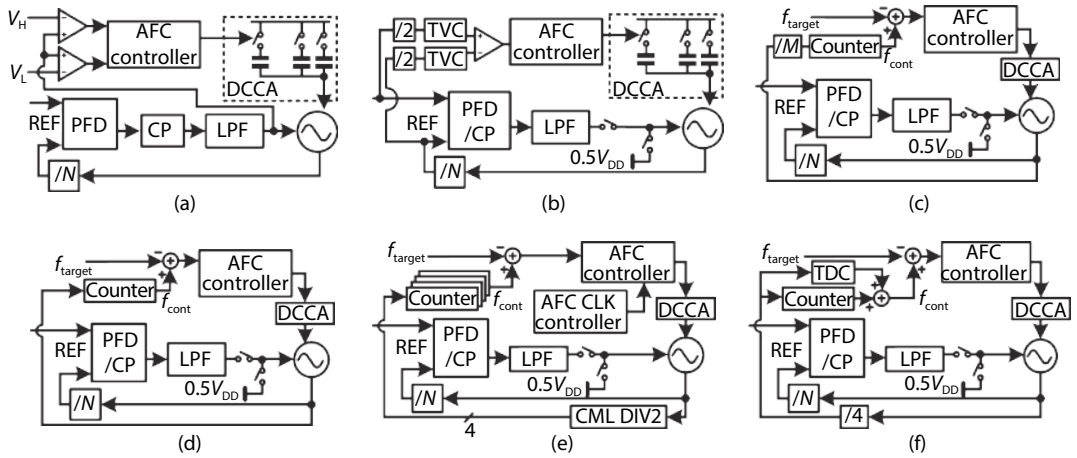


Fig. 13. AFC techniques: (a) V_{tune} monitoring technique, (b) relative period comparison technique, (c) counter-based AFC, (d) VCO-counting AFC, (e) four-phase counting AFC, and (f) TDC-assisted AFC.

high that it can operate at lower supply voltage, the current-reuse technique[71, 72] can be used to reduce power by stacking the VCO with the high-frequency prescaler and the MMD between the supply and ground, as shown in Fig. 12(d).

To extremely save power consumption for the low-power applications such as the internet-of-thing (IoT), the low-voltage PLL[17, 46, 62, 73–80] (supply voltage ⩽ 0.7 V) with several low-voltage circuit design techniques can be adopted.

3.5. Fast settling techniques

Usually, in a wideband PLL, the VCO is designed with a digitally-controlled capacitor array (DCCA). So, the VCO can cover several frequency bands to achieve a wide frequency range and a low VCO tuning gain, which is required to lower down the VCO phase noise caused by the amplitude-to-phase (AM-PM) noise conversion[81] and the LPF-induced phase noise (see the NTF of the LPF in Fig. 2). Thus, the auto-frequency control (AFC) techniques are required to automatically find the frequency band whose central frequency is nearest to the target frequency. After AFC searching process, the PLL enters the fine locking process to achieve phase and frequency locking. Hence, the PLL fast settling technique includes two parts: the fast AFC techniques and fast fine locking techniques.

Fig. 13 presents six AFC techniques[82–91]. The first one is the V_{tune} monitoring technique based AFC[82, 83], as shown in Fig. 13(a). Using this technique, the PLL loop keeps closed, and the DCCA optimal code is selected when the VCO tuning voltage V_{tune} is finally settled between two predetermined voltages (see V_H and V_L in Fig. 13(a)). If V_{tune} is higher than V_H or lower than V_L, the AFC controller (see Fig. 13(a)) adjusts the DCCA code accordingly and finally the AFC controller finds the optimal DCCA code. Due to the feature of closed loop, using this technique takes long settling time for the AFC process.

The second AFC technique is the relative period comparison technique[84, 85], as illustrated in Fig. 13(b). This is an open-loop based AFC technique. The difference between the period of divided VCO and that of the reference clock is first converted to a voltage difference ΔV (see Fig. 13(b)) by a time-to-voltage converter (TVC), and then the comparator gets the polarity of ΔV to decide if the VCO frequency is fast or slow so as to adjust the DCCA code accordingly. According to Ref. [84], this technique can achieve a very short AFC time (several μs or even sub-μs). But this work is not suitable for fractional-N PLL because its divider output period is not fixed but modulated by the DSM.

The third technique is the counter-based AFC[86], as shown in Fig. 13(c). This is also an open-loop AFC. The divided VCO frequency is counted by a counter first, and then,

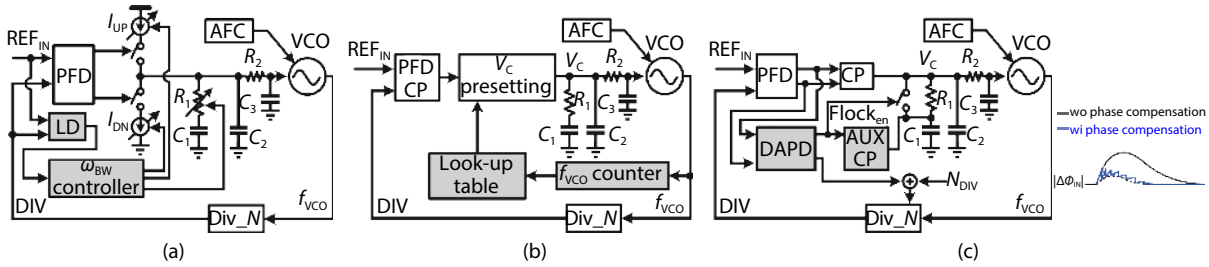


Fig. 14. Fast fine locking techniques: (a) dynamic loop bandwidth switching technique, (b) frequency presetting technique, and (c) dynamic phase error compensation (DPEC) technique.

the error between the counted VCO frequency f_{cont} (see Fig. 13(c)) and the target frequency code f_{target} is detected so as to adjust the DCCA code accordingly. Since the slow closed-loop settling process of the closed-loop AFC (see Fig. 13(a)) is avoided, and the VCO frequency can be estimated by the counter regardless of the integer-*N* or fractional-*N* mode, the counter-based AFC technique is widely used.

If the VCO frequency is not so high, the AFC speed can be improved by directly counting the VCO output[87–89], as shown in Fig. 13(d). This is because the required time for the VCO frequency counting can be reduced by directly counting the VCO output without the penalty of counting resolution, compared to the counter-based AFC shown in Fig. 13(c).

To further improve the AFC speed, the four-phase clock, which is generated by a CML divided-by-2 divider (DIV2) connected to the VCO output, can be used for VCO frequency counting[90], as shown in Fig. 13(e). Since the interval of each adjacent phase of the 4-phase clock from the CML DIV2 is half of the VCO period, the counting resolution can be doubled with the same counting time compared with the AFC shown in Fig. 13(d). In other words, the counting time can be halved with the same counting resolution to reduce the counting time of the AFC process. Furthermore, an AFC clock controller[90] can be used to double clock frequency of the AFC controller (used for frequency comparison and DCCA code searching) to further improve the AFC speed. The settling time of the AFC process reported in Ref. [90] is 1.25–1.86 μs with the reference frequency range from 15 to 50 MHz.

The last AFC technique is the TDC-assisted AFC technique[91], as shown in Fig. 13(f). A TDC is used to get a finer counting resolution than that shown in Figs. 13(c)–13(e) so as to achieve a very short AFC time (1.25 μs in Ref. [91]) by shortening the counting time. This technique is suitable for the PLL design with old process (the design in Ref. [91] was implemented in 180-nm CMOS) because a short AFC time can be achieved without directly counting the high-frequency VCO output.

After AFC process, the fine frequency locking process is required to make the PLL lock to the target frequency accurately. Hence, the fast fine locking techniques is necessary to accelerate such process. There are mainly three fine locking techniques, including the dynamic loop bandwidth switching technique[92, 93], frequency presetting technique[94–96], and dynamic phase error compensation (DPEC) technique[97].

Fig. 14(a) shows the CPPLL with dynamic loop bandwidth switching technique. A lock detector (LD) is used to detect the locking state of the PLL. If PLL is not locked, a large loop bandwidth is selected for fast locking by adjusting the CP current or the resistance of R_1 using the loop bandwidth controller. If the locking state is detected by the LD, a narrower loop bandwidth, which makes the PLL achieve its optimal phase noise performance[93], is selected.

However, the locking time may still not be fast enough with the dynamic loop bandwidth switching technique if the frequency difference between the initial frequency of the PLL after AFC process and the target frequency is not adequately small. To further speed up the fine frequency locking process, the frequency presetting technique can be used, as shown in Fig. 14(b). Initially, when start up, by sweeping the tuning voltage (V_C) and the DCCA code of VCO, the VCO frequencies at different V_C and DCCA control codes can be obtained and recorded by the look-up table. Hence, V_C can be preset nearest to the target frequency according to the look-up table to reduce the difference between the initial frequency and the target frequency so as to reduce the settling time.

However, even with the technique of loop bandwidth switching or frequency presetting, the PLL may still take a long time to remove the overshoot of the input phase error (see $\Delta\Phi_{IN}$ in Fig. 14(c)) during the PLL settling process[97]. This is called phase settling process. To further reduce the PLL settling time, the value of the phase error overshoot needs to be reduced to shorten the phase settling process. Based on this concept, the dynamic phase error compensation (DPEC) technique was proposed in Ref. [97], as shown in Fig. 14(c). A discriminator-aided phase detector (DAPD) is used to detect $\Delta\Phi_{IN}$ so as to adjust the division-ratio of the divider accordingly to compensate $\Delta\Phi_{IN}$. Thus, a small $\Delta\Phi_{IN}$ is kept during the PLL settling process so that a shorter phase locking time is achieved. Since $\Delta\Phi_{IN}$ is kept small, an auxiliary CP (Aux CP) is used to speed up the frequency acquisition process[97]. As a result, both frequency acquisition and phase settling process are accelerated simultaneously to reduce the PLL locking time.

3.6. CP linearization techniques

As discussed in Section 2. 2, the nonlinearity of PFD/CP I/O characteristics, which are induced by the CP current mismatch and the PFD non-ideality, degrade the in-band phase noise and fractional spur level. Although the techniques for CP current mismatch suppression (see Section 3.1) can improve the linearity of CP, the nonlinearity induced by the PFD non-ideality still exists. Hence, to further improve the linearity of PFD/CP, the most widely used method for the CPPLL is to induce an offset phase ($\Delta\Phi_{off}$) in the transfer curve of the PFD/CP, as shown in Fig. 15(a). $\Delta\Phi_{off}$ should be larger than half of the range of the input offset phase error at the lock-

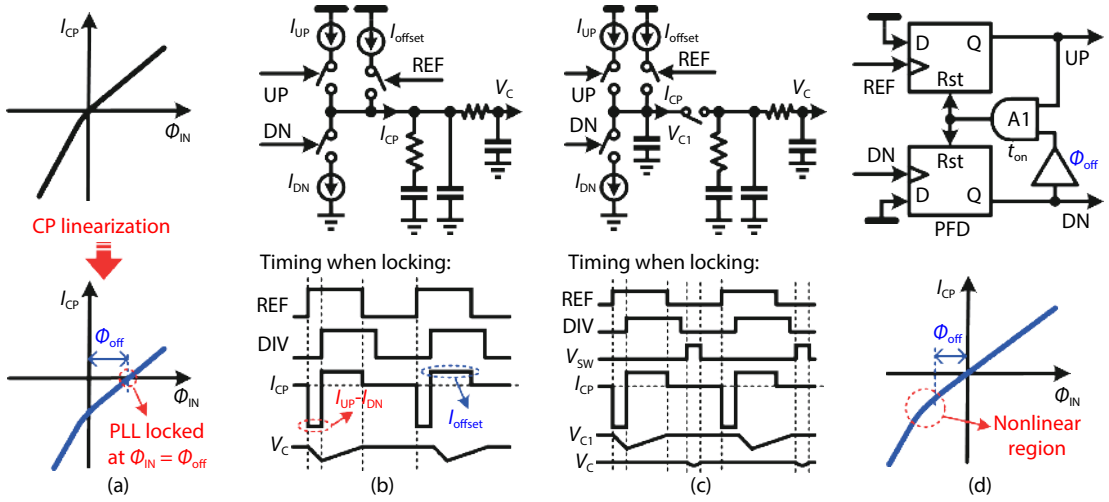


Fig. 15. (Color online) CP linearization techniques: (a) basic idea, (b) CP offset current technique, (c) CP offset current technique with sampling loop filter, and (d) PFD offset delay technique.

ing state so as to avoid the nonlinear region of the PFD/CP transfer curve.

To realize this idea, the widely used method is to add a gated-offset current[9, 11] branch in the CP, as shown in Fig. 15(b). By adding a small gated offset current I_{offset} (see Fig. 15(b)), the linearized transfer curve of the PFD/CP shown in Fig. 15(a) can be achieved. The issue of adding an offset current is that an additional voltage ripple is induced on the VCO tuning voltage V_C, which degrades the spur level. To avoid such voltage ripple, the sampling loop filter (as introduced in Fig. 8(b)) can be used[98, 99], as shown in Fig. 15(c).

Besides the CP offset current technique, one can also introduce an offset delay into the PFD to avoid the nonlinear region of the PFD/CP I/O characteristics[100, 101], as an example (reported in Ref. [100]) shown in Fig. 15(d).

In summary, all these CP linearization techniques introduced in this sub-section require wider pulse width of CP output current pulse to avoid the nonlinear region on the transfer curve of the PFD/CP. This increases the in-band phase noise induced by the CP, as discussed in Section 3.3. Hence, to mitigate this issue, the input phase error range at the PLL locking state should be reduced so as to reduce the required $\Delta\Phi_{off}$ (see Fig. 15) and the pulse width of CP output current pulse. This is also necessary to reduce the DSM quantization noise, and can be achieved by reducing the division ratio step (see Δ in Fig. 2), as the details presented later in Section 3.7.

3.7. Quantization noise suppression techniques

In this sub-section, an overview of the quantization noise suppression techniques is presented. The existed quantization noise suppression techniques can be categorized into eight types: 1) sub-integer-N divider technique; 2) phase-interpolator (PI) based compensation technique; 3) DTC-based compensation technique; 4) phase-domain quantization noise filtering technique; 5) reference frequency multiplication technique; 6) current-mode digital-to-analog converter (DAC) based compensation technique; 7) finite-impulse-response-embedded (FIR-embedded) noise filtering technique; 8) space-time averaging technique.

As indicated by the quantization noise formula shown in Fig. 2, reducing the quantization step (division ratio step, see Δ in Fig. 2) can effectively lower down the quantization noise. For example, if the quantization step is reduced from 1 to $(1/M)$, the quantization noise is reduced by $20\log(M)$ dB. In addition, as discussed in Section 3.6, reducing Δ is also favorable to reduce the CP-induced in-band phase noise when adopting the CP linearization techniques (see Section 3.6). Hence, to realize this idea, the sub-integer-N frequency divider[56, 80, 91] can be used, as shown in Fig. 16(a). Since the division ratio step is reduced from 1 to 0.5, the quantization noise is reduced by 6 dB. To further reduce the quantization noise, the M-phase phase-interpolator (PI)[102–104], which can adjust its output phase with a step of $(2\pi/M)$, can be used to reduce Δ by M times so as to reduce the quantization noise by $20\log(M)$ dB, as shown in Fig. 16(b). To further reduce Δ to a very fine value, one can replace the PI with a DTC[57] (see Fig. 16(c)), which usually achieves the resolution of sub-1 ps. Since the DTC gain and dynamic range varies with PVT variation, a background calibration block is required to adaptively control the DTC gain. This is achieved by the least-mean-square (LMS) algorithm, as presented in Ref. [57]. The main issue of the PI or DTC is the nonlinearity, which also deteriorates the in-band phase noise and fractional spur, like the PFD/CP nonlinearity. Hence, the PI and DTC should be carefully designed to reduce the nonlinearity as much as possible.

Since the characteristic of the quantization-noise-induced phase noise at the divider output is high-pass, one can directly use an additional PLL[105–106] as the phase-domain low-pass filter to suppress the quantization noise, as shown in Fig. 16(d). However, this approach suffers from the following issues. First, since the additional PLL is inside the main PLL loop, the loop bandwidth of the main PLL should be adequately smaller than the additional PLL. This limits the main PLL loop bandwidth, and thus, may cause limited VCO phase noise suppression. Second, the additional PLL introduces more noise sources and higher power consumption.

The quantization noise formula shown in Fig. 2 also indicates that increasing the operation frequency of DSM can push more quantization noise to higher offset frequency so that the quantization noise can be filtered out by the PLL

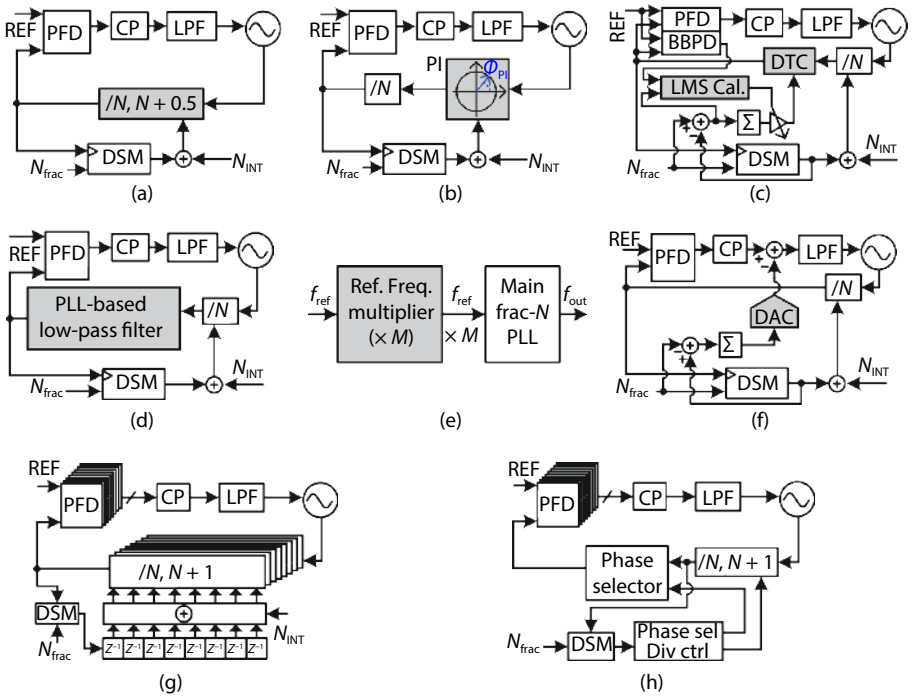


Fig. 16. Quantization noise suppression techniques: (a) sub-integer-N divider technique, (b) phase-interpolator (PI) based compensation technique, (c) DTC-based compensation technique, (d) phase-domain quantization noise filtering technique, (e) reference frequency multiplication technique, (f) current-mode DAC based compensation technique, (g) finite-impulse-response-embedded (FIR-embedded) noise filtering technique, and (h) space-time averaging technique.

loop more readily. Since the DSM operation frequency equals to the reference frequency at the locking state of the PLL, a reference frequency multiplier can be used, as shown in Fig. 16(e). The reference frequency multiplier can be a XOR-gate-based frequency doubler[98, 99], a frequency quadrupler[107], or a multiplying delay-locked loop (MDLL)[108, 109]. A higher reference frequency benefits quantization noise suppression but with the penalty of higher power consumption of the DSM, reference frequency multiplier and PFD.

The quantization noise can also be cancelled by the current-mode digital-to-analog converter (DAC)[8, 11, 110–115], which generates a current pulse with opposite current direction of the CP output current pulse induced by the quantization noise. Suppose the charges of the DAC output and the CP output induced by the quantization noise are Q_{DAC} and Q_{CP}, respectively. In order to effectively cancel the quantization noise, the sum of Q_{DAC} and Q_{CP} should be approximately zero ($Q_{DAC} + Q_{CP} \approx 0$). Hence, the gain of the DAC should be carefully controlled to meet this condition. This can be done by properly selecting the current ratio between the DAC and CP output current. To avoid any mismatch of the ratio between the DAC and CP output current, the LMS-based calibration method can also be used to adaptively control the gain of the DAC[110–112]. Similar to the PI and DTC, the DAC also suffers from the issue of nonlinearity. Hence, the dynamic element matching (DEM) technique is required to improve the DAC linearity[114].

The embedded finite-impulse-response (FIR) noise filtering technique[102, 116–119] can filter out more high-frequency quantization noise without an additional PLL inside the main PLL loop or an additional reference frequency multiplier, as shown in Fig. 16(g). In the PLL with such technique, multiple dividers, PFDs and CPs are adopted. The instantaneous phase error due to the quantization noise generated in each fractional divider is transferred to individual PFD-CP path, and all of the CP outputs are averaged at the loop filter act as the summing unit in FIR filtering[102]. Compared with the DAC-based technique and the PI-based as well as DTC-based technique, this approach does not require additional linear analog circuit block like DAC, PI or DTC. Hence, the circuit linearity and matching performance requirements are relaxed. However, FIR filtering cannot filter the quantization noise at low offset frequency, and multiple dividers are power-hungry.

To mitigate the issues of the embedded FIR noise filtering technique mentioned before, the space-time averaging technique is proposed[120], as the simplified schematic shown in Fig. 16(h). Spatial averaging is achieved by using an array of dividers running in parallel with differential division ratio to obtain an instantaneous fractional division ratio. For example, if M dividers are used, and at least one of the divider's division ratio is $N + 1$ and the division-ratios of the rest dividers is N, the division ratio can varies from $N + 1/M$ to $N + (M - 1)/M$ with a step of $1/M$. To achieve finer fractional division ratio, the DSM is also used, and the quantization noise is reduced by $20\log(M)$. This is similar to the PI-based technique but no additional circuit nonlinearity issue exists. Ref. [120] also proposes a method to reduce the number of the required divider to one by using a phase selector with a controller.

4. Ultra-low-jitter AMS-PLL architectures

As presented in Section 3, there are amount of circuit design techniques to mitigate the design issues of the basic CPPLL introduced in Section 2. However, since the CP-induced in-band phase noise is multiplied by N^2 at the PLL output, it is difficult to further reduce the integrated jitter of the

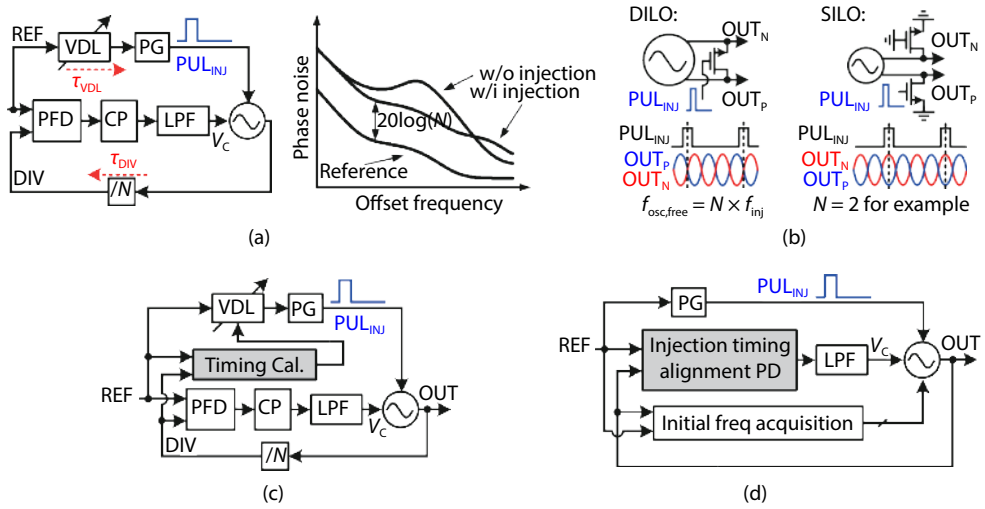


Fig. 17. (Color online) ILPLL: (a) Block diagram of the basic ILPLL and the principle of the phase noise suppression of the ILPLL, (b) schematic of DILO and SILO with their injection timing, (c) ILPLL with injection timing calibration, and (d) conceptual block diagram of the ILPLL with adaptive injection timing alignment techniques.

CPPLL to sub-100-fs with low power consumption, which is required for 5G mm-wave communication[121]. Although a recently reported CPPLL[122] achieves sub-100-fs clock jitter with output frequency range from 7.4 to 14 GHz, it consumes large power with high reference frequency (500 MHz), and an advanced process (16-nm FinFET is used in Ref. [122]) is required to achieve ultra-fast transition edge of divider and PFD so as to reduce the in-band phase noise[122]. To achieve sub-100-fs PLL clock jitter using a cheaper process (e. g. 65-nm or 40-nm CMOS) with low power consumption, other AMS-PLL architectures are proposed, including the injection-locked PLL (ILPLL)[123–147], sub-sampling PLL (SSPLL)[148–183] and sampling PLL (SPLL)[184–192]. In this section, a brief overview of these ultra-low-jitter AMS-PLL architectures is presented.

4.1. Injection-locked PLL

Fig. 17(a) shows the block diagram of the basic ILPLL[123]. In the ILPLL, both the in-band phase noise and the output band phase noise are suppressed by the injecting a clean pulse (see PUL_{INJ} in Fig. 17(a)) to the oscillator[123]. PUL_{INJ} is generated by a pulse generator (PG). So, the phase noise of the ILPLL is almost dictated by the reference clock phase noise. This indicates that the ILPLL can multiply the input clock frequency with almost no jitter degradation. Hence, the noise requirement of the building blocks in the ILPLL can be significantly relaxed. As a result, the ILPLL can generate an output clock with sub-100-fs clock jitter and low power consumption[124, 133–136, 145].

Fig. 17(b) presents two widely used injection-locked oscillator (ILO), including the ILO with direct injection technique (DILO) and the ILO with single-ended injection technique (SILO)[124]. To minimize the phase noise and spur of the ILO, the free running frequency of the ILO ($f_{osc,\ free}$) should equal to the N multiple of the frequency of the injection pulse (f_{inj})[123]. The timing relationship between the outputs of the two ILOs and the injection pulse (PUL_{INJ}) are shown in Fig. 17(b) when $f_{osc,\ free}$ equals to Nf_{inj}. To meet the timing diagram shown in Fig. 17(b), a variable delay line (VDL) is used in the ILPLL to adjust the injection timing, as shown in Fig. 17(a). In the basic ILPLL reported in Ref. [123], the delay of the VDL is manually controlled. This makes the ILPLL performances sensitive to the PVT variation, and the VDL needs to be readjusted if the ILPLL output frequency changes.

To avoid this drawback of the basic ILPLL, Refs. [125, 126] proposed the injection timing calibration method to adjust the VDL automatically before the injection locking is performed. Hence, the process variation can be overcome. However, the foreground calibration method cannot track the voltage and temperature variation. This also makes the ILPLL performance sensitive to environmental variation. To make the ILPLL more robust, the adaptive injection timing alignment techniques are widely used for the ILPLL design[127–147], as the conceptual block diagram of the ILPLL with such techniques shown in Fig. 17(d). The key building block for the adaptive injection timing alignment technique is the injection timing alignment phase detector (PD), which makes the ILPLL meet the timing diagram shown in Fig. 17(b) when the ILPLL is locked. Since the injection timing alignment PD keeps operate when the ILPLL is locked, the injection timing can be aligned adaptively regardless of the PVT variation. An initial frequency acquisition block is used to preset the oscillator free-running frequency $f_{osc,\ free}$ close to the target frequency (Nf_{inj}). The goal of the research on the adaptive injection timing alignment technique is to make the actual timing of the ILPLL as close to the idea timing shown in Fig. 17(b) as possible so as to reduce the spur level with low phase noise and low jitter. Recently, a low spur level of –72 dBc was achieved with low jitter of 140 fs using an injection-locked ring oscillator[142].

4.2. Sub-sampling PLL

Fig. 18(a) shows the simplified block diagram of the integer-N SSPLL[148–169]. According to the analysis presented in Ref. [148], unlike the CPPLL, the CP noise is not multiplied by N^2 at the PLL output. This is the main reason that the SSPLL can achieve a very low in-band phase noise without large CP current so that the SSPLL can generate a clock with sub-100-fs jitter and low power consumption[165–169]. Furthermore, the rejection of N^2 amplification of the in-band phase noise induced by the CP can significantly relax the CP design chal-

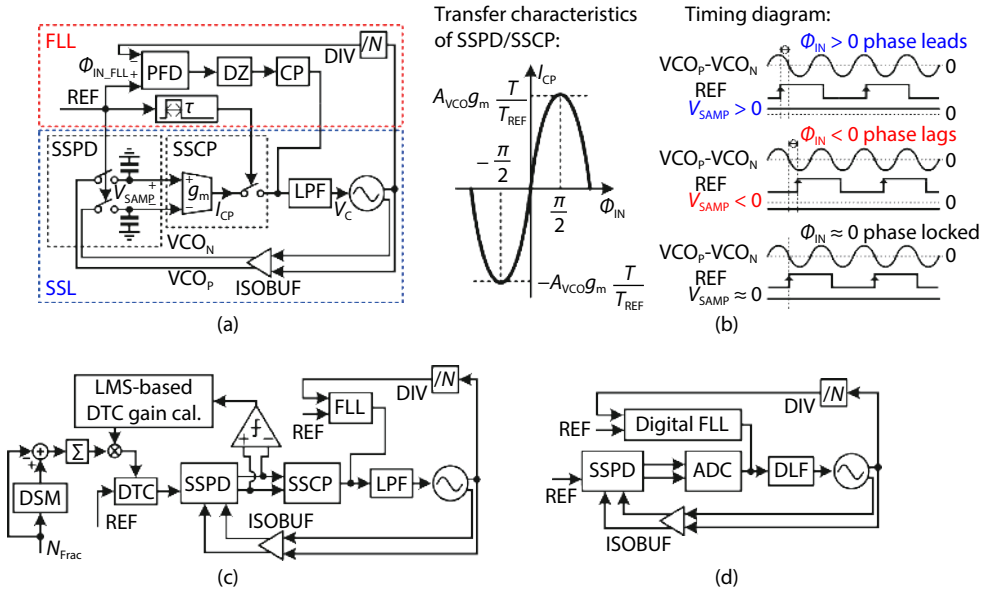


Fig. 18. (Color online) SSPLL: (a) block diagram of the integer-N SSPLL, (b) timing diagram and the transfer characteristics of the SSPD/SSCP, (c) simplified block diagram of the fractional-N SSPLL, and (d) simplified block diagram of the digital SSPLL.

lenges[168]. Hence, a SSPLL with an ultra-low clock jitter of 56.4 fs can be achieved even under a low supply voltage of 0.65 V[167, 168].

As shown in Fig. 18(a), the SSPLL consists of a sub-sampling loop (SSL) and a frequency-locked loop (FLL). The SSL is the main loop and serves as the main function of the SSPLL. In the SSL, the sub-sampling PD (SSPD) and the sub-sampling CP (SSCP) instead of the conventional PFD and CP are adopted. Fig. 18(b) shows the timing diagram and transfer characteristics of the SSPD/SSCP[148]. The buffered VCO differential outputs (VCO_P and VCO_N) are sampled by a low frequency reference clock. The input phase error $|\Phi_{IN}|$ between the reference clock (REF) and the buffered VCO output is transferred to a voltage difference V_{SAMP} (see Fig. 18(b)) first, and then, the SSCP with transconductance of g_m converts V_{SAMP} into a SSCP output current I_{CP} ($I_{CP} = g_m V_{SAMP}$) so as to charge or discharge the LPF to control the VCO frequency and phase. As shown in Fig. 18(b), at the phase locking state of SSL, V_{SAMP} keeps around zero so that I_{CP} keeps around zero and V_C keeps constant.

As shown in Fig. 18(b), the monotonic input range of the SSPD is only $\pm 0.5\pi$ VCO phase. Thus, the SSPD cannot distinguish between Nf_{ref} and other harmonics of f_{Ref}. This may make the SSPLL lock to the wrong frequency. Hence, a FLL (see Fig. 18(a)), which consists of a feedback frequency divider, a PFD with deadzone (DZ) and a conventional CP, is adopted to achieve initial frequency acquisition[148]. When the VCO frequency is close to the target frequency, the input phase error between the reference clock (REF) and the divider feedback clock (DIV) Φ_{IN_FLL} is small enough so that it can fall within the DZ to disable the CP in the FLL. Thus, the SSL can lock to the target frequency without the interference of the FLL[148]. If the SSL loses lock due to some sudden interference, the variations of VCO frequency and phase make Φ_{IN_FLL} fall out of the DZ so that the FLL is enabled automatically to relock the VCO frequency. The isolation buffer (ISOBUF, see Fig. 18(a)) is used to mitigate the interference from the SSPD to the VCO due to the sampling operation so as to reduce the SSPLL spur level[149].

The concept of the SSPLL can also be adopted for the fractional-*N* PLL by using a DTC to modulate the frequency of reference clock[172–179], as shown in Fig. 18(c). Similar to the DTC used in the CPPLL for quantization noise reduction (see section 3.7), the DTC used in the fractional-*N* SSPLL also requires background calibration using a LMS block to avoid large fractional spur[172]. By replacing the CP and analog LPF with an analog-to-digital converter (ADC) and a digital loop filter (DLF), the digital SSPLL[165, 169, 180–183] can be achieved, as shown in Fig. 18(d), which can avoid the non-ideality of the CP and analog LPF such as the leakage. The main design challenge of the digital SSPLL is ADC design, which requires adequate high resolution to make the quantization-induced in-band phase noise be very low and low power consumption to maintain the key advantages of low-jitter and low power of the SSPLL.

4.3. Sampling PLL

Fig. 19(a) shows the simplified diagram of the integer-*N* sampling PLL (SPLL)[184–188]. Compared with the SSPLL, the difference between the SPLL and SSPLL is that the frequency of the sampled clock is equal to the reference frequency at the locking state of the VCO. Hence, the monotonic range of the sampling PD (SPD) is enlarged to $\pm 0.5 T_{REF}$ (T_{REF} is the reference period). Thus, the SPLL is more preferred during the phase/frequency acquisition[190] and more robust over large external disturbance[184] compared to the SSPLL. The SPD gain is controlled by adjusting the slope of the sampled transition edge of the input reference clock V_{ramp} (see Fig. 19(a))[184]. A high SPD gain can be achieved with a high slope of V_{ramp} to achieve lower in-band phase noise than the CPPLL without large CP current. Hence, the SPLL can also achieve sub-100-fs output clock jitter with low power consumption compared with the CPPLL[190, 191]. The main penalty of using SPD instead of SSPD is that the divider noise is still multiplied by N^2 at the PLL output as the in-band phase noise. Hence, the retiming technique introduced in Section 3.3 is also necessary for the SPLL. This makes the SPLL consumes more power than

Table 1. Summary of the features of the AMS-PLL architectures

Architecture	Pros	Cons	Suitable application scenarios
CPPLL	Simple and robust	1. CP-induced in-band phase noise is multiplied by N^2 (N is division ratio) 2. Divider noise contributes in-band phase noise	1. Jitter and PLL power requirements are not stringent 2. Generates low-jitter clock without ultra-low jitter reference clock
ILPLL	Both in-band and outband phase noise are suppressed simultaneously	Large spur induced at large division ratio N	Generates ultra-low-jitter clock with small N and ultra-low-jitter reference clock
SSPLL	1. Ultra-low in-band phase noise 2. No divider-induced phase noise	Narrow PD monotonic input range	Generates high frequency (e. g. > 20 GHz) ultra-low-jitter clock with large N and ultra-low-jitter reference clock
SPLL	1. Ultra-low in-band phase noise 2. Wider PD monotonic input range than that of SSPLL	Divider-induced phase noise still exists	Generates low frequency (e. g. < 10 GHz) ultra-low-jitter clock with large N and ultra-low-jitter reference clock

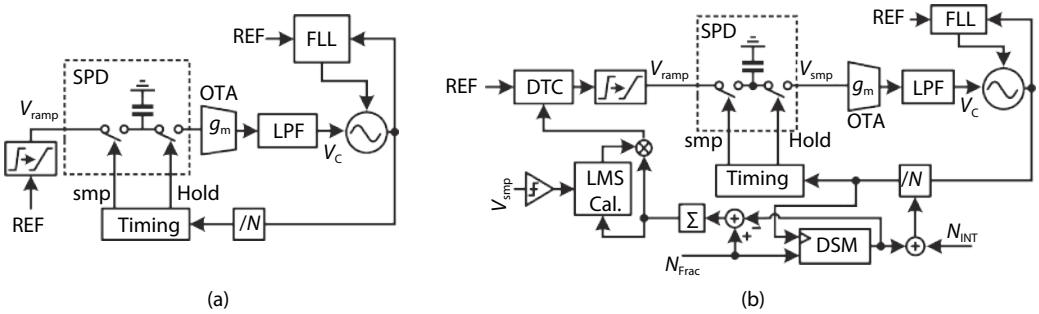


Fig. 19. SPLL: simplified block diagram of (a) the integer-N SPLL and (b) fractional-N SPLL.

the SSPLL, especially in the case of high PLL output frequency.

Fig. 19(b) shows the schematic of the fractional-N SPLL[189–192]. Since the frequency divider is used in the SPLL main loop, a DSM is also adopted like the CPPLL to generate the fractional division ratio. Similar to the CPPLL (see Section 3.7), the DTC is also used to compensate the quantization noise of the DSM, and a LMS block is used to calibrate the DTC gain.

5. Discussion

Since several AMS-PLL architectures are introduced in this paper, it is worthwhile to present a discussion about the consideration of the AMS-PLL architecture selection so as to help designers meet their performance requirements.

Although the ILPLL, SSPLL and SPLL perform better than the CPPLL mainly in terms of jitter and power, the CPPLL architecture is still recommended to be adopted for most of the applications if the required jitter and power are not simultaneously very low. The reasons are as follows. First, as presented in Section 2, the monotonic range of the input phase difference of the PFD is from -2π to 2π. This makes the CPPLL be more robust to maintain its lock state over any disturbance, compared to the other AMS-PLL architectures. Second, the CP current of the CPPLL is less sensitive to the PVT variation compared to the PD gains of the SSPLL and SPLL. Last, the main drawback of the ILPLL is the poor spur level and limited phase noise suppression in the case of large division ratio[123] or high output frequency[139]. This limits the scope the application of the ILPLL.

If an ultra-low-jitter (e. g < 100 fs) clock is required, there are two different scenarios needs to be considered.

In the first scenarios, if the jitter of the reference clock is not adequately low, the CPPLL is still more preferable compared to the other AMS-PLL architectures introduced in this paper. The reason is as follows. As presented in Section 4, the main advantage of the ILPLL, SSPLL and SPLL is the low in-band phase noise. This is true only when the reference clock jitter is adequately low because the NTFs of the reference clock phase noise of all the PLL architectures are low-pass. Furthermore, as discussed before, the CPPLL is more robust. Hence, with a noisy reference clock, the CPPLL is more suitable and robust than the other AMS-PLL architectures to generate a low-jitter clock by setting a narrow loop bandwidth and designing a low-phase-noise VCO.

In the second scenario, if an ultra-low-jitter reference clock is available, the ILPLL, SSPLL and SPLL architectures are more suitable than the CPPLL to generate an ultra-low-jitter clock with low power consumption. If a small multiplication factor is required, the ILPLL is a good choice because both the in-band and out-band phase noise are suppressed simultaneously by injection locking with an acceptable spur level. This significantly relaxes the noise requirement of each PLL building blocks. With a large multiplication factor, the SSPLL and SPLL are more preferable due to their lower spur levels than that of the ILPLL. If the PLL output frequency is not very high (e. g. <10 GHz), the SPLL is more suitable because of the wider monotonic input range of SPD compared to that of the SSPD. However, at a higher frequency (e. g. > 20 GHz), it is challenging to design a low-noise and low-power divider chain, which is necessary for an ultra-low-jitter SPLL. Hence, the SSPLL becomes more suitable to generate an ultra-low-jitter clock at a higher frequency.

The discussions presented above are summarized in Table 1.

6. Conclusion

In this paper, an overview of the AMS-PLL is presented, in-

cluding a brief introduction of the basics of the charge-pump based PLL (CPPLL), a summary of the design issues of the basic CPPLL architecture, a systematic introduction of the techniques for the performance enhancement of the CPPLL, and a brief overview of ultra-low-jitter AMS-PLL architectures (including ILPLL, SSPLL and SPLL), which can achieve lower jitter (< 100 fs) and lower power consumption compared with the CPPLL. Finally, a discussion about the consideration of the AMS-PLL architecture selection is also given, which could help designers meet their performance requirements.

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