REVIEWS

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Silicon-based FMCW signal generators: A review

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Abstract: FMCW radars with high resolution necessities the generation of highly linear, low phase noise, and low spur chirp signals with large bandwidth and a short modulation period. This paper reviews recent research progress on silicon-based FMCW signal generators, identifies advances in architecture, fundamental design, performance analysis, and applications of the FMCW synthesizer.

Key words: slicon; FMCW; PLLs; radars; wireless; two-point modulation; fast chirp; digital pre-distortion

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1. Introduction

Frequency-modulated continuous-wave (FMCW) signal sources in the form of a sinusoid signal with time-varying frequencies are widely adopted in ranging, communication, and imaging applications. For example, the FMCW signal can be utilized to determine the round-trip propagation delay by detecting the frequency difference between the transmitted and returned signals, which is widely used in FMCW radars.

Historically, FMCW radar sensors were built using discrete components and III–V technologies such as gallium arsenide (GaAs). However, they suffer from high production cost, poor integration, a low yield, which makes them inefficient and uneconomic for adopting in high volume and low-cost radar system. Recent advances in silicon germanium (SiGe) and complementary metal oxide semiconductor (CMOS) technologies significantly reduce fabrication cost making silicon-based radar sensor available for high-volume marker[1–10]. Particularly, the high cutoff frequency of transistors in modern scald CMOS technologies allows integration of the radar transceiver together with a comprehensive digital core for the digital signal processing.

This paper reviews the literature on silicon-based FMCW signal generators, identify advances in performance analysis, steps in the evolution of the FMCW signal source architecture including one-point modulation scheme and two-point modulation scheme. Digital pre-distortion for FMCW PLL is also discussed. This paper is organized as follows. Section 2 introduces performance analysis of the FMCW signal generators. Various FMCW signal source architectures are discussed in Section 3. Section 4 briefly lists key challenging that remain to be solved. Conclusion is summarized in Section 5.

2. Performance analysis of FMCW signal generators

Fig. 1 shows the simplified block diagram of an FMCW radar transceiver. An FMCW signal source generates a signal whose frequency increases and/or decreases linearly over time as $f(t) = f_0 + \mathrm{SL} \cdot t$, where f_0 is the carrier frequency and SL is the slope of the chirp signal. A radar transmitter amplifies the FMCW signal and radiates the signal through a TX antenna. Then, the radiated signal hits the target which is located at the distance R from the radar transceiver and a portion of the signal are reflected back to the radar transceiver. The received signal is amplified and mixed with a local oscillator which is generated from the same FMCW signal source. The delay between the transmitted signal and the reflected signal is known by calculating the frequency difference, which can be used to determine the position of the target object. For a moving target, the Doppler frequency will be included in the frequency difference, thus the system can get the relative speed of the target, as shown in Fig. 2. For triangular waves, the relationship between the beat frequency and the target distance and speed is shown as follows[11]:

$$f_{\mathrm{b1,2}} = \pm\frac{2\mathrm{BW_C}}{T_\mathrm{C}C}\cdot R + \frac{2f_\mathrm{C}}{C}\cdot v, \tag{1}$$

where $\mathrm{BW_C}$ is the bandwidth of the chirp, T_C is the duration of the chirp, f_C is the center operating frequency, $f_{\mathrm{b1,2}}$ is a pair of beat frequencies of the rising and falling segments, and v is the velocity of the target object.

Different radar applications have difference requirement for the radar function including range, range resolution, maximum detectable speed, and speed resolution. In the case of short-range radars, chirp bandwidth of several gigahertz is needed to obtain range resolution Δr better than 5 cm. For long-range detection, a short duration period is needed to detect the high-speed target since the maximum unambiguous speed v_{max} is inversely proportional to chirp period. In addition, a fast chirp pushed the intermediate frequency (f_{IF}) of the reflection signal away from the $1/f$ noise corner, thereby improving signal-to-noise ratio (SNR) which is critical to CMOS radar system on chip. Fast-chirp signal is also beneficial for distinguish a small target with a low radar cross section (RCS) from a near-by high RCS target. This is because fre-

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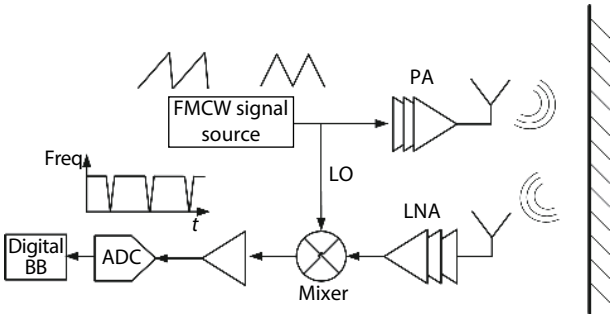

Fig. 1. Block diagram of the FMCW transceiver.

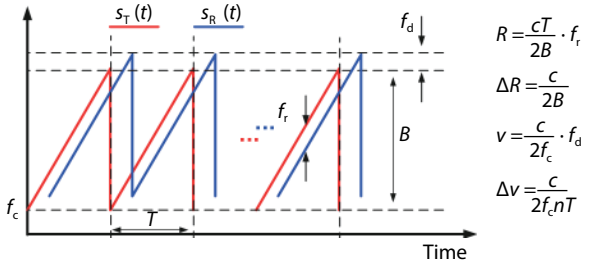

Fig. 2. (Color online) FMCW principle of a sawtooth wave.

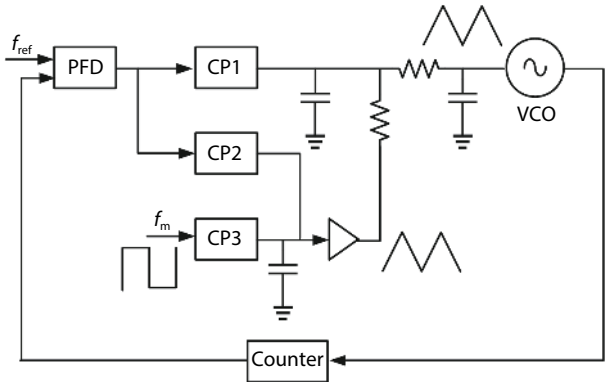

Fig. 3. FMCW PLL using direct-modulating VCO.

quency distance between the targets is spread wider with a faster chirp signal, which contributes to relaxing the phase noise requirement.

3. FMCW signal generators architecture

Various methods for FMCW signal generation have been reported so far, each with its own advantages and disadvantages. The most intuitive method is to adopt a VCO in an open loop and the compensation of nonlinearity is achieved by using a look-up table (LUT) and digital-to-analog converter (DAC). While the frequency drift over supply voltage or temperature variations may be compensated by periodical updating of the LUT, the unexpected disturbances and load variations cannot be compensated effectively thereby leading to insufficient frequency modulation accuracy. In order to overcome the issues of open-loop approaches, FMCW modulators are usually implemented with fractional-*N* phased-locked loops (PLLs) as follows.

3.1. FMCW PLL with one-point modulation scheme

In PLL-based FMCW modulator, the output frequency can be modulated by imposing the control voltage of a VCO[12–15]. Fig. 3 shows the block diagram of the FMCW PLL using direct-modulating VCO. This method has the advantages

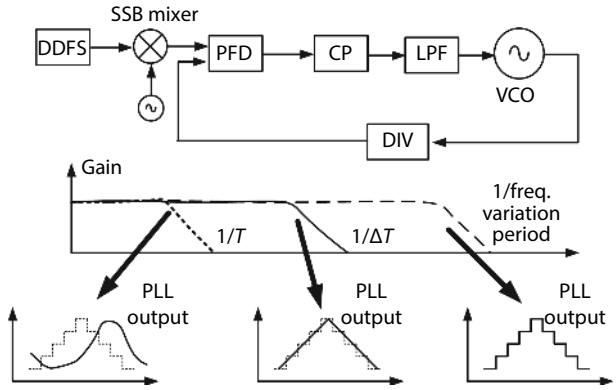

Fig. 4. Block diagram of DDFS-based FMCW generator.

of a simple circuit structure and the absence of additional noise sources originating from delta–sigma modulators and DACs. However, the loop bandwidth of a PLL has to be much less than the modulation frequency in order to allow the VCO frequency variations. Typically, the required loop bandwidth is about one of ten times smaller than that in the modulation. Assuming the modulation frequency of 30–50 kHz, the loop bandwidth of the PLL is around 3 to 5 kHz, which leads to a large capacitor if more than 10 nF in the loop filter in the case of the analog PLL implementation.

As depicted in Fig. 4, PLL-based FMCW modulation can be achieved by modulation the reference frequency of an integer-*N* PLL, which is known as direct digital frequency synthesis (DDFS)[16, 17]. The frequency chirp of the reference signal has discrete stair-like shape, which is converted to the time-domain voltage variations at the output node of the PLL charge pump. The low-pass filter can smooth the stair-like voltage variations and generates the non-stair-like voltage which is supplied to the VCO. As a result, the PLL output frequency is smoothed into linear chirp. However, this method suffers from considerable area and power penalties, since high resolution DACs and large read-only-memory (ROM) tables may be needed to achieve fine and linear frequency tuning. The cut-off frequency of the PLL transfer function, f_{PLL}, should be much higher than the modulation frequency, $1/T$, in order to generate a tri-angle shape of the FMCW signal. On the other hand, f_{PLL} should be lower than the refresh rate of the DDFS, $1/\Delta t$, in order to suppress the spurs at $1/\Delta t$ that cause sinusoidal nonlinear frequency chiro at the output. In order to relax the requirement of clock frequency and frequency control word length of the DDFS, the reference frequency is generated from a single-sideband and a crystal oscillator in Ref. [16].

Frequency modulation can be achieved by varying the feedback frequency divider ratio in a fractional-*N* PLL[18–25], as shown in Fig. 5. This method does not necessities a low noise DAC nor a large LUT and it provides a highly linear frequency chirp. The power consumption of this architecture can be significantly lower than FMCW PLL using DDFS. As the phase-modulation signal is low-pass filtered by the loop filter, the shortest possible chirp time is typically longer than 100 μs. Moreover, narrow loop bandwidth is necessary in conventional fractional-*N* PLL based FMCW signal generator in order to suppress the quantization from the delta-sigma modulator, which degrades the linearity of fast chirps. In addition, the typical charge pump-based fractional-*N* PLL

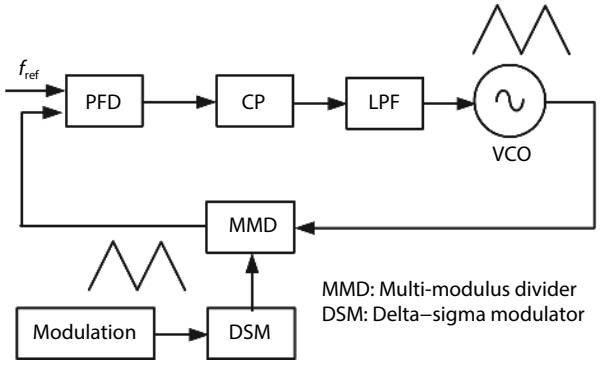

Fig. 5. Block diagram of the FMCW PLL using feedback modulation.

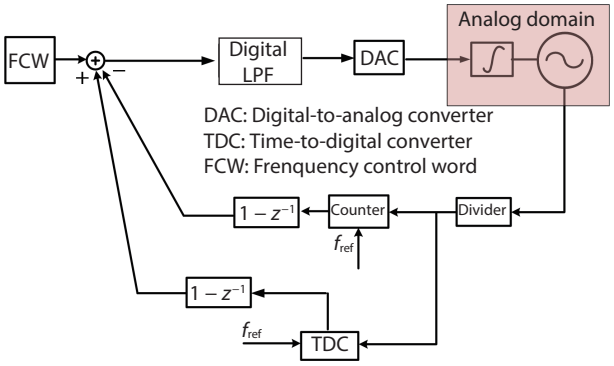

Fig. 6. (Color online) Block diagram of the FMCW PLL using digital modulation.

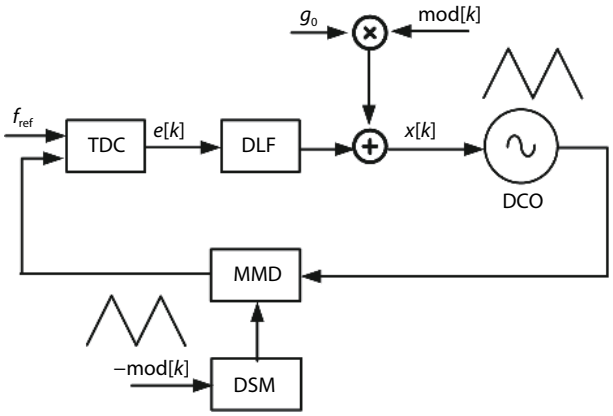

Fig. 7. Block diagram of the digital PLL based FMCW signal generator using TPM.

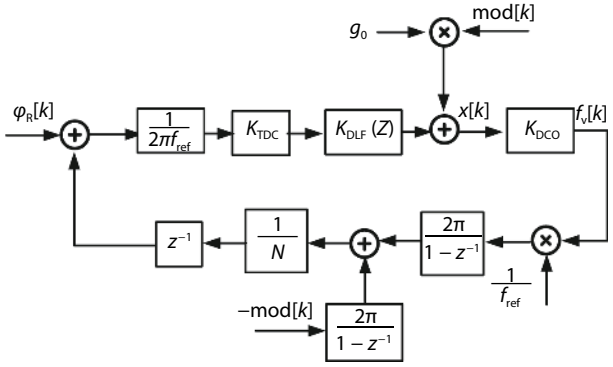

Fig. 8. Simplified linear model of the digital PLL based FMCW signal generator.

cannot be fully integrated on silicon at low cost due to the passive loop filter.

Alternatively, a digital modulation technique used in a phase-domain digital PLL architecture is proposed in Refs. [11, 26, 27]. As shown in Fig. 6, phase of the divided VCO output is captured and digitalized by a digital phase detector and the quantized phase is converted to the frequency by a digital differentiator. The frequency is compared with a triangular frequency control word (FCW) and the difference between the two values is further processed by a digital loop filter. Without adopting a programmable frequency divider, the mixed-mode PLL avoids the undesired phase noise degradation due to the quantization noise from the delta-sigma modulator. However, the integrator, VCO, and DAC still operate in analog domain which is not scaled easily to future CMOS technology nodes.

All above-mentioned FMCW signal generator based on indirect VCO modulation is limited by the loop bandwidth of the PLL. For triangular modulation with a 100-μs period, the PLL bandwidth has to be larger than 1 MHz in order to let the first 100 harmonics pass through the loop filter, which is necessary to achieve 0.01% sweep linearity. Therefore, the PLL loop bandwidth, which is needed to handle the fast FMCW modulation, could be higher than that desired for an optimum phase noise of the PLL.

3.2. FMCW PLL with two-point modulation scheme

Two-point modulation (TPM) technique can be used to decouple the modulation bandwidth from the PLL loop bandwidth by injecting the modulation signal into both the tuning port of the VCO (or DCO) and the feedback path[28–30]. Fig. 7 shows the block diagram of a digital FMCW PLL with TPM scheme. While the modulation signal mod[k] is sample at the reference rate and directly modulates the tuning port of the DCO, -mod[k] is injected into the feedback to changes the division ratio of the divider. Fig. 8 shows the simplified linear model of the digital PLL-based TPM FMCW signal generator. The signal $\varphi_r[k]$, $\varphi_d[k]$ and $\varphi_v[k]$ represents the variable phase of the reference, divided and output clocks respectively. The PLL loop gain can be written as

$$G_{loop}(z) = K_{TDC} \cdot K_{DCO} \cdot H_{DLF}(z) \cdot \frac{z^{-1}}{1-z^{-1}} \cdot \frac{1}{Nf_{ref}^2}, \quad (2)$$

where K_{TDC} is the TDC gain, K_{DCO} is the DCO gain, $H_{DLF}(z)$ is the transfer function of the loop filter, N is the feedback division ratio, and f_{ref} is the reference frequency.

The z-transforms of the time-domain signal mod[k] and the output frequency variation $\Delta f_v[k]$ can be denoted as mod[z] and $\Delta f_v[n]$, respectively. The transfer function from mod[z] to $\Delta f_v[n]$ is given as

$$H_{LP}(z) = f_{ref} \cdot \frac{G_{loop}(z)}{1+G_{loop}(z)}. \quad (3)$$

Similarly, the transfer from the injection point at the DLF output is given as

$$H_{HP}(z) = g_0 \cdot \frac{K_{DCO}}{1+G_{loop}(z)}. \quad (4)$$

Then the transfer function of TPM can be obtained by summing Eqs. (2) and (3) as

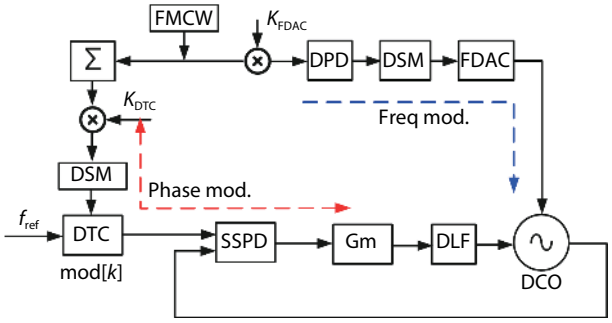

Fig. 9. (Color online) Block diagram of SSPLL based FMCW signal generator.

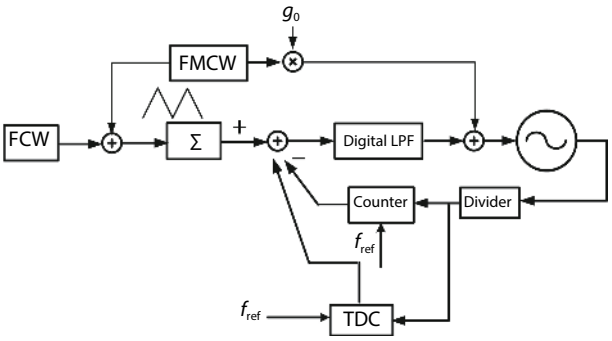

Fig. 10. Block diagram of phase domain digital PLL based FMCW signal generator.

$$H_{TPM}(z) = f_{ref} \cdot \left[\frac{G_{loop}(z)}{1 + G_{loop}(z)} + \frac{g_0 K_{DCO} \cdot (1/f_{ref})}{1 + G_{loop}(z)} \right]. \quad (5)$$

It can be seen from Eq. (4) that $H_{TPM}(z)$ is an all-pass transfer function if the value of the gain g_0 is exactly equal to f_{ref}/K_{DCO}.

Fig. 9 shows the simplified block diagram of analog PLL with TPM scheme[29, 31]. The prototype is designed with an analog sub-sampling PLL[32, 33] which relies on the alignment of the VCO zero-crossing moment with the reference clock edge to sampling the instantaneous PLL output phase error. For the fractional-*N* operation, the reference clock needs to be delayed by a digital-to-time converter (DTC) in order to realign with the VCO zero crossing point, which compensates the accumulated fractional phase residue. In addition, the extra phase shift is added to the DTC to accommodate the FM modulation of the VCO. The FMCW PLL presented in Ref. [29] achieves a 1.5 GHz chirp bandwidth with a fast slope under 10 μs at 16-GHz carrier.

TPM architecture also can be applied to phase-domain digital PLL[34]. Fig. 10 shows the simplified block diagram of the phase-domain digital PLL with TPM. One data path directly modulates a DCO which has a high pass characteristic. The other path compensates the frequency difference and prevents the modulating data from affecting the phase error which has a low pass characteristic. When both paths are combined without any delay mismatch in ideal case, an all-pass transfer function is realized and the maximum triangle modulation frequency is not limited by the PLL loop bandwidth.

While the TPM provides an all-pass characteristic allowing fast chirp generation, it is sensitive to gain mismatch between the high-pass and low-pass modulation path. As plotted in Fig. 11, the gain of the feedforward path becomes higher if the gain of the VCO gets higher due to environment variations. As a result, the PLL will try to correct the gain mismatch since PLL seems to be in the unlock condition.

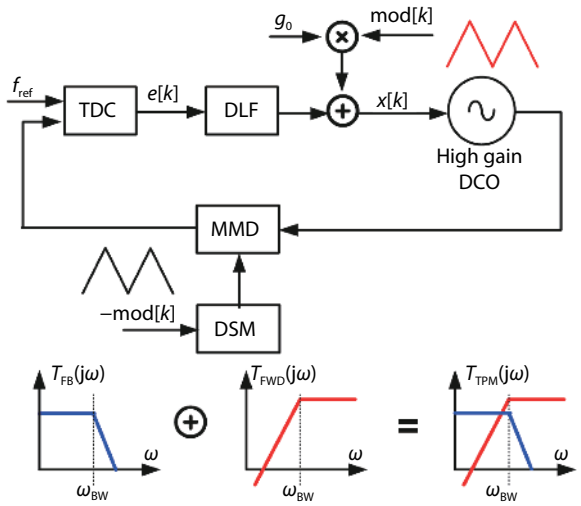

Fig. 11. (Color online) Block diagram of the TPM digital PLL with gain mismatch.

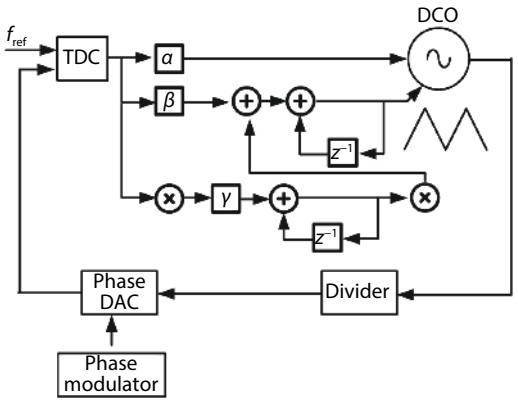

Fig. 12. Block diagram of the FMCW signal generator using a type-III frequency ramp estimator.

In order to avoid additional gain and timing calibration for the feedforward modulation path, a type-III third-order chirp frequency synthesizer PLL architecture is proposed and presented in Ref. [35]. As shown in Fig. 12, the proposed FMCW PLL is consisting of a second-order DLF using frequency ramp estimator, a linear TDC with constant-gain, a DCO, a divider, a phase DAC and a phase modulator. The key point to achieve the gain self-tracking of the feedforward modulation path is the second-order loop filter that drives the slope of the output frequency ramp to track the slope of the target frequency ramp by the negative feedback. In other words, this architecture utilizes the loop filter output to calibrate the gain of the feedforward modulation path in reference to the gain of feedback modulation path. As a result, the gain self-tracking is operating in background with respect to the environment variations. Authors in Ref. [36] presents a mixed-mode PLL with the same type-III frequency ramp estimator based on bang-bang phase detector. A 1-bit third-order single-loop modulator, combining with the hybrid finite-impulse-response filtering technique, significantly suppresses the BBPD induced quantization noise. In addition, two infiniteimpulse-response (IIR) filtering stages is cascades with the second-or-

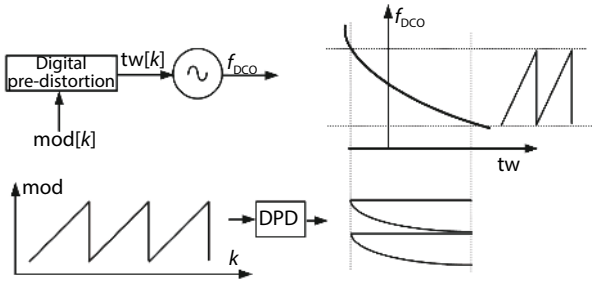

Fig. 13. The concept of DCO pre-distortion scheme.

der DLF in order to smoothen the generated chirp waveform by reducing the instant variation of the DLF's output.

3.3. Adaptive digital pre-distortion

It is known that the DCO gain K_{DCO} is not only sensitivity over process, temperature, voltage variations, and aging, but also depending on the oscillator output frequency due to the DCO frequency nonlinearity characteristic. Practical DCOs may demonstrate a random or periodic nonlinearity due to unavoidable mismatch within digitally-controlled capacitor array, in addition to the intrinsic $1/\sqrt{LC}$ nonlinearity. In order to make sure the coefficient g_0 is always equal to f_{ref}/K_{DCO}, the TPM scheme requires an accurate estimation of the coefficient g_0. Assuming the DCO gain is altered by a relative gain error ϵ_K, which is $\hat{K}_{DCO} = K_{DCO}(1+\epsilon_K)$, the resulting error between ideal and actual frequency can be written as[28]

$$\Delta_{chirp}(z) = \mathrm{mod}(z)\cdot[f_{ref} - H_{TPM}(z)] = \frac{\epsilon_K}{1+\epsilon_K}\cdot f_{ref}\cdot \mathrm{mod}(z)\cdot\frac{1}{1+G_{loop}(z)}. \quad (6)$$

It can be seen from Eq. (6) that spectrum of the chirp frequency error is determined by the spectrum of the modulation signal after high-pass shaping. The dominate pole of the high-pass filtering function is located at the closed-loop bandwidth of the PLL, which indicates that the PLL can reject chirp error introduced by the oscillator gain error to some extent if the modulation speed is slow. However, if the modulation speed is fast with respect to the bandwidth of the closed loop, a portion of the spectrum of mod[k] is beyond the PLL bandwidth, the feedback loop cannot detect the chirp error which propagates to the output thereby causing chirp distortion.

In general, DCO tuning nonlinearity can be compensated by using an adaptive pre-distortion method. The simplified concept of DCO pre-distortion is depicted in Fig. 13. Assuming that a nonlinear function links the DCO tuning word, tw[k] to the DCO output frequency f_{DCO}, the DCO pre-distortion is expected to estimate the inverse of the function and use it to remap the modulation signal mod[k] ti to the tuning work tw[k]. A common approach is to implement pre-distortion in the digital domain by utilizing a loop-up table (LUT) or polynomial correction. Authors in Ref. [34] use a 24 kbit SRAM LUT to store the pre-distortion coefficients during initial calibration phase at power-up. The entire DCO gain calibration takes 4 s. However, the pre-distortion coefficient is generated in foreground only, which is less reliable over voltage and temperature variations.

An ideal digital pre-distortion (DPD) for an N-bit DCO requires a LUT with 2^N fields. While this kind of hardware complexity is acceptable for the foreground DPD implementation, the hardware complexity increases considerably if the background calibration is necessary. This is because an LMS-based implementation requires an accumulator and a multiplexer for every LUT field. In order to overcome this issue, a piecewise-linear DPD is proposed to make an adaptive implementation feasible. In the case of the PLLs, the adaptive DPD was first demonstrated in Ref. [37] with the purpose of linearizing the characteristic of the digital-to-time converter (DTC), and later successfully applied to pre-distort the DCO tuning curve[38] and time-to-digital converter nonlinearity[39]. The general concept of the piecewise linear DPD is to approximate the inverse characteristic of the nonlinear block with a piecewise linear curve. Only a subset of the points of the inverse characteristic is estimated and these points are linearly interpolated to get the entire characteristic.

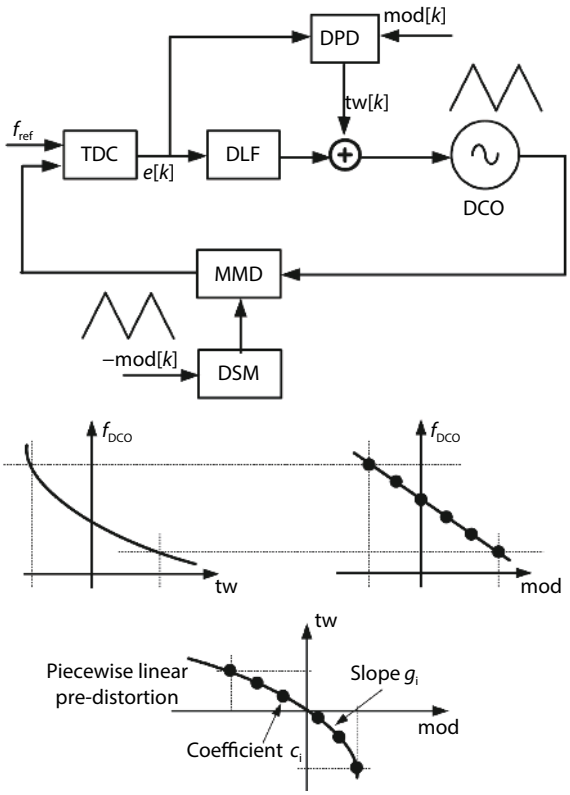

Fig. 14. Block diagram of the TPM digital PLL with digital pre-distortion.

Fig. 14 shows simplified block diagram of the adaptive piecewise linear DPD and the concept diagram, of a piece wise-linear DPD. It can be seen that the modulation signal mod[k] is pre-distorted at the high-pass injection path before being applied to the digital PLL with TPM scheme. Any mismatch between the two-injection path appears as a phase error at the input of the TDC. The output of the TDC $e[k]$ can be adopted to adapt the DPD characteristic.

Fig. 15 shows the piecewise-linear DPD scheme report in Ref. [40]. Only two section of piecewise linear characteristic are plotted for simplicity. The modulation signal mod[k] is quantized coarsely into a three-level word $Q_c[k]$ which is correlated with the output of the TDC. Thus, the average correction, which is needed in each of the three regions of mod[k], is estimated. The slopes, g_o and g_1, of the piecewise linear curve in Fig. 15 can be simply obtained by the difference of the c_i coefficients. However, the LMS loop, which is used to es-

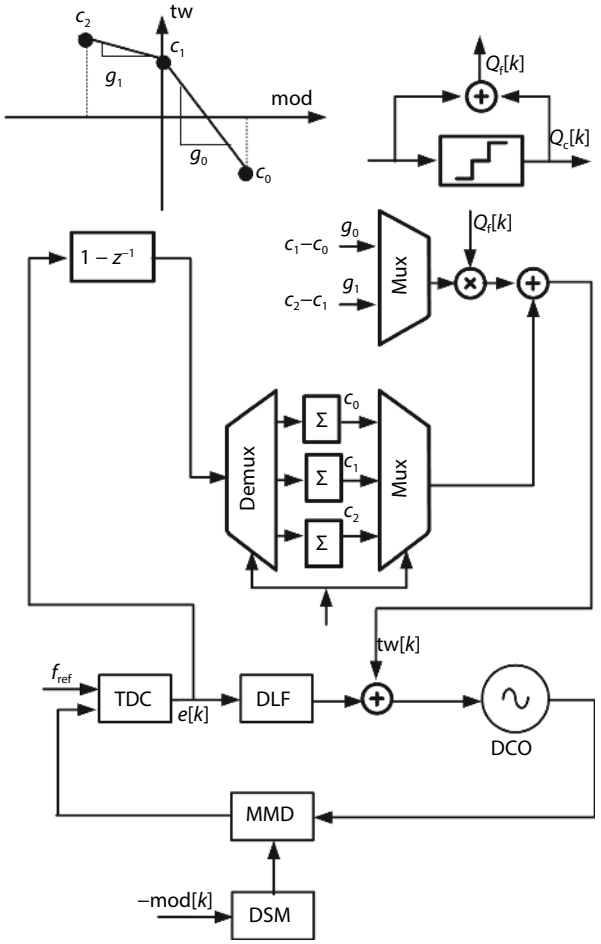

Fig. 15. Adaptive piecewise-linear DPD in Ref. [40].

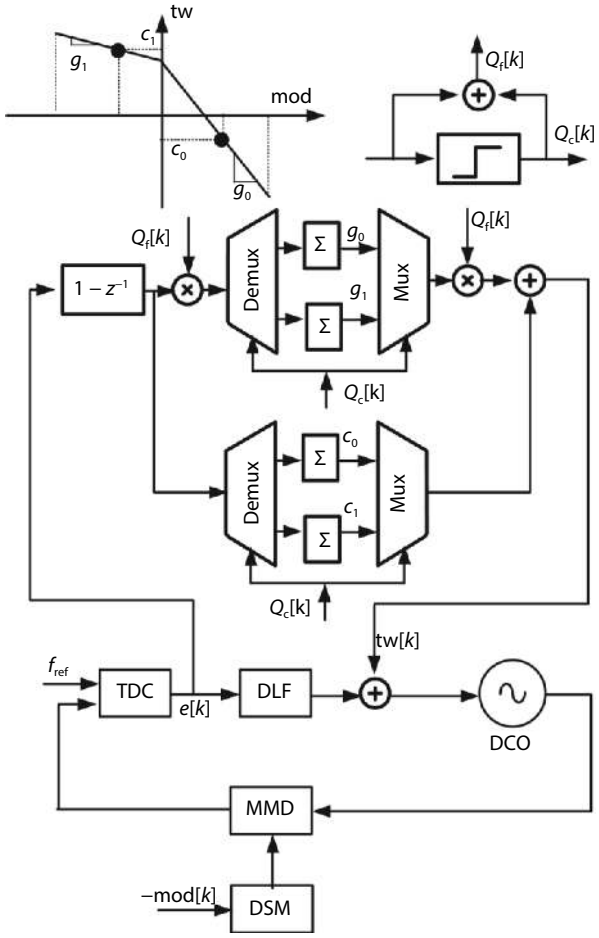

Fig. 16. Adaptive piecewise-linear DPD in Ref. [28].

timate c_i, may interact with each other through the calculation of the slopes g_i. In order to avoid this issue, the slopes g_i have to calculated and used after the estimation of c_i is settled, which slows down the coefficient convergence and may introduce instability in some cases. Authors in Ref. [28] introduce a solution that can decouple the estimation of the c_i coefficients from that of the g_i coefficients, as shown in Fig. 16. While the number of LMS loops is almost doubled, the c_i coefficients no longer interact with each other and the LMS loop can operate in background properly.

4. Key challenges

While different FMCW radar applications require various configuration and different noise levels, in general, reducing the chirp period would be one of the key factors to improve the overall radar performance. Generation of fast chirps allows improvement of velocity resolution, pushing the beat frequency beyond the flicker noise corner, improving the system SNR by averaging the detected signal, and increasing the maximum unambiguous velocity. Wider modulation bandwidth contributes to improve the range resolution and phase noise level thereby improve the SNR. Table 1 summarizes the existing FMCW signal sources with the state-of-the-art CMOS and BiCMOS implementation.

If fast chirp generation is not required for a given application, the FMCW PLL architecture with one-point modulation scheme can be adopted. Compared to the FMCW PLL using direct-modulation VCO and DDFS-based FMCW generator, the FMCW PLL using feedback path modulation or its digital equivalent has the advantages of simpler topology and circuit implementation. If fast chirp generation is necessary for a given application, the FMCW PLL architecture with TPM scheme has to be used. The all-pass transfer function can be provided by the TPM and the maximum chirp rate is no longer limited by the PLL loop bandwidth. However, typical TPM FMCW PLLs require non-trivial gain calibration thereby increasing the overall complexity. The type-III FMCW PLL with TPM scheme can avoid the gain calibration since it can track frequency ramp with a zero steady-state phase error providing self-aligned gain between the high-pass and low-pass modulation path. Nevertheless, there may be potential stability issue in the type-III FMCW PLL. In addition, the achievable chirp rate is limited by the gain of the extra integral path, which is introduced by the type-III PLL. It can be seen from the above discussions that existing type-II FMCW PLLs with the TPM scheme and type-III FMCW PLLs with the self-adapted TPM scheme have their own advantages and disadvantages. As for future research directions on FMCW signal sources, it would be meaningful to investigate the possibility of achieving wider chirp bandwidth and faster chirp rate with minimized RMS and peak frequency error. It is also necessary to study the stability issues on various types of type III (or even higher-order) FMCW PLLs. New architectures, circuit design techniques, digital compensating methods and basic theory analysis on FMCW signal sources are inevitably required for future advanced radar applications.

Table 1. Performance summary of the state-of-the-art work.

Ref.	Topology	Ref. Freq. (MHz)	Freq. (GHz)	BW/T_{chirp} (GHz/μs)	Rms FM_{err} (kHz)	Max slope (GHz/μs)	Norm. slope (GHz/μs)	Phase noise[1] (dBc/Hz)	Waveform	Power (mW)	Tech.
[28]	TPM	52	22	0.2/1.2	800	0.16	0.66	−97	Sawtooth triangular	20	65 nm CMOS
[29]	TPM	80	16	1.5/10	230	0.15	0.75	−92.4	Sawtooth triangular	44	28 nm CMOS
[2]	TPM	1000[2]	20	1/40	600	0.025	0.1	−94	Sawtooth triangular	>120	40 nm CMOS
[35]	TPM	276.8	9	0.95/80	1900	0.019	0.17	−86.2	Triangular	14.8	65 nm CMOS
[34]	TPM	40	60	1/210	384	0.47	0.06	−88	Triangular	48	65 nm CMOS
[41]	Frac-*N*	125	20	1.25/50	800	0.025	0.1	−97	Sawtooth triangular	240	130 nm SiGe

[1]Normalized to 79 GHz. [2]A clean-up PLL is required to generate the 1 GHz reference clock for FMCW synthesizer.

5. Conclusion

During the past few years silicon-based FMCW signal source attracted a lot research interest both from academia and industry. Promising performance in terms of modulation bandwidth, modulation period, phase noise level, and frequency error has been achieved from sub-10 GHz range to mm-wave and terahertz frequency range. Key challenging that remain are the realization of wider modulation bandwidth and shorter period FMCW signal source at acceptable power consumption in deep scaled CMOS technology.

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