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4H-SiC trench MOSFET with an integrated Schottky barrier diode and L-shaped P+ shielding region

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Abstract: A novel 4H-SiC trench MOSFET is presented and investigated by simulation in this paper. The device features an integrated Schottky barrier diode and an L-shaped P+ shielding region beneath the gate trench and aside one wall of the gate trench (S-TMOS). The integrated Schottky barrier diode works as a free-wheeling diode in reverse recovery and reverse conduction, which significantly reduces reverse recovery charge (Q_{rr}) and reverse turn-on voltage (V_F). The L-shaped P+ region effectively shields the coupling of gate and drain, resulting in a lower gate–drain capacitance (C_{gd}) and date–drain charge (Q_{gd}). Compared with that of conventional SiC trench MOSFET (C-TMOS), the V_F and Q_{rr} of S-TMOS has reduced by 44% and 75%, respectively, with almost the same forward output current and reverse breakdown voltage. Moreover, the S-TMOS reduces Q_{gd} and C_{gd} by 32% and 22%, respectively, in comparison with C-TMOS.

Key words: SiC; MOSFET; Schottky barrier diode; reverse recovery; gate-drain charge

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1. Introduction

SiC MOSFET, as one of the most promising power switch devices, has replaced part of Si counterpart in many applications. In a common bridge rectifier circuit, SiC MOSFET is usually anti-paralleled with an external SiC Schottky barrier diode (SBD) as a free-wheeling diode (FWD), due to the bipolar degradation of the intrinsic body diode[1–4]. However, external SBD inevitably introduces extra package cost and stray inductance, resulting in worse switching performance. Therefore, it is highly desired to integrate a SiC SBD into SiC MOSFET to improve the third quadrant performance[5]. In addition, the gate–drain capacitance (C_{gd}) and gate–drain charge (Q_{gd}) are extremely critical factors that influence the switching performance of MOSFET. A lot of work has been done to reduce C_{gd} and Q_{gd}[6–11]. Furthermore, Infineon has proposed a CoolSiC™ MOSFET with an asymmetric concept, which achieves excellent reliability and static characteristics[12].

In this paper, we propose a novel SiC trench MOSFET with an integrated SBD and L-shaped P+ shielding region (S-TMOS). This device achieves excellent third quadrant performance with low C_{gd} and Q_{gd} values. Moreover, the static and dynamic characteristics of the S-TMOS and conventional SiC trench MOSFET (C-TMOS) are compared in detail.

2. Device structure and mechanism

Schematic cross sections of the S-TMOS and C-TMOS are presented in Fig. 1. The main parameters of the two structures are given. Since the Schottky contact occupies a part of cell area, an excessive L_s leads to a large area and $R_{on,sp}$. Moreover, if L_s is too large, then the protection effect of the P+ shielding region on Schottky contact will be weakened and thus the leakage current may increase. In contrast, if L_s is too small, then the reverse conduction and reverse recovery performances of S-TMOS will degrade. The grounded P+ shielding region exists both beneath the gate trench and aside one side wall of the gate trench in S-TMOS. The S-TMOS has lower C_{gd} and Q_{gd} than C-TMOS because the L-shaped P+ region shields the coupling of gate and drain more effectively. Meanwhile, the SBD is located next to the P+ shielding region so that the highly doped P+ region can absorb electric field lines from drain and reduce the surface electric field of the Schottky contact. The static and dynamic characteristics of S-TMOS and C-TMOS have been investigated by numerical TCAD simulations. The thickness of gate oxide is 50 nm and the channel mobility is set to be 20 cm^2/(V·s). In order to form a favorable Schottky contact, nickel (Ni) is selected as the Schottky metal. The workfunction of Ni is between 5.04 and 5.35 eV[13], so the workfunction of the Schottky metal is set as 5.05 eV. The breakdown voltage is defined as the drain-source voltage when ionization integral equals to unity. The $R_{on,sp}$ refers to the value measured at V_{gs} = 20 V and V_{ds} = 1 V.

3. Results and discussion

Fig. 2 shows the static *I–V* characteristics of the S-TMOS with varied L_s and the C-TMOS. In reverse conduction condition, S-TMOS turns on earlier than C-TMOS because the integrated SBD turns on prior to the P-body/N-drift junction in C-TMOS. Moreover, the larger L_s is, the lower turn-on voltage is. This happens because the ratio of Schottky junction to PN junction is increased. When V_{ds} is –2 V at $L_s \geqslant 0.4$ μm, the SBD of S-TMOS has already turned on and the reverse cur-

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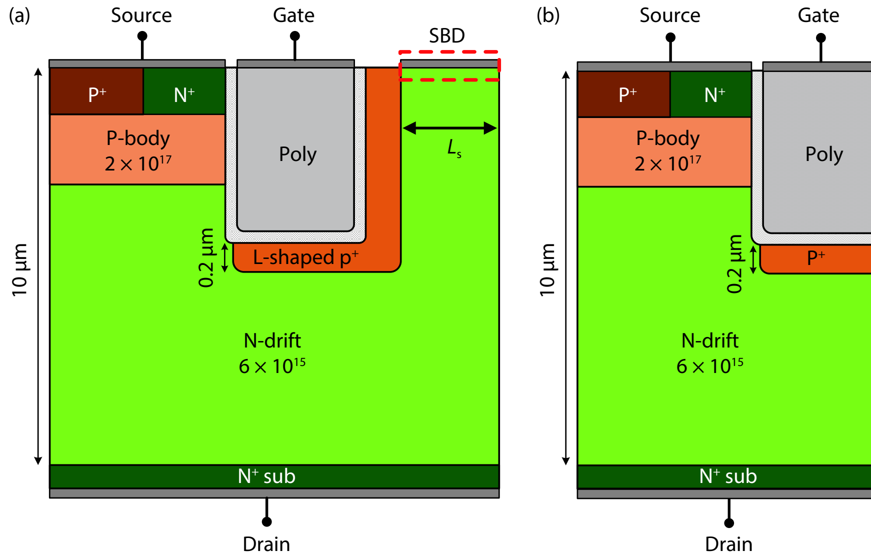

Fig. 1. (Color online) Device structure of (a) S-TMOS and (b) C-TMOS.

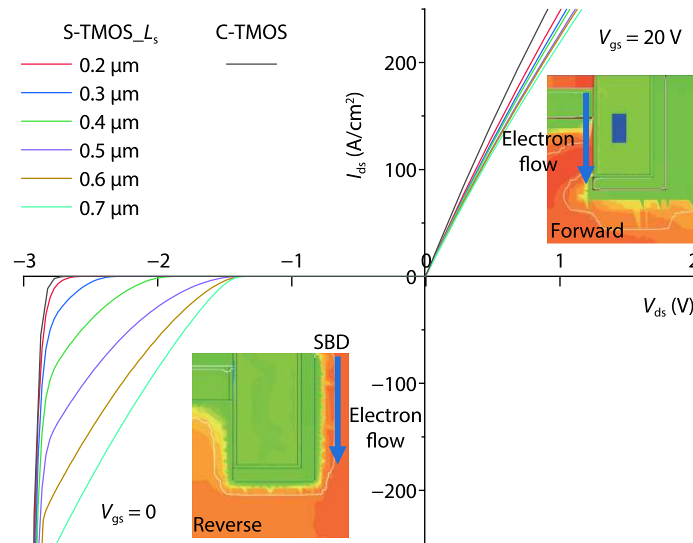

Fig. 2. (Color online) Forward and reverse conduction *I–V* characteristics of C-TMOS and S-TMOS with varied L_s. The insets show the forward and reverse current contours of S-TMOS at V_{ds} = +/– 2 V.

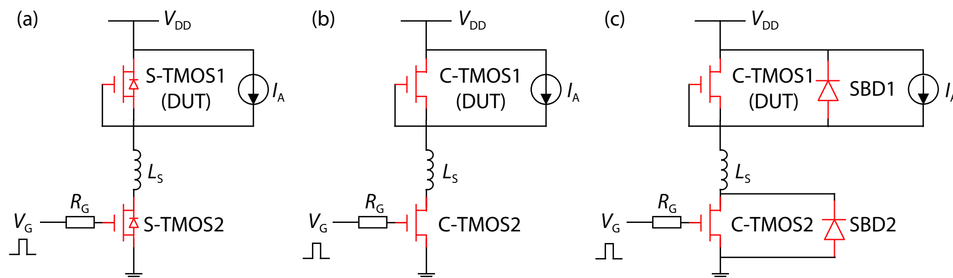

Fig. 3. (Color online) Test circuit for (a) S-TMOS, (b) C-TMOS, and (c) C-TMOS paralleled with an external SBD.

rent flows through the Schottky contact. While the intrinsic body diode of the C-TMOS has not turned on yet. When L_s > 0.5 μm, the V_F of S-TMOS hardly drops anymore and remains at about 1.5 V, which is much lower than 2.7 V of C-TMOS. In forward conduction condition, all current in S-TMOS flows through the reverse layer channel, and the SBD does not work. The forward conduction characteristics of the two designs are similar. The different cell areas caused by different L_s make the $R_{on,sp}$ of the devices slightly different. The $R_{on,sp}$ of S-TMOS with L_s = 0.5 μm (4.44 mΩ·cm²) is a little bit larger than that of C-TMOS (3.71 mΩ·cm²).

The test circuits in Fig. 3 are used to evaluate the reverse recovery performance of the devices. V_G is switched between 0 and +20 V. The chip areas of all devices are fixed

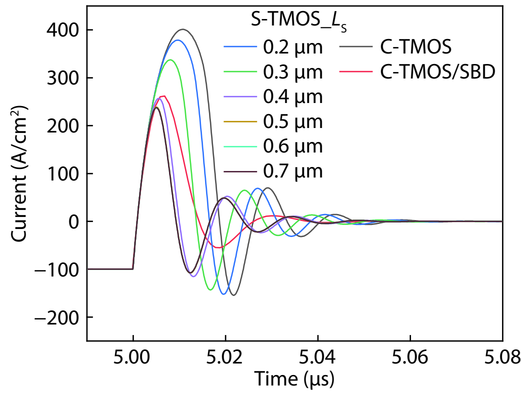

Fig. 4. (Color online) Reverse recovery current waveforms of C-TMOS, S-TMOS with varied L_s and C-TMOS/SBD solution.

to be 1 cm². The load inductance and load current are 5 nH and 100 A/cm², respectively.

Fig. 4 shows the reverse recovery current waveforms of C-TMOS, S-TMOS with varied L_s and C-TMOS/SBD solution. The carriers stored in drift region must be fully extracted to withstand reverse voltage during reverse recovery, and this process will generate current overshoot. More carriers will cause larger current overshoot and prolonged oscillations. The current overshoot not only increases power consumption and slows down the transfer speed but also reduces reliability of the whole system. Since the reverse recovery current flows through the intrinsic body diode in C-TMOS and the intrinsic body diode is a bipolar device, C-TMOS has the largest current overshoot and Q_{rr}. For S-TMOS, the reverse recovery current flows through the integrated SBD, resulting in better reverse recovery performance. As L_s increases, the reverse recovery current is lower and the reverse recovery time is shorter, so both the reverse recovery current oscillation and the Q_{rr} decrease. Compared with C-TMOS paralleled with an external SBD, when $L_s \geqslant 0.5$ μm, the S-TMOS achieves a lower forward current overshoot. Since the SBD integrated inside the cell of S-TMOS suppresses the bipolar conduction more effectively, the Q_{rr} of S-TMOS (L_s = 0.5 μm) is only 1.25 μC, which is much smaller than that of C-TMOS (5.04 μC) and C-TMOS/SBD solution (2.11 μC).

The influence of L_s on BV and Q_{rr} of S-TMOS is shown in Fig. 5(a). With the increase in L_s, the reverse recovery performance of S-TMOS is greatly improved, resulting in a significantly reduced Q_{rr}. The drain leakage current of C-TMOS and S-TMOS (L_s = 0.5 μm) at forward blocking state is shown in Fig. 5(b) and the distribution of equipotential lines is also shown in the inset. Since the P⁺ shielding region is deep enough, the protection effect on Schottky contact is very effectively. There is almost no potential line passing through the Schottky area and the electric field under high drain voltage is successfully shielded, thereby avoiding the barrier lowing of Schottky contact, so the breakdown voltage of S-TMOS is barely reduced compared with that of C-TMOS. Based on this discussion, the optimum value of L_s is selected as 0.5 μm and it is used in subsequent simulations.

Gate–drain capacitance (C_{gd}) and gate–drain charge (Q_{gd}) are key factors which affect the switching speed of power devices. Fig. 6(a) compares the C_{gd} of C-TMOS and S-TMOS under different drain-source voltages. The coupling effect between gate and drain is weakened due to the shielding ef-

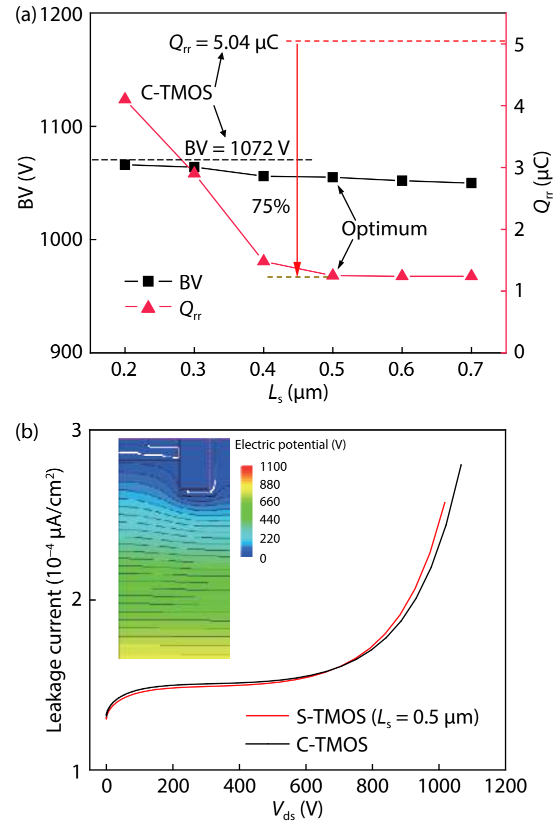

Fig. 5. (Color online) (a) Influence of L_s on BV and Q_{rr} of S-TMOS. (b) Leakage current of S-TMOS (L_s = 0.5 μm) and C-TMOS.

fect of the L-shaped P⁺ region, resulting in reduced C_{gd}. The C_{gd} of C-TMOS and S-TMOS are 179 and 139 pF/cm² at V_{ds} = 600 V, respectively.

Meanwhile, gate charges were tested with the circuit in the inset of Fig. 6(b). The load inductance and load current used in simulation are 10 nH and 100 A/cm², respectively. The S-TMOS exhibits a narrower Miller platform and a lower Q_{gd} value of 143 nC/cm² than that of the C-TMOS (209 nC/cm²), as shown in Fig. 6(b). By the way, the rising slope of V_g for S-TMOS is a little bit lower before reaching Miller platform because the L-shaped P⁺ region shorted to source contact leads to a relatively larger gate-source charge Q_{gs}. Therefore, S-TMOS has a desirable smaller ratio of Q_{gd} relative to Q_{gs}. This feature is crucial to suppress additional losses caused by a parasitic turn-on half bridge circuit and allows for a well-controlled switching with very low dynamic losses[12, 14].

The simulation circuit for switching characteristic is presented in Fig. 7(a). The MOSFETs turn off at t = 25 μs and all device areas are 1 cm². The load inductance used in simulation is 10 nH. A SiC Schottky barrier diode is used as the freewheeling diode. The load current (I_A) and the gate resistor (R_G) are set as 100 A/cm² and 10 Ω, respectively. Fig. 7(b) shows the turn-off waveforms of the two MOSFETs. The S-TMOS has a delay before turn-off process due to a larger Q_{gs}, but there is almost no extra power consumption during the delay. Actually, the two devices have almost the same current rise time during turning on and fall time during turning off. Owning to a smaller Q_{gd}, the S-TMOS achieves lower turn-off loss (E_{off}) since Q_{gd} plays a more important role in turning off. The E_{off} of S-TMOS is 2.49 mJ/cm², which has reduced by 19% compared with 3.08 mJ/cm² of the C-TMOS.

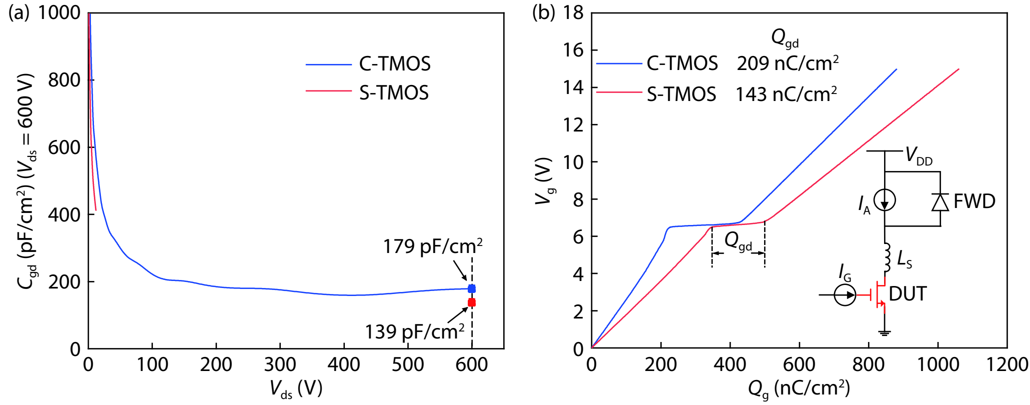

Fig. 6. (Color online) (a) Gate-Drain capacitance (C_{gd}) of the C-TMOS and S-TMOS. (b) Gate charge characteristic curves of C-TMOS and S-TMOS.

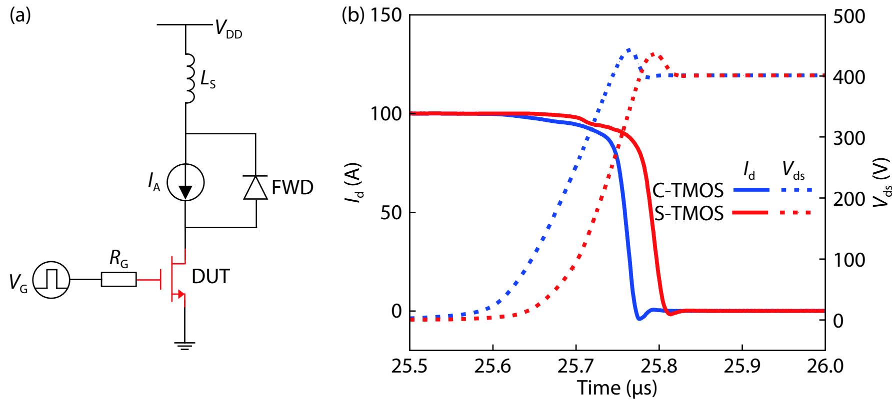

Fig. 7. (Color online) (a) Test circuit for switching characteristic. (b) Turn- off waveforms of C-TMOS and S-TMOS.

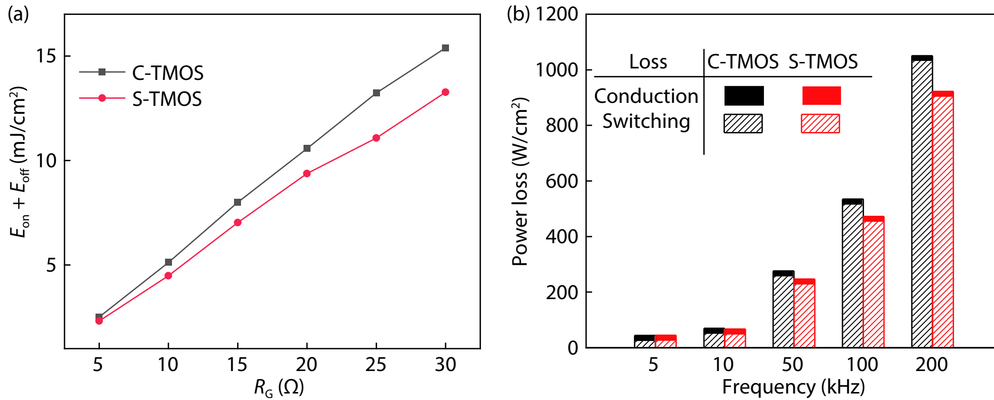

Fig. 8. (Color online) (a) Dependence of switching loss (E_{on} + E_{off}) on gate resister R_G. (b) Comparison of power losses as a function of switching frequency f (@ R_G = 10 Ω).

Fig. 8(a) shows the influence of the gate resister R_G on switching loss (E_{on} + E_{off}) in one switching cycle. The S-TMOS exhibits a lower switching loss at all different R_G values. As R_G increases, the difference of the switching loss between the two MOSFETs increases. The total power losses P_t of the device consists of conduction loss and switching loss, and can be calculated by[15, 16]:

$$P_t = kR_{on,sp}I_d^{\ 2} + f(E_{on} + E_{off}),$$

where k is the duty cycle defined as the ratio of the interval in which the MOSFET conducts versus the total period, and f is the switching frequency. Fig. 8(b) shows the power losses as a function of f and the duty cycle is set as 0.5. With the increase in switching frequency, conduction loss is almost negligible and switching loss becomes the major part of power dissipation. The advantage of S-TMOS also increases with the increasing frequency. When operating at 200 kHz, the S-TMOS realizes 13% reduction in the power losses compared with the C-TMOS.

Table 1 summarizes the performance parameters for the two devices. Obviously, the S-TMOS obtains better comprehensive performances than C-TMOS.

A feasible fabrication procedure is shown in Fig. 9. Tilted implantation is adopted to form the L-shaped P^+ shielding region. To form the Schottky contact and ohmic contact at the same time, Nickel (Ni) single ohmic/Schottky contact process scheme is chosen in metallization process[17, 18].

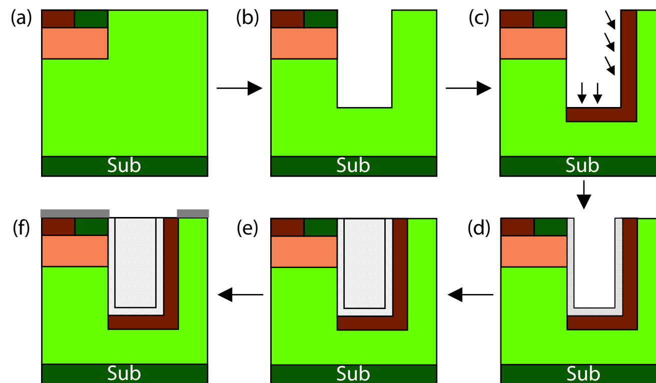

Fig. 9. (Color online) Key fabrication process flows for the S-TMOS: (a) ion implantation to form the P-well and N+, P+ sources, (b) gate trench etching, (c) P+ shielding region implantation, (d) thermal oxidation to form the gate oxide, (e) poly silicon deposition, (f) metallization.

Table 1. Performance comparison of C-TMOS and S-TMOS.

Parameter	S-TMOS	C-TMOS
$R_{on,sp}$ (mΩ·cm²)	4.44	3.71
BV (V)	1055	1072
V_F (V)	1.5	2.7
Q_{rr} (μC)	1.25	5.04
C_{gd} (pF/cm²) (@ V_{ds} = 600 V)	139	179
Q_{gd} (nC/cm²)	143	209
E_{off} (mJ/cm²)	2.49	3.08
E_{on} + E_{off} (mJ/cm²)	4.50	5.16

4. Conclusion

A novel SiC trench MOSFET with an integrated SBD and L-shaped P+ shielding region is proposed in this paper. The integrated SBD works as a free-wheeling diode with a low reverse on-state voltage and reverse recovery charge. Compared with conventional SiC trench MOSFET, the V_F and Q_{rr} of S-TMOS has reduced by 44% and 75% without sacrificing the *BV*, resulting in excellent third quadrant characteristic. Furthermore, the P+ shielding region reduces the gate–drain capacitance and gate–drain charge. The Q_{gd} and C_{gd} of S-TMOS reduce by 32% and 22% in comparison with that of C-TMOS, leading to lower switching power consumption. Furthermore, due to the P+ shielding region, the leakage current hardly increases with the increase of drain-source voltage. The S-TMOS is much more competitive and promising in high power and high frequency applications.

Acknowledgements

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