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Effect of microstructure of Au80Sn20 solder on the thermal resistance TO56 packaged GaN-based laser diodes

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Abstract: Au80Sn20 alloy is a widely used solder for laser diode packaging. In this paper, the thermal resistance of GaN-based blue laser diodes packaged in TO56 cans were measured by the forward voltage method. The microstructures of Au80Sn20 solder were then investigated to understand the reason for the difference in thermal resistance. It was found that the microstructure with a higher content of Au-rich phase in the center of the solder and a lower content of (Au,Ni)Sn phase at the interface of the solder/heat sink resulted in lower thermal resistance. This is attributed to the lower thermal resistance of Au-rich phase and higher thermal resistance of (Au,Ni)Sn phase.

Key words: Au80Sn20; laser diodes package; thermal resistance

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1. Introduction

With the rapid evolution of semiconductor laser technology, the optical power of laser diodes (LDs) keeps increasing, and the joule heat induced by series resistance increases. The joule heat needs to be dissipated effectively otherwise will adversely affect LD performance and reliability[1]. Therefore, packaging techniques with a low thermal resistance are needed. The total thermal resistance of LD packaging is limited by the portion with the highest thermal resistance. The solder layer, which bonds LD chips and heat sinks, is the portion with lowest thermal conductivity in the GaN-based LD package. Therefore, it has a significant effect on the total thermal resistance[2]. To improve the optical power, decreasing the thermal resistance of the bonding layer is effective[3, 4].

As the material connecting the LD chips and the heat sink, solder plays an important role in the thermal packaging system. Au80Sn20 alloy has good thermal and electrical conductivity. As a hard solder with high melting point, Au80Sn20 alloy has good creep resistance and mechanical properties, and thus it can be used in LDs, power electronics, MEMS sensors, and other applications[5–8]. Due to the big difference of electronegativity between Au (2.3) and Sn (1.8), Au80Sn20 alloy tends to form a stable intermetallic compound (IMC) rather than solid solution. The IMCs in Au80Sn20 alloy play a key role in the mechanical and thermoelectric properties[9, 10].

In this paper, the thermal resistance of GaN-based blue laser diodes packaged in TO56 cans were measured by the forward voltage method. The microstructures of Au80Sn20 solder were then investigated to understand the reason for the difference in thermal resistance. It was found that the microstructure with higher content of Au-rich phase in the center of the solder and lower content of (Au,Ni)Sn phase at the interface of the solder/heat sink resulted in lower thermal resistance.

2. Experimental details

The packaged LD samples studied here are from the same epitaxial wafer and chip processing but different packaging processing, and the chip size of both is 200 × 400 μm^2. The results shown in this paper are from typical samples of each batch named E09 and Y00. These two samples have a similar structure, and the schematic diagram of the structure is shown in Fig. 1. The Au80Sn20 solder bonds the LD chip and heat sink, and there are two solder layer interfaces.

We first measured the thermal resistance of TO56 packaged GaN-based LDs using the forward voltage method, which was reported by us previously[11]. It is based on the linear relation between the junction temperature (T) and the forward voltage (V_f). When the injection current is a constant[12–15], the relation can be fitted as follows:

$$V_f = AT + B, \tag{1}$$

where T is the junction temperature of the LD, and A and B are the fitting parameters. We first measured the value of the temperature-sensitive parameter A. Next, by changing the injection current from an operation current to a very low current at which joule heat is negligible, we measured the voltage variation (ΔV) of the LD caused by the variation of the junction temperature (ΔT) using a MDO4104-3 mixed domain oscilloscope. The ΔT can be calculated by the following equation:

$$\Delta T = (V_{f0} - V_{ft}) / A, \tag{2}$$

where V_{ft} is the forward voltage of the LD at high injected current. As the joule heat dissipates rapidly, the decrease of junction temperature will cause the forward voltage to in-

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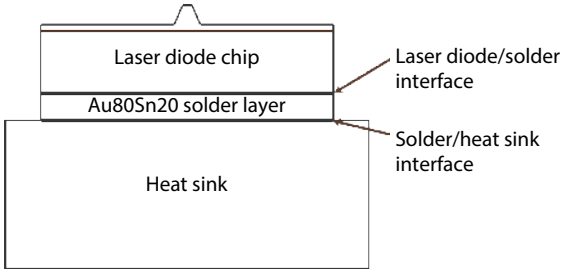

Fig. 1. The schematic diagram of structure of packaged laser diodes.

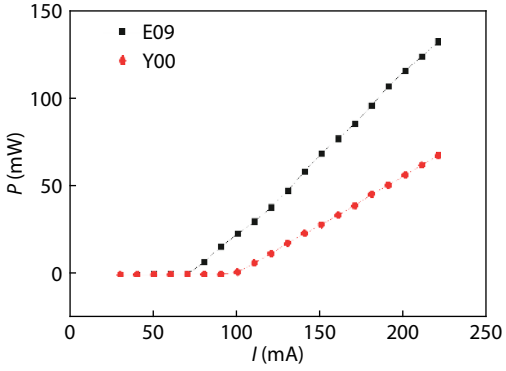

Fig. 2. (Color online) The *P*–*I* curve of sample E09 and Y00.

crease[16]. V_{f0} is the forward voltage of the LD when the junction temperature decreases to room temperature. The thermal resistance (R_{th}) of the LD can be expressed as[15]:

$$R_{th} = \Delta T_J / \left(I_H V_H - P_{opt}\right), \quad (3)$$

where I_H is the injection current, while V_H and P_{opt} are the voltage and optical output power of the LD under the corresponding injection current I_H.

For IMCs analysis, the scanning electron microscope (SEM) and energy dispersive X-ray spectroscopy (EDS) have been carried out. We selected FEI quanta FEG 250 to perform SEM, which has EDS subassembly named EDXX Apollo XP. In order to observe the IMCs in the solder joint clearly, the packaged LDs were polished into cross-sectional samples.

3. Results and discussions

Fig. 2 shows the power–current (*P*–*I*) curves of two LD samples. E09 has a lower threshold current and a higher slope efficiency than Y00. It is suggested that the difference of optical power between these two LD samples is caused by the different thermal resistance.

In order to verify the effect of thermal resistance on optical power, we then measured the thermal resistance of the two samples. From the *I*–*V* curves under different measured temperatures, the relation between the junction temperature and the forward voltage was fitted with Eq. (1), and the temperature-sensitive parameter *A* was thus calculated to be 4.33 mV/K for E09, 2.66 mV/K for Y00. We then measured the time-resolved voltage variation of these two samples. In the working state, after the LD samples reached a steady-state, we measured the working current I_H, voltage V_H and optical output power P_{opt}. In the measuring state, we measured the variation of forward voltage from the very beginning of the measuring state to room temperature. According to our previous simulation and experimental work[11, 17], the time-resolved voltage curve of a LD can be distinguished by the slope and the time scale. When the current injected into a LD was reduced to a very low value, the heat generated in the LD chip dissipated to the heat sink. During this process, the temperature at different positions of the LD change over different time scale and different rate. The time scale of the heat dissipation of a LD chip and solder junction were 0–10^{-4} s and 10^{-4}–0.1 s, respectively. Fig. 3 shows the first two periods of

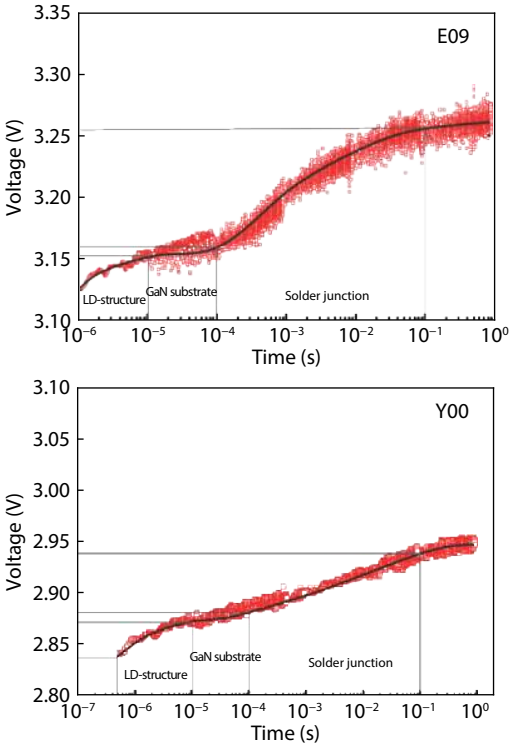

Fig. 3. (Color online) The time-resolved voltage variation during the measurement.

Table 1. Parameters of thermal resistance calculation.

Sample	*A* (mV/K)	V_{f0}–V_{ft} (mV)	$I_H V_H$–P_{opt} (W)	R_{th} (K/W)
EL-00	4.33	85.37	0.47	41.95
YJ-09	2.66	59.05	0.34	65.29

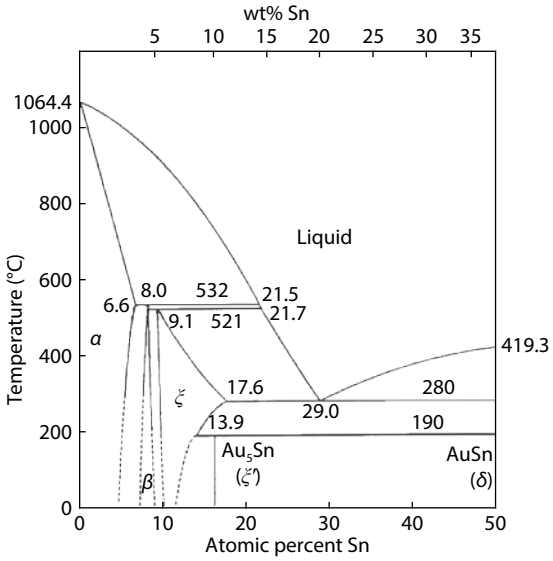

Fig. 4. Gold-rich portion of the Au–Sn phase diagram.

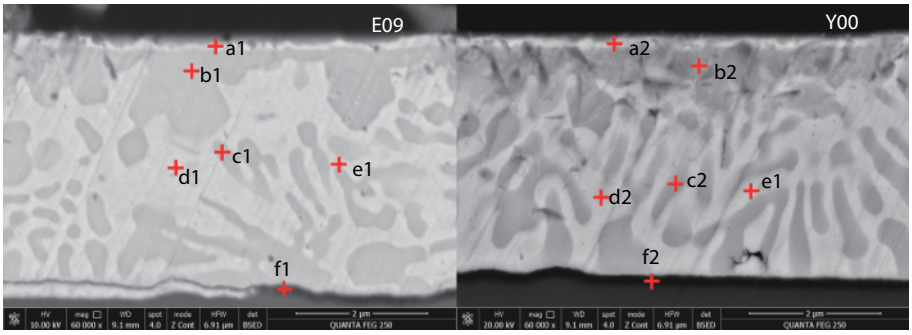

Fig. 5. Cross-sectional SEM of the two samples. The red crosses are the EDS measure points.

Table 2. EDS results of the points marked in Fig. 5.

Parameter	a		b		c		d		f	
	a1	a2	b1	b2	c1	c2	d1	d2	f1	f2
Phase	(Au,Pt)Sn	(Au,Pt)Sn	AuSn	AuSn	AuSn	AuSn	Au_5Sn	Au_5Sn	(Au,Ni)Sn	(Au,Ni)Sn
at%Au	47.4	46.88	67.25	60.11	79.73	76.86	87.27	81.97	41.13	36.03
at%Sn	46.69	47.01	32.75	39.89	20.27	23.14	12.73	18.03	40.49	33.71
at%Pt	5.91	6.11	—	—	—	—	—	—	—	—
at%Ni	—	—	—	—	—	—	—	—	18.38	30.26

the voltage variation with time. The first period is caused by heat dissipation in the LD chip, and the second period is caused by heat dissipation in the solder layer.

The voltage variation of the solder layer (V_{f0}–V_{ft}) is 85.37 mV for E09 and 59.05 mV for Y00. Table 1 shows all the parameters of thermal resistance calculation. According to Eqs. (2) and (3), the thermal resistance was 41.95 K/W for E09 and 65.29 K/W for Y00. The total thermal resistance of a LD is determined by chip structure, bonding materials and microstructure, and heat sink. In our study, the chip structure, the heat sink, and the bonding materials are the same, and therefore we focused on the microstructure of the solder layer, as follows.

The gold-rich portion of the Au–Sn phase diagram is shown in Fig. 4[18]. The IMC phases of interest in solder are β($Au_{10}Sn$), ζ'(Au_5Sn) phase, ζ(Au_5Sn)phase and δ(AuSn) phase. From the phase diagram, the Au80Sn20 alloy system consists of ζ' phase and δ phase at room temperature. In practice, however, the nonequilibrium solidification usually results in the formation of primary ζ phase. In addition, Teo *et al.* have also found β phase in Au80Sn20 solder joint[19]. The eutectic point at 280 °C and 29.0 at.% Sn has the reaction $L \leftrightarrow [\zeta + \delta]$. There is a peritectoid reaction at 190 °C and 16.0 at.% Sn, $\zeta' \leftrightarrow [\zeta + \delta]$. Prior to this reaction, it is believed that the reaction at 190°C and 18.5 at. % Sn is $\zeta \leftrightarrow [\zeta' + \delta]$. The ζ-Au_5Sn phase emerges from the peritectic $\zeta \leftrightarrow [\beta + L]$ 9.1 at.% Sn at 521 °C to 17.6 at.% Sn at 280 °C, and 13.9 at.% Sn at 190 °C. The composition of Sn in the hexagonal structure ζ' phase is 16%, where it remains until the temperature reaches 190 °C. The ζ phase has a Mg-type close-packed hexagonal structure. As the Sn concentration increases, the volume of ζ phase per atom will increase. The δ (AuSn) phase is a hexagonal structure intermetallic compound with a melting point of 419.3 °C. The β phase is considered as a kind of commercial gold solder which is used as Au-protected surfaces[20–22].

Fig. 5 shows the cross-sectional SEM images of the solder layer in these two samples. The EDS results and the possible phase of the marked points are shown in Table 2. The thickness of solder layer is roughly 4 μm. The a1, a2, b1, b2 points are at the LD chip/solder interface region. From the EDS results, it can be found that the δ phase is in the same region. Because Sn-rich phase such as δ has a lower surface tension than Au-rich phase, δ phase tends to coalesce at the surface[23, 24]. During the packaging process, Pt diffused from the LD electrode and coalesced at the LD chip/solder interface. As the EDS data shows, there is Pt–Sn phase in the region around points a1, a2. Also, the solder/heat sink interface has an analogous phenomenon. Under the effect of thermal diffusion, Ni in the heat sink coalesced at the solder/heat sink interface. In these regions, Ni replaced Au in AuSn phase to form (Au,Ni)Sn phase[25]. The gray line on the left part of the interfacial layer at the bottom side of E09 is void, which could be induced during the SEM sample preparation. In the center of the solder layer, the bright phase is Au-rich, and the dark phase is Sn-rich. It is notable that most of the Sn-rich phase in sample E09 distributes in the form of spheroidized structure. On the other hand, most of the Sn-rich phase in sample Y00 is lamellar structure. The hard and brittle nature of the primary ζ' phase which has a dendrite microstructure leads to difficulties in the manufacture of Au80Sn20 solder. According to the phase diagram, Au80Sn20 alloy consists of ζ' phase and δ phase at room temperature. The reason for the difference of morphology between two samples may be the different cooling rate. At a fast cooling rate, the dendrite growth of ζ' phase will be suppressed. Furthermore, the suppressed growth results in refined microstructure and metastable phases. At the same time, the dendrites of ζ' phase will generate more fractions. A mass of branches from the fractions are intertwined. The intertwining process divided the lamellar Sn-rich phase into a spheroidized structure. This structure transformation has a good effect on the mechanical properties of the solder[26].

It is suggested that the main reason for the higher thermal resistance in sample Y00 is the lower content of the

Au-rich phase. Au-rich phases in the center are the primary phase ζ' and metastable phase. The Au-rich phase not only has a good mechanical property, but also has a lower thermal resistance. As the content of Au-rich phase in E09 is much higher than that in Y00, E09 has a lower thermal resistance. In addition, the interface also has a great effect on thermal resistance. In this case, the LD/solder interfaces of the two samples are analogous to some extent. However, the content of Ni in the solder/heat sink interface has a remarkable difference. It is believed that Ni comes from the heat sink by thermal diffusion. Since (Au,Ni)Sn is harmful to thermal resistance improvement, the decrease of (Au,Ni)Sn phase in E09 ensures a good thermal contact[27, 28].

4. Conclusion

In summary, the thermal resistance of GaN-based blue laser diodes packaged in TO56 cans were measured by the forward voltage method. The microstructures of Au80Sn20 solder were then investigated to understand the reason for the difference in thermal resistance. It was found that the microstructure with higher content of Au-rich phase in the center of solder and lower content of (Au,Ni)Sn phase at the interface of the solder/heat sink resulted in lower thermal resistance. This finding will help improve the packaging processing in the future.

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