REVIEWS

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Silicon photonic transceivers for application in data centers

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Abstract: Global data traffic is growing rapidly, and the demand for optoelectronic transceivers applied in data centers (DCs) is also increasing correspondingly. In this review, we first briefly introduce the development of optoelectronics transceivers in DCs, as well as the advantages of silicon photonic chips fabricated by complementary metal oxide semiconductor process. We also summarize the research on the main components in silicon photonic transceivers. In particular, quantum dot lasers have shown great potential as light sources for silicon photonic integration—whether to adopt bonding method or monolithic integration—thanks to their unique advantages over the conventional quantum-well counterparts. Some of the solutions for high-speed optical interconnection in DCs are then discussed. Among them, wavelength division multiplexing and four-level pulse-amplitude modulation have been widely studied and applied. At present, the application of coherent optical communication technology has moved from the backbone network, to the metro network, and then to DCs.

Key words: data center; silicon-based optoelectronic transceiver; high-speed optical interconnection; quantum dot lasers

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1. Introduction

With the rapid popularization of personal computers and smartphones, the construction of 5G networks, cloud services, the Internet, and the Internet of Things, global data traffic and the consumption of information and communications technology (ICT) are explosively increasing (as shown in Fig. 1). In the short span of more than a decade in the 21st century, global data traffic has reached the ZB scale and it is predicted to continue to grow exponentially in the coming years. A recent white paper published by IDC forecasts that the global datasphere will grow up to 175ZB in 2025 from 33ZB in 2018[1]. At the same time, Nature's forecast shows that the total electricity demand of ICT will accelerate in 2020 and will reach near 9000 TWh in 2030[2]. The electrical consumption of data centers (DCs) would take a large slice of this demand. A huge amount of data traffic is imported into DCs and needs to be processed rapidly. This places higher requirements on DCs and supercomputers in terms of information processing speed, total storage capacity and transmission bandwidth of the physical hardware layer, as well as total electricity reduction.

So far, the development of semiconductor electronic integrated circuits (IC) has basically followed Moore's Law to improve computing and storage capacity by reducing the size of transistors, optimizing the device's structure, and increase integration. Nowadays, DCs and supercomputers use parallel operation technology: parallel processing or computing with multiple processors to improve the performance that cannot be achieved with a single processor. However, based on the existing microelectronic material system and operating principle, the transmission bandwidth of traditional copper interconnection is close to its physical limit. This makes the processing speed of chip processors much faster than the data exchange speed of the copper interconnections between the chips. Thus, the parallel processing capability between chips is restricted[3]. Worse still, the copper interconnections suffer from problems of power consumption, signal interference, and high delay, which reduce performance and cost. Therefore, the electrical interconnection based on traditional microelectronic technology is facing significant challenges.

The performance of copper links in high-speed interconnection has reached its physical limit, thus a new generation of high-speed short-distance interconnection technology needs to be developed. Optical transmission has the characteristics of high bandwidth, low delay, low power consumption, low transmission loss, low crosstalk and strong spatial multiplexing capability, and has been recognized as the successor

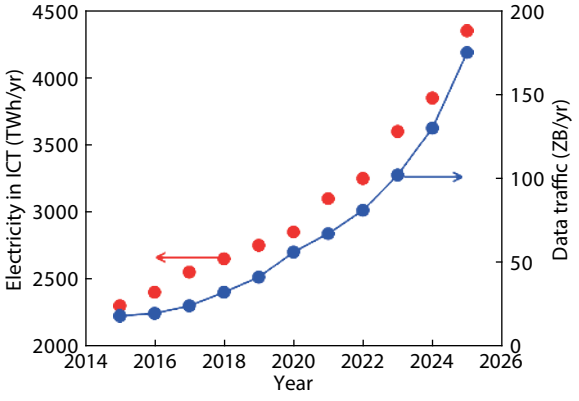

Fig. 1. (Color online) Forecast of global data traffic and electricity in ICT[1, 2].

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of copper links[4]. High-speed data transmission between racks and racks, boards and boards, chips, and chips in DCs can be realized by optical interconnections.

However, traditional photonic integrated circuit (PIC) manufacturing processes are complex because many functional photonic components are based on different material systems. For example, laser diodes (LDs) are mainly based on InP[5] or GaAs[6], modulator uses the most sensitive $LiNbO_3$ material[7, 8], most of the waveguides are fabricated by using SiO_2/Si or SiO_2/Si_3N_4, and the photodetectors (PDs) prefer SiGe[9], *et al*. A main challenge for PICs is how to integrate the different materials and functional components on the same substrate while ensuring that they can operate well together.

Silicon photonic chips have shown great potential as a new large-scale optoelectronic integrated chips because they combine low cost, large scale, high integration and reliability of mature complementary metal oxide semiconductor (CMOS) process with high bandwidth, low latency, low power consumption and strong spatial multiplexing of optical interconnects. Si is well known for its extremely low loss waveguides and various passive components, as follows:

(1) Si is a cheap and stable material. It is used to produce 300-mm large-scale wafers and the silicon-based waveguide manufacture is compatible with CMOS process. Thus, it can be integrated with CMOS electronic circuits.

(2) Si has an ultra-low material absorption coefficient at communication wavelengths.

(3) Si has an ideal oxide SiO_2 with extremely low optical loss and high electrical isolation. Si waveguides have the high refractive index contrast in both horizontally and vertically on silicon-on-insulator (SOI) substrates. The curved waveguide is able to have a small radius to make the optical devices more compact and then reduce the overall PIC package area.

In addition to the monolithically integrating Si waveguides, spot-size converters (SSCs)[10], beam splitters[11], wavelength division multiplexers[12], demultiplexers[13], grating couplers (GCs)[14] and other passive components on SOI. Optical active components such as Si modulators[15] and Ge PDs[16] are also monolithically integrated by standard CMOS process.

However, because Si is an indirect bandgap semiconductor with low emission efficiency, it is difficult to be used as an efficient and reliable light source for silicon photonic integrated chips. Researchers proposed to dope with impurities to improve internal quantum efficiency, such as erbium doped silicon which uses Er^{3+} as the atomic luminescence center[17]. Others have proposed to adjust it to direct bandgap semiconductor through energy gap engineering, such as growing IV alloys on Si substrate[18], introduction of tensile strain, superlattice[19], heavy doping[20], etc. Although many schemes have been put forward to improve its emission efficiency[21], it still has not reached the application level due to its large optical loss.

Simultaneously, it has been proposed to introduce high-gain III–V semiconductors on Si substrates to fabricate efficient LDs[22–29]. There are two types of III–V semiconductor lasers for optical interconnection: vertical-cavity surface-emitting lasers (VCSELs) and edge emitting lasers. Nowadays, most of short reach (< 300 m) optical links are based on VCSELs over multimode fibers (MMFs). Typically, VCSEL plays an important role in "top of rack (TOR) switch" in each rack of a server[30]. VCSELs are easy to fabricate laser array, easy to couple to MMFs and they are very cheap. It is presently impossible for PICs with edge emitting laser to compete against VCSELs on price, especially in extremely short distance. However, due to VCSEL's structure characteristics, it is hard to maintain single-mode operation when the optical output is high[31]. In addition, MMFs cost more than standard single-mode fibers (SSMFs). Besides, the bandwidth distance product of VCSEL is about 2 GHz·km. At 25 Gb/s, the maximum distance is about 100 m. Therefore, it is more suitable for edge emitting laser with SSMFs to apply in more than 300 m optical links in DC.

Until now, three schemes have been widely used to realize III–V high-efficiency edge emitting LDs on Si:

(1) Hybrid integration or flip-chip bonding[22]: the III–V LD chips are placed on the PIC by flip-chip bonding and the light from the gain section of the III–V LD chips is directly coupled into the Si waveguide by edge coupling. This method can separately manufacture and optimize III–V components and silicon photonics chips, but it is mainly limited by the large optical coupling loss, the complexity of the device package, and the additional cost of separately manufacturing the laser device and PIC chip.

(2) Heterogeneous integration or wafer-bonding[28, 29]: using wafer-bonding technique to transfer the III–V materials on the SOI and the light from the gain section enters vertically into the underlying Si waveguide by evanescent coupling. Placing a large number of small III–V epitaxial wafers on target area in large-scale SOI can significantly reduce the total cost. This method can also achieve multiple functions by integrating different epitaxial structures on a single chip.

(3) Direct hetero-epitaxial integration[23–27]: at present, the direct epitaxial growth of III–V materials on Si is the most promising monolithic integration solution for Si-based light sources. Because it is more suitable for large-scale integration and production, especially for direct growth of quantum dot (QD) LDs on Si. Nevertheless, the lifetime and reliability of the hetero-epitaxial LDs need to be further improved due to the mismatch of lattice, polarity and thermal expansion coefficient between Si and III–V materials. Additionally, to eliminate threading dislocations from the III–V/Si interface, a thick buffer layer is adopted, which makes it difficult to couple the output from LDs into the waveguide of the Si device layer.

2. Silicon photonics main optical components

The overall performance improvement of a silicon photonic transceiver depends on the performance breakthrough of each optical component. The modulation speed of the active component is a main factor limiting the single-channel bandwidth. Additionally, multiplexers (MUXs) and demultiplexers (DEMUXs) also boost the total speed of a transceiver in wavelength division multiplexing (WDM). Therefore, improving the performance of silicon photonic optical components is a popular research topic for silicon photonic transceivers.

2.1. Laser diode (LD)

At present, there are three mainstream coupling methods for integrated III–V/Si lasers: 1) lens coupling[11], 2) edge coupling[22, 32] and 3) evanescent coupling[28, 33]. This section will also introduce the latest research of using QD-LD dir-

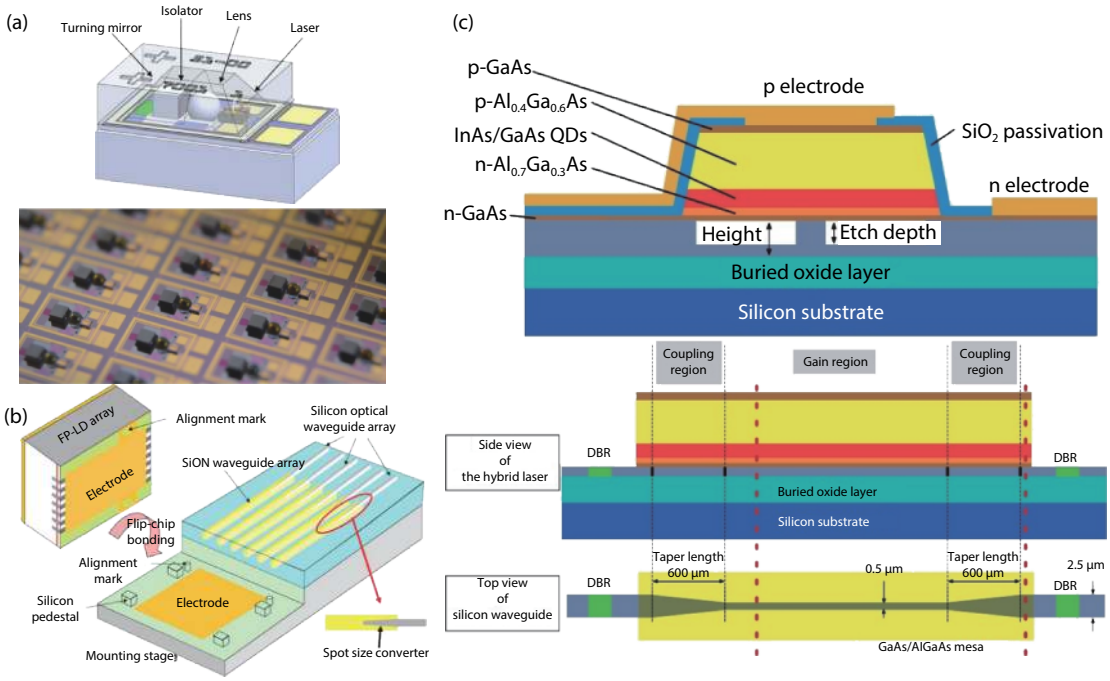

Fig. 2. (Color online) Three coupling modes of silicon-based III–V lasers: (a) lens coupling[11], (b) edge coupling[32], (c) evanescent coupling[33].

ectly as a hetero-epitaxial on a Si substrate.

2.1.1. Lens coupling

Luxtera's products rely on an externally packaged light source that is called the LaMP. This is a mature InP-based laser diode co-packaged with an optical isolator and a lens, as shown in Fig. 2(a)[11]. LaMP is attached at wafer scale to the PIC-wafer with epoxy and uses a lens to collect the divergent light from the LD output. This method enables the light source to be independent of PIC, which can separately debug the performance and keep it away from the heat-generating large-scale integrated circuit (LSIC) chips. So, the negative effect caused by the LSI heat generation is smaller, and the off-chip light source is more flexible than the on-chip light source. However, it requires highly precise optical connectors and paying much attention to polarization characteristics. This would increase the size and cost of the package due to its independence and the introduction of large lens.

2.1.2. Edge coupling

In contrast with an off-chip light source, the on-chip light source is more suitable for large-scale integration in practice situations because it does not need optical connector or introduce polarization. In Ref. [32], a 13-channel LD array is mounted on a Si waveguide platform with solder bumps by flip-chip bonding. The LD array faces the SiON waveguides facet to couple the light into them by edge coupling, as shown in Fig. 2(b). The SiON waveguides have a core section size of 2.5 × 2.5 μm^2, and inversely tapered SSCs are used to transfer the optical mode into the Si optical waveguides with a core section size of 440 nm wide and 220 nm high. The alignment marks placed on the LD and the mounting stage are capable of highly accurate horizontal positioning, and the Si pedestals are also capable of highly accurate vertical positioning. An output power of up to 100 mW and good heat dissipation have been achieved by this method[22], but it requires sub-micron level alignment accuracy, high package cost, and SSCs with limited integration density.

2.1.3. Evanescent coupling

Evanescent coupling avoids the alignment error by using established lithography techniques and it does not introduce SSC, which was firstly demonstrated in 2006[28]. The III–V wafers are directly bonded onto a Si waveguide on the SOI with BCB. Due to the symmetry of the III–V region in the lateral direction, both the laser waveguide and the passive waveguide segment are defined using the same etching step, so that no alignment precision is required. The novelty of this structure is that the optical mode can be amplified from the III–V region while being guided by the underlying Si waveguide region. Moreover, it does not require complex alignment, which is beneficial for increasing integration density and lowering package cost. Japanese scientists have used electron beam lithography to introduce a tapered waveguide and a distributed Bragg reflection (DBR) on both sides of an underlying Si waveguide, as shown in Fig. 2(c)[33], the frequency interval in the spectrum proves that the DBR can define the cavity length of the evanescent laser. However, the disadvantages of this structure are obvious because the heat dissipation performance of the laser is poor due to the high thermal resistance of the bonding material BCB. Furthermore, the mode field confinement of the gain material is too weak to obtain high mode gain and high coupling efficiency because they compete with each other. Additionally, the light continuously crosses through the bonding material and the heavily doped region, resulting in a high absorption loss and a limited output power up to 4 mW[34].

2.1.4. Quantum dot laser on Si substrate

In 1982, Arakawa *et al.* proposed that, due to the three-dimensional quantum confinement of carriers, QD materials have a δ-function-like density of states[35]. This can greatly reduce the carrier thermal excitation, thereby QD-LDs would have lower threshold current density, higher slope efficiency and temperature stability. It is reported that the InAs/GaAs QD-LD has much higher characteristic temperature and slope

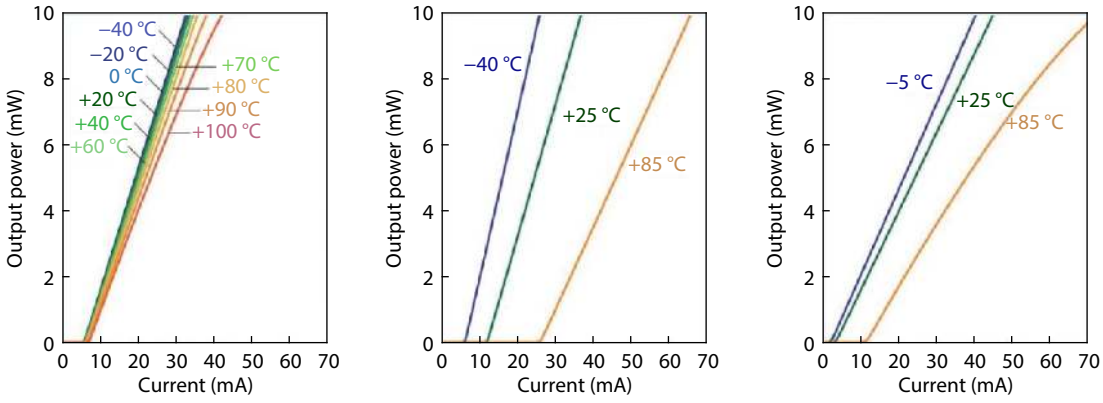

Fig. 3. (Color online) Comparison of typical power–current characteristics of FP lasers. QD-LD (left) is insensitive to temperature and has an almost constant threshold current and slope efficiency. Other two pictures (right two) show the characteristics of two typical QW-LDs[36].

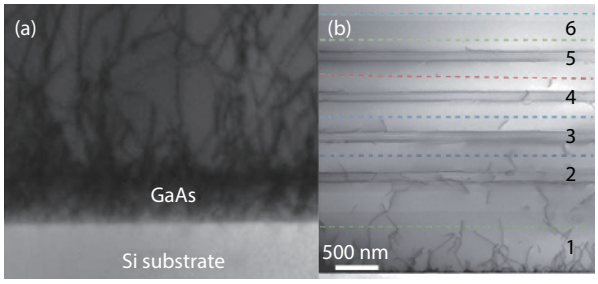

Fig. 4. (a) TEM image of GaAs/Si interface generating a large number of dislocations[43]. (b) The TDs density gradually decreased after DFLs[24].

efficiency than conventional quantum-well (QW) lasers[36], as shown in Fig. 3. Additionally, QD-LDs also exhibit other excellent characteristics, such as narrow spectral line width[37], long device lifetime[38], high modulation bandwidth brought by fast carrier level filling[39] and low relative noise intensity (RIN) due to reduced optical feedback sensitivity[40, 41]. It is particularly important to achieve low RIN in a semiconductor laser, because RIN will increase the bit-error rate of the optical signal which causes reduced data transmission performance[42, 43]. Moreover, QD-laser Inc. predicts that the use of QD-LDs as light sources in silicon photonic transceivers would reduce power consumption by 30% in global DCs[44].

Direct hetero-epitaxy of InAs/GaAs QD-LDs on Si is currently the most promising solution of monolithic integrated light sources on Si[24, 45–47]. Due to the mismatch of lattice, polarity and thermal expansion coefficient between III–V materials and Si, a large number of crystal defects, such as threading dislocations (TDs) with 10^9–10^{10} cm^{-2}, are generated near the interface of the III–V epitaxial buffer layer and the Si substrate[43], as shown in Fig. 4(a). These TDs can slip on the (111) plane and extend into the active region to become non-radiative recombination centers. This would greatly reduce the internal quantum efficiency of the gain medium[48]. By optimizing the growth conditions and various measures to lower the dislocation density, such as double steps obtained by substrate annealing at high temperature[49, 50], offcut substrate[24], V-groove[25], U-shaped patterned Si (001) substrate[47, 51], GaP buffer layer[45, 52], Ge buffer layer[53], low-temperature seed layer[24, 47, 54], dislocation filter layer (DFL)[48, 55] and thermal cycle annealing[56], the negative effects brought from the mismatches between the GaAs and Si have been significantly reduced. The TDs density is decreased by several orders of magnitude to 10^5 cm^{-2}[24], as shown in Fig. 4(b).

Another advantage of QD-LDs on Si is that it has been proven to be defect-insensitive when compared to bulk material LDs and QW-LDs[24]. Because the carriers are three-dimensionally confined in QDs, and each QD is independent of others. Only a very limited part of QDs that TDs, pass through are affected, and most of QDs are intact and can provide optical gain. Additionally, QDs can push away or fix TDs, and the strong strain fields near QDs are able to limit dislocation movement in the plane as shown in Fig. 5(a). Therefore, compared with a QW-LD, a QD-LD is expected to have higher reliability even in the presence of high-density dislocations. Researchers at the Institute of Physics at the Chinese Academy of Sciences, have demonstrated that the room temperature PL spectral intensity of the InAs/GaAs QDs epitaxially grown on Si substrates stronger than that of the InAs/GaAs QDs grown on natural GaAs substrate[47], as shown in Fig. 5(b).

At present, the threshold current density of the QD-LDs epitaxially grown on Si substrates can be reduced to 62.5 A/cm^2, and the output power at 120 °C exceeds 105 mW[24] while a Si-based direct modulated QD-LD with a ring structure fabricated by the researchers, the University of California has a small threshold current of 3 mA with a characteristic temperature of 103 K in the temperature range of 20–40 °C[57]. Schematic diagrams of the two devices are shown in Figs. 6(a) and 6(b), respectively. No matter the QD-LD is integrated on Si by bonding method or monolithically integrated on Si substrate, both play an important role in silicon photonics transceivers. The latter is expected to be the ultimate solution for monolithic integrated light source on Si substrates in the future.

2.2. Modulator

In contrast from the most sensitive $LiNbO_3$ material, monolithic integrated Si-based modulators are based on plasma free carrier effect. The refractive index of a Si waveguide changes by changing the number of free carriers by doping, electrical field methods or optical methods. Fig. 3 shows the three types of Si-based modulators: 1) PIN type, 2) PN-type and 3) MOS-type.

2.2.1. PIN type

In the ridge waveguide PIN modulator, the light field will

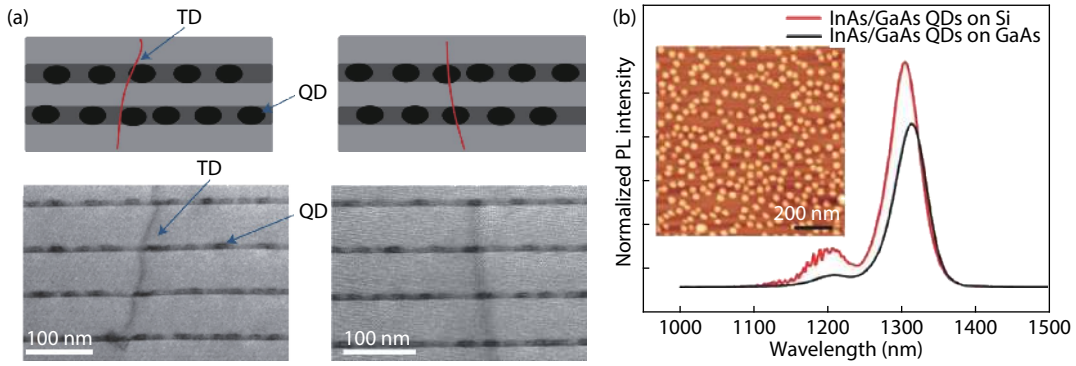

Fig. 5. (Color online) (a) Schematic and TEM images of interaction between QDs and TDs[24]. (b) Room temperature PL spectra of InAs/GaAs QDs grown on GaAs and Si (001) substrates shows that PL peak intensity of QDs grown on Si (001) substrates is stronger, and the inset is an AFM image of a surface InAs/GaAs QDs 1 × 1 μm^2 grown on Si (001)[47].

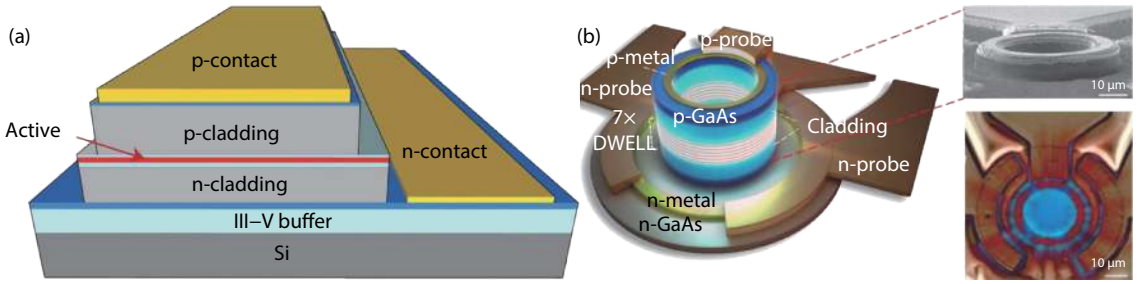

Fig. 6. (Color online) (a) Diagram of Ridge QD-LD reported by UCL university[24]. (b) Schematic diagram of ring structure QD-LD, SEM top view and infrared imaging reported by UCSB University[30].

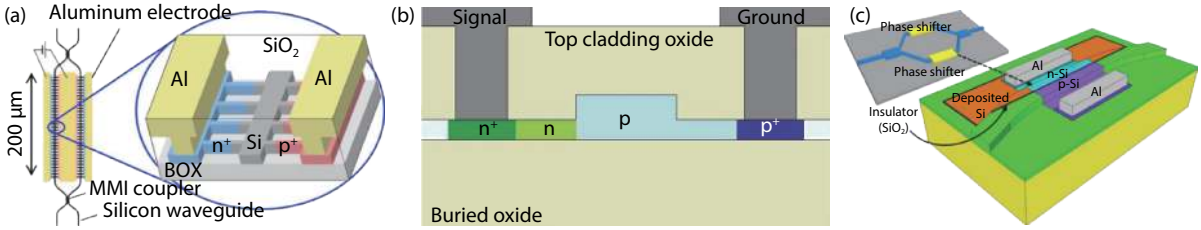

Fig. 7. (Color online) Three types of silicon-based modulators: (a) PIN[31], (b) PN[59], (c) MOS[63].

expand into the flat plates on the two sides. Thicker plates lead to a wider pattern profile, which requires a wider p–n spacing. Thus, it will lead to large resistance, as well as low modulation efficiency and modulation rate. Because the optical modulation characteristics, such as optical mode loss, modulation efficiency, and modulation rate are very sensitive to the thickness of the Si plate, it must be made as an extremely thin when etching. To solve these difficulties, a new structure has been proposed to replace the ridge waveguide, as shown in Fig. 7(a)[31]. The phase shifter of the lateral PIN structure has a sidewall grating structure with the same thickness on the two sides of the waveguide, thus the etching process becomes simple. Carriers are injected into the intrinsic region to change the refractive index by the carrier dispersion effect when forward biased. This structure is capable of stronger lateral optical mode confinement, lower resistance, higher modulation efficiency and modulation rate. The measured DC responses are as follows: π-phase shift voltage (V_π) is 0.3 V, modulation efficiency ($V_\pi L$) is 0.006 V·cm, which is twice that of the ridge waveguide[58], and 3 dB bandwidth is estimated to be 12.5 GHz.

2.2.2. PN-type

The PN-type modulator increases the width of the depletion region by applying a reverse bias voltage, at the same time reduces the concentration of carriers near the PN junction. Thereby, the refractive index of the waveguide is changed and the light can be modulated. The carrier drifts extremely fast at strong electric field in the depletion region, leading in a high modulation rate. A 50 Gb/s Si modulator is shown in Fig. 7(b)[59]. Currently, up to 90 GHz high operation bandwidth is also achieved[60], but at the expense of modulation efficiency[61], while the micro-disk structure PN-type modulator can reduce energy consumption to 0.79 fJ/bit[62].

2.2.3. MOS-type

A MOS structure modulator provides both high modulation efficiency and large modulation bandwidth. A very thin gate oxide layer is interposed between the P and N type Si of the ridge waveguide to form a capacitor structure, as shown in Fig. 7(c)[63]. When a bias voltage is applied, two types of free carrier accumulation occur on both sides of the gate oxide layer, causing a change of refractive index in the waveguide, and thereby obtain a modulated output. The first silic-

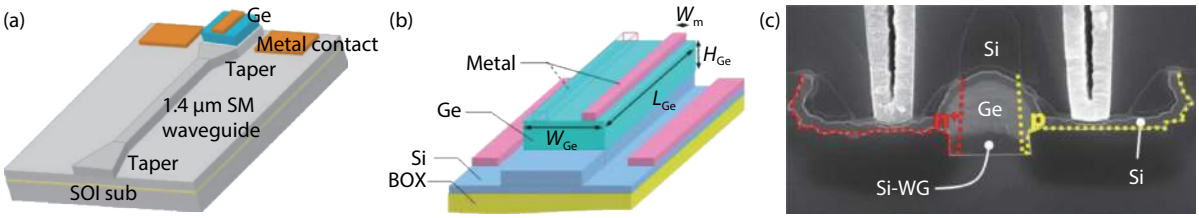

Fig. 8. (Color online) (a) Ridge waveguide PD designed by Intel Corp.[66]. (b) Electrode-biased Ge waveguide PD by Kotura[9]. (c) Ge PD was made by BiCMOS process, which increased the ratio of intrinsic region width to doped region width[68].

on-based high-speed electro-optical modulator was reported by Intel Corp. with a voltage-length product ($V_\pi L_\pi$) as low as 0.2 V·cm and a 40 GHz modulation bandwidth in 2004[15].

2.3. Photodetector (PD)

Due to the inherent characteristics of the band structure, Si has low absorption coefficient and long absorption lengths in the near-infrared band, and it especially does not respond to bands above 1.1 μm. Ge material has attracted great attention to make near-infrared PDs with low dark current, high response and absorption wavelength covering 1.3–1.55 μm because Ge has a large carrier mobility and large absorption coefficient among 1.3–1.55 μm. Its band gap in the single crystal state is 0.67 eV. Additionally, because there is a thermal expansion coefficient mismatch between Ge and Si, tensile stress is introduced in Ge when it is directly grown on Si, which further narrows the Ge band gap. The absorption wavelength of Ge can be extended to 1.87 μm[64, 65].

As shown in Fig. 8(a), researchers in Intel Corp. selectively deposited Ge material on a SOI substrate, which reduces the diffusion length of carriers and lowers the dislocation density[66]. Thus, the bandwidth is increased to 31 GHz and the dark current is greatly reduced. In addition, compared to the planar waveguide[67], the application of the ridge waveguide enhances the optical field limitation in the waveguide and improves the internal quantum efficiency. Finally, the lateral tapers are added to improve the coupling efficiency of evanescent wave coupling between the fiber and single-mode Si waveguide, as well as between Si waveguide and Ge waveguide PDs.

Kotura company considers the influence of the electrode, so they reduce the width of the electrode, put the electrode away from the center of the Ge waveguide, and also increase the thickness of the Ge material[9], as shown in Fig. 8(b). These measures are used to reduce the overlap of the light field and the metal contact part, and the light absorption of the metal is reduced. The PD's responsivity in the 1550 nm band increases to 0.95 A/W, and 3 dB bandwidth reaches 36 GHz under –1 V bias, which is enough to detect 40 Gbps high-speed optical signals.

A horizontal PIN PD with responsivity up to 1 A/W and 70 GHz bandwidth under –1 V bias has also been reported, as shown in Fig. 8(c)[68]. This new structure reduces the epitaxial width of the intrinsic Ge by BiCMOS process. The Ge layer outside the area is protected by the SiN pedestal and the Si waveguide below provides almost constant dopant concentration during ion implantation. Therefore, the carrier diffusion region is reduced, and the ratio of the width of intrinsic region to that of Ge-doped region is thus increased. Finally, the bandwidth and responsivity are increased.

2.4. Muiltiplexer and demultiplexer

DC is used because of its ability to increase bandwidth and lower power consumption[69]. WDM is the key technology to increase the total bandwidth of a transceiver and reduce the assemble cost. WDM usually requires MUX (or DeMUX) to transmit (or receive) optical signals into (or from) an optical fiber. In terms of low optical power penalty and signal wavelength accuracy, it is necessary for MUX and DeMUX to have low insertion loss and flat spectral. Here, we introduce recent published two types of MUX (or DeMUX): 1) delayed Mach-Zehnder interferometers (DMZI) type, 2) arrayed waveguide grating (AWG) type.

2.4.1. DMZI type

The multistage DMZI type (De) MUX is considered to have advantages of low insertion loss, low crosstalk, and spectral flatness. Widening the waveguide width in the DMZI region is an effective way to reduce refractive index change per unit length and keep the filter spectral wavelength nearly constant, both theoretically and experimentally[70]. To further evaluate the influence of the waveguide width in the DMZI region on spectral uniformity, researchers fabricated 1 × 4 channel multistage DMZI with three chips of different waveguide width by using 300 mm SOI wafer scale ArF-immersion lithography process, as shown in Fig. 9(a). For the conventional Chip-A, the waveguide width is set to 0.44 μm whereas that of optimized Chip-B and Chip-C is set to 0.8 and 1.0 μm, respectively. Tapered waveguides are used to connect different width regions in Chip-B and Chip-C. All of three chips exhibited low insertion loss of < 0.2 dB and low spectral crosstalk of < 24 dB. Theoretically, the calculated standard deviation of filter center wavelength of Chip-B and Chip-C is less than half of that of conventional Chip-A, and the experimental result is comparable. Meanwhile, compared to conventional Chip-A with 0.44 μm, the maximum deviation of filter spectral center wavelengths is reduced to 0.32–1.7 nm when waveguide width increases to 0.8 μm. Therefore, this proposed structure would be more practical in high performance WDM silicon photonic transceivers.

2.4.2. AWG type

An AWG (De)MUX consists of two parts: two free propagation regions and an array of waveguides with successive increments in length. The spectral response of conventional AWG channel is Gaussian-like, but a flat spectral response is necessary for many WDM applications. Thus, an AWG integrated with a Multimode Interference (MMI) coupler is designed to satisfy this requirement. On SOI substrate, a high refractive index allows us to reduce the size of waveguides and are beneficial for compact design. However, it makes the design of AWG and MMI coupler difficult because the silicon

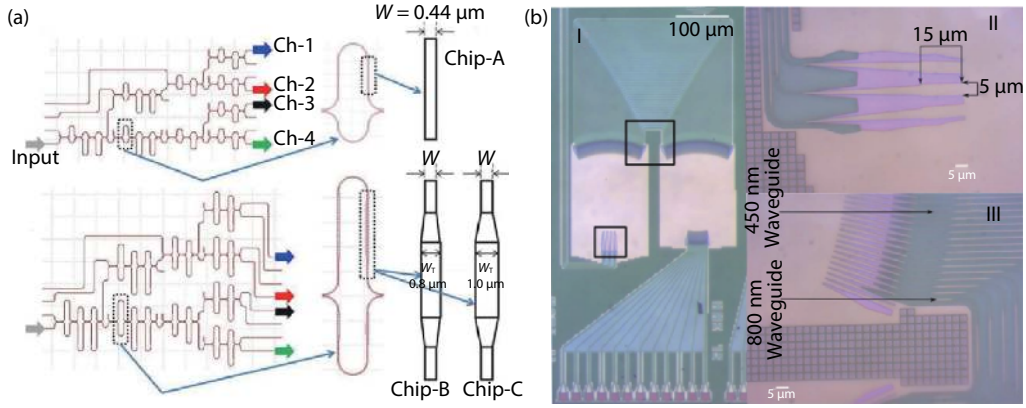

Fig. 9. (Color online) (a) Device structures of 1 × 4 Ch optical (De)MUX with different waveguide width[70]. (b) Microsoft image of fabricated 12 × 400 GHz MMI-AWG[71].

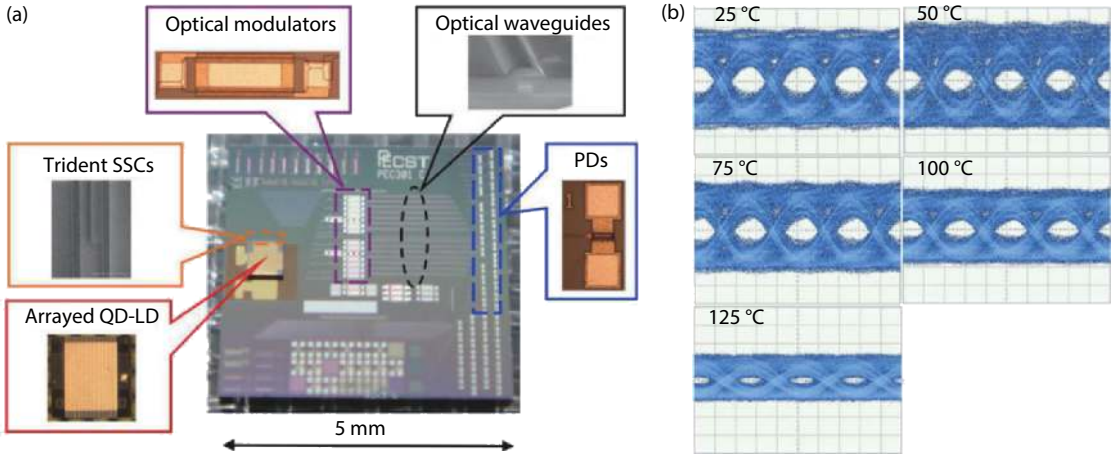

Fig. 10. (Color online) (a) Image of athermal Si optical interposer with close-ups of the components. (b) 20 Gb/s eye diagram with continuous temperature change from 25 to 125 °C[72].

waveguides are sensitive to phase error in the array. In this reference, an optimized design of compact SOI-based 12 channel 400 GHz AWG with MMI is presented[71]. A 15 μm long and 5 μm wide MMI is adopted, because it is suitable for achieving a flat spectral response. Moreover, compared to conventional AWG, the 0.52 aspect ratio of the channel response of the MMI-AWG is improved. This MMI-AWG also presents minimal loss and good crosstalk level with 56 waveguides. The microscopic images of the fabricated 12 × 400 GHz MMI-AWG is shown in Fig. 9(b). This optimized MMI-AWG possess low insertion loss of –3.29 dB, 17 dB crosstalk and average channel spacing of 391 GHz.

3. Silicon photonic transceivers

Because of the rapid development of transceiver applied in DC, there has not been sufficient time to establish standards. Thus, although various solutions for short-distance optical links have been developed, they cannot interoperate. Users and customers do not need to care too much as long as the price is cheap. In this section, we introduce two solutions for short-distance optical interconnect links in DC: 1) parallel single-mode, 2) wavelength division multiplexing and two advanced modulation formats: 3) four-level pulse-amplitude modulation, and 4) coherent optical technology.

3.1. Parallel single-mode

Increasing the number of interconnect channels to increase the total bandwidth is one of the current solutions for high-speed interconnection between chips and boards. A successful PIC short-distance multi-channel interconnection solution is parallel single-mode (PSM) technology. This technology contains multiple fibers or waveguides which transmit the identical wavelength light. Small size, low power consumption, high-speed and stable interconnection thus can be achieved.

Due to their temperature-insensitive and low-RIN characteristics, as mentioned earlier, QD-LDs are very suitable as the light source on Si. High-temperature operation is essential to dense integration. The LDs can be assembled with high-temperature LSICs that generate great heat. The output power of conventional QW-LDs decreases sharply with the increase of temperature while the highest operation temperature of a QD-LD has reached 220 °C[37]. The first athermal Si optical interposer is integrated with temperature-insensitive components, such as monolithically integrated symmetrical structure Mach-Zehnder interferometer (MZI) modulators, Ge PDs with light-dark current ratio greater than 30 dB at 100 °C, as well as hybrid integrated QD-LD array. The QD-LD array has an output power of up to 10 mW in 100 °C and lasing wavelength temperature coefficient of 0.67 nm/K from 25 to 125 °C[72], as shown in Fig. 10(a). Therefore, under high temperature or rapid change temperature environment, the transceiver does not need complicated feedback control circuits. 20 Gb/s

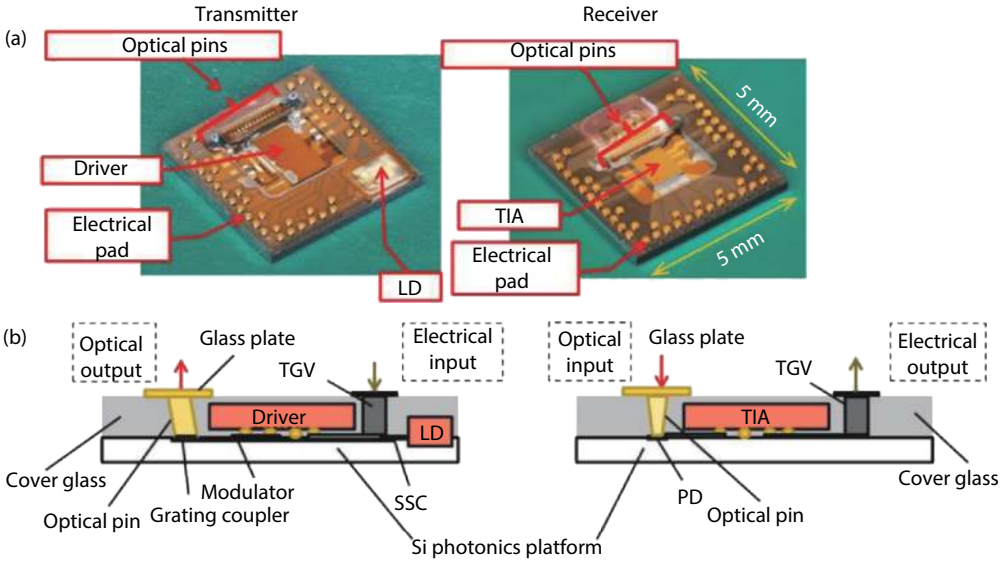

Fig. 11. (Color online) (a) Photographs of the transmitter and receiver optical I/O core. (b) Cross section of the transmitter and receiver optical I/O core[73].

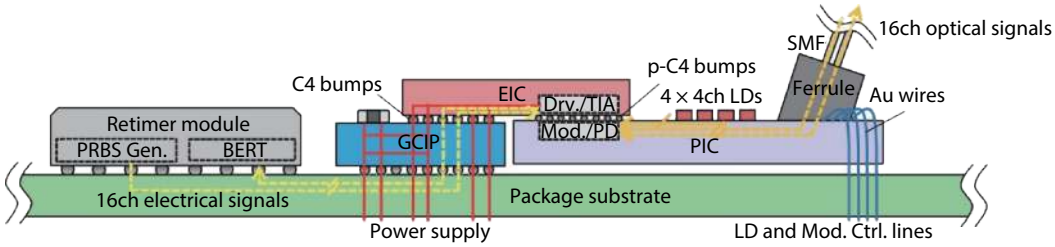

Fig. 12. (Color online) Schematic structure of a 16-channel × 25 Gb/s silicon photonic optical transceiver on a package substrate. EIC and PIC are bonded together by solder bumps and mounted on a glass ceramic interposer (GCIP)[76].

single-channel error-free transmission and 19 Tbps/cm^2 bandwidth density are realized at the temperatures up to 125 °C. Meanwhile, 20 Gbit/s eye diagrams under the different temperatures from 25 to 125 °C are shown in Fig. 10(b).

Researchers at AIO Core have demonstrated a fingertip-size optical module, which has received much attention in recent years[73–75]. All optical/electrical functions are integrated onto a new silicon photonic chip-scale optical TXs and RXs, called optical I/O cores. Various kinds of customized optical transceivers can be formed by attaching optical/electrical components to the I/O core. Therefore, the I/O core can be configured for various optical interconnection systems by combining periphery components and equipment. Fig. 11(a) shows photographs of TX and RX 4ch × 25-Gbps parallel optical I/O cores. The optical I/O core consists of a silicon photonic platform, CMOS LSIC (driver or TIA), a cover glass, optical pins, and through-glass vias (TGVs). At the TX, in addition to these components, 1.3-μm QD Fabry-Perot (FP) LDs integrated with SSCs are mounted in the TX as the light source. MZI modulators adopt MOS-type optical phase shifters and GCs are used for extracting the optical signal from the silicon photonic devices. At the RX, surface-illuminated Ge PIN PDs are connected to TIA and electrical-signal lines for CMOS LSIC are connected through TGVs. The optical signal enters into multimode fibers (MMFs) through the optical pins that are fabricated on the Si platform. By tuning the ultraviolet exposure condition, the optical pins are formed with a taper shape and 8 degrees tilt angle, as shown in Fig. 11(b). Taper shape makes beam size of incident light controlled, and misalignment tolerance against the outer waveguides can be optimized. By applying tilt angle, beam-divergence angle keeps small and generation of higher-order propagation mode at the optical pins is suppressed. This 5 × 5 mm^2 optical I/O cores demonstrated 25-Gbps/ch error-free operation over 300 m MMF with power consumption of 5 mW/Gbps. Applications in active optical cables (AOCs), application-specific integrated circuits (ASICs) and field programmable gate array (FPGA) are expected.

Fig. 12 shows a 400 G high-speed transceiver[76]. It achieves high-density 16-channel × 25 Gb/s with silicon optical interposer at room temperature, and realizes a high bandwidth density of 363 Gb/s/cm^2. In order to suppress the crosstalk loss, the impedance and capacitance of the signal line and power line are carefully designed, thus a low impedance circuit is obtained. The Tx and Rx power wires are separated from the package (PKG) substrate to ensure that Tx power noise does not affect Rx sensitivity.

Schematic diagrams of the EIC and PIC chips are shown in Fig. 13. The EIC chip and the PIC chip are directly flip-chip bonded through solder bumps to minimize the wiring length and parasitic capacitance between electronic circuits and photonic circuits. Thus, the attenuation of electrical signals between PD, driver, and modulator are reduced. At the transmitter, 2 × 8 drivers on the EIC control 2 × 8 PN-type MZI modulators on the PIC. Modulators load the electrical signals gener-

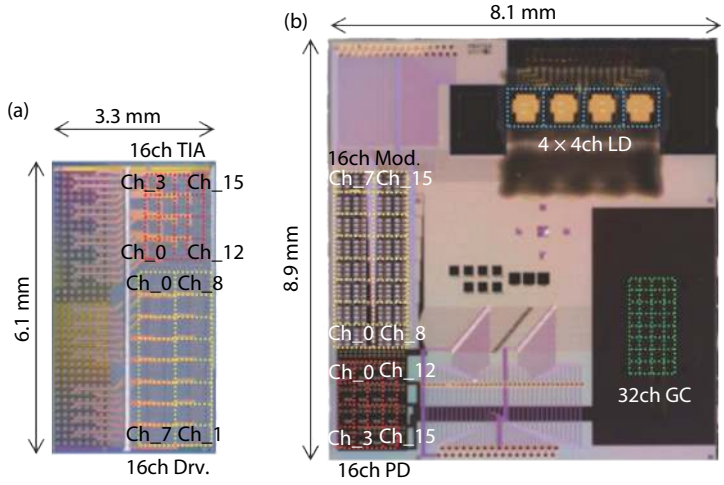

Fig. 13. (Color online) (a) EIC and (b) PIC photographs of a high-density 16-channel optical transceiver[76].

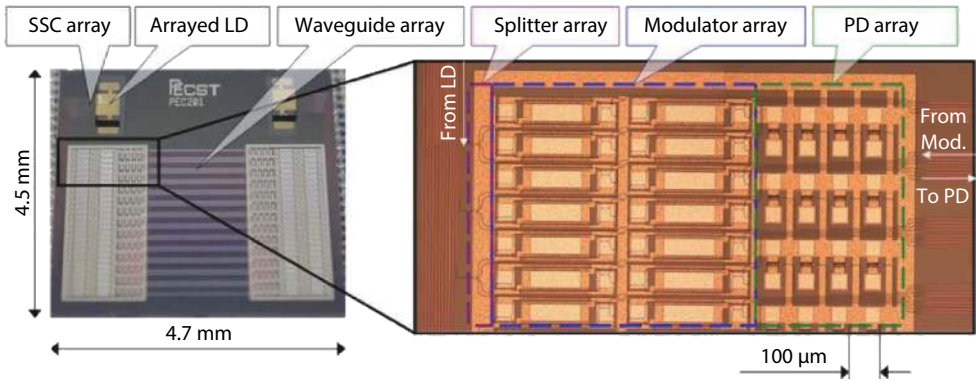

Fig. 14. (Color online) This silicon interposer integrated the beam splitters to increase the number of interconnect channels[57].

ated from pseudo random bit sequence (PRBS) on the output from hybrid integrated 4 × 4 array LDs. The light is efficiently coupled into the SSCs by passive alignment, then fed into an array of 16 GCs and finally coupled into 16 single-mode fibers. At the receiver, optical signals from 16 single-mode fibers are coupled into the PIC waveguide through 16 GCs array, and finally are sent into 4 × 4 PIN-type PD array with responsivity of 0.75 A/W at 1550 nm under −2 V reverse bias voltage. All 32 channels can transmit and receive at the same time with a modulation rate of 25 Gb/s per channel. Besides, the channel crosstalk loss is less than 0.1 dB. Therefore, the transceiver module achieved 400 Gb/s error-free (bit-error ratio (BER) < 10^{-12}) operation.

In Ref. [57], the number of channels is increased by using beam splitters. Multiple divided channels can be modulated and overall bandwidth is improved, as shown in Fig. 14. Two groups of 13-channel array LDs are hybrid integrated on a Si substrate. 26 low optical loss "trident" SSCs, 26 1 × 4 beam splitters, 104 PIN-type modulator array, 104 inter-chip optical waveguides and 104 PIN-type PD array are monolithically integrated. Due to the modulation rate limit of the PIN-type modulator, each channel can achieve a maximum bandwidth of 20 Gb/s. Thus, transceiver of 2.1 Tb/s intra-chips interconnect has been achieved. Because the packaging area of a single channel is 0.0677 mm^2, the bandwidth density reaches 30 $Tbps/cm^2$.

A multi-source agreement (MSA) is made between multiple manufacturers to fabricate inter-compatible products for customers to choose. For example, the 100 G PSM4 is and MSA that was specifically designed for more than 500 m transmission network applications. The purpose of its formulation is to provide a low-cost solution for transmitting 4 × 25 Gbps wavelengths through SSMF outside the IEEE 100 G Ethernet specification. This 100 G PSM4 uses eight SSMFs to form four independent channels, and the speed of each channel is 25 Gb/s.

As shown in Fig. 15[11, 77], Luxtera's generic transceiver architectures of 100 G (4 × 25 G) and 200 G (8 × 25 G) have realized multi-channel transmission by using only one laser and a 1 × 4 (or 8) beam splitter. At the transmitters, the output from off-chip LaMP light source is divided into 4 or 8 channels by the beam splitter. Each channel is separately modulated by an independent MZI, which is driven by an independent driver to maximize the phase shift. The length of the component is minimized and the integration is more compact. For the receivers, due to the use of a polarization-splitting grating coupler (PSGC), waveguide PDs have two separate inputs. Thus, the PDs have a sensitivity advantage from differential coupling. Each channel (Tx/Rx) is able to support 28 Gbps data transmission, thus 100G and 200G transceiver modules are realized.

An external light source is also used in Sicoya's design of 4 × 25 Gbit/s EPIC transceiver chip[78]. The monolithic production process with a co-integration of photonic and electronic

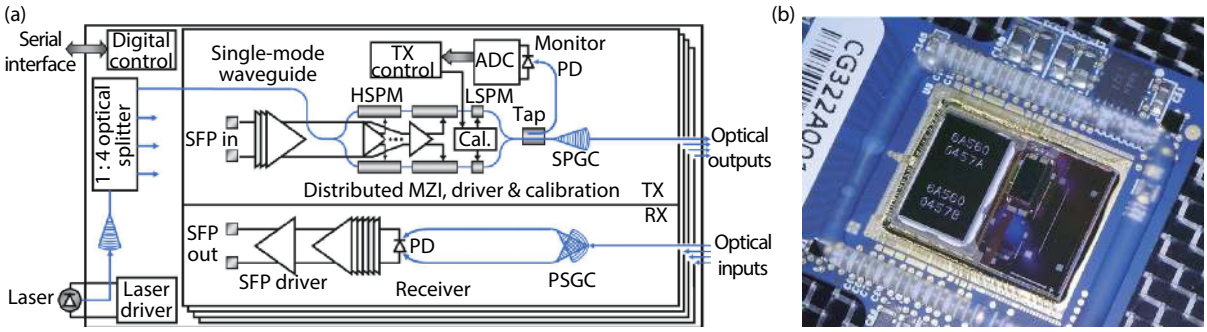

Fig. 15. (Color online) (a) Generic transceiver architecture of the $N\times 25$ G Luxtera product. (b) Photograph of assembled 8×25 G chipset (without fiber array), including: EIC, LaMP and PIC[11].

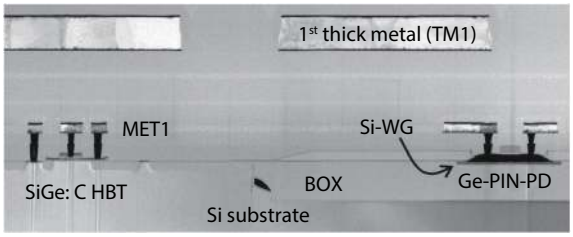

Fig. 16. Cross section of co-integrated optical and electronic structures on the chip[78].

structure is based on the BiCMOS process. This technology includes BiCMOS electrical devices within or over Si bulk area, such as n- and p-doped MOS, high-speed SiGe heterojunction bipolar transistors (HBTs) and Schottky diodes, as shown in the left-hand side of Fig. 16. On the same baseline, photonic structures such as Ge PDs, MZI, node-matched diode (NMD), ring modulators, GCs and waveguides can also be produced on SOI, as shown in the right-hand side of Fig. 16.

A photograph of this EPIC transceiver is shown in Fig. 17(a). The RX block consists of GCs, high-efficiency Ge PDs (shown in Fig. 8(c)), TIA and limiting amplifiers. RX performance strongly benefits from the co-integration of PD and TIA, because the proximity of PD and TIA input allows a strong reduction of parasitic capacitances. Besides, elimination of transmission lines and contact pads results in much lower inductance and capacitance. At 40 Gbit/s using 2^{15}–1 not return to zero (NRZ) PRBS, an error rate of 2.5×10^{-12} was obtained. At the TX, the modulation of the external laser output is achieved by a compact NMD modulator whose p–i–n diode is placed laterally to waveguide resonator[79], as shown in Fig. 17(b). Two 1D-photonic crystals form the mirrors which increase the effective interaction length of the light with the intrinsic region and therefore leads to a compact design. The p^+, n^+ doped areas are located in the nodes of the resonator standing wave to ensure that the lowest possible scattering and absorption from doping can be achieved. The energy consumption of the NMD modulator is determined to be 56 fJ/bit at 25 Gbit/s NRZ coding. Finally, a complete 4×25 Gbit/s EPIC transceiver chip is achieved and SiGe BiCMOS technology is not limited to 25 Gb/s, but can scale up to 50 Gb/s and above.

Commercially, Intel Corp. researchers use 4×25 Gb/s PSM transmission technology[80] to achieve a 100 Gb/s silicon transceiver within 2 km with a maximum power consumption smaller than 3.5 W.

3.2. Wavelength division multiplexing

WDM is another successful short-range optical interconnect solution. Compared with PSM, WDM has the advantage of requiring only two fibers instead of *N*, but its disadvantage is that it requires *N* lasers instead of one. Compared to fiber and installation costs, WDM is more meaningful because the total cost of the transceiver is decreased.

Another MSA is 100 G CWDM4, which is a 100 G transmission solution that is based on coarse wavelength division multiplexing (CWDM). Optical signal transmission is performed by using four center wavelengths of 1270, 1290, 1310, and 1330 nm, and each wavelength transmits 25 Gb/s data. The 100 G CWDM4 module can (de)multiplex the above four center wavelength into a SSMF for transmission through CWDM technology. Intel Corp. presented a high-speed, low consumption and uncooled 4×25 Gb/s silicon transceiver with a CWDM wavelength interval of 20 nm in the 1310 nm band. The transmission distance is up to 10 km and it can be used in DC and 5 G front-haul[81].

Intel Corp. reported the first 8-channel 400 G CWDM silicon optical transmitter[82]. Eight discrete DFB LDs with a 20 nm spectral interval are hybrid integrated. Eight high-bandwidth carrier-depleted PN-type modulators and a Si optical multiplexer are monolithically integrated on the same chip by using Intel's highly integrated wafer-level processing platform. Fig. 18 shows the spectrum of the eight transmitter channels which overlapped with the measured multiplexor (MUX) transmission spectrum, illustrating excellent wavelength targeting of the laser and MUX.

Fig. 19 shows a 16-channel WDM receiver integrated on Si[13]. Si SSCs are integrated on the low loss SiO_x array waveguides (AWG), and are connected to the Ge PD array through the Si waveguide. Crosstalk between channels is lower than –22 dB at a rate of 22 Gb/s per channel, and error-free transmission of 40 km was achieved at a rate of 12.5 Gb/s per channel.

An optical frequency comb mode-locked laser (MLL) with a wide gain spectrum can reduce the dependence of the transmitter on multiple different wavelength lasers. Therefore, the transceiver can avoid integrating multiple light sources[83]. Fig. 20(a) shows an 8-ch × 14 Gbps WDM silicon-based optical transceiver. An external cavity MML is used as the light source. Resonant ring modulators (RRMs), filters and WDM are monolithically integrated. Combination of MLL and RRMs makes transceiver compact. Because each optical frequency comb provides limited power, the InP/InGaAsP quantum well

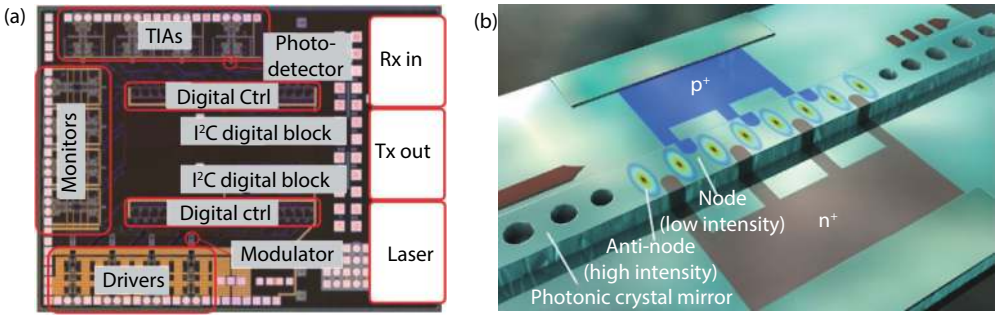

Fig. 17. (Color online) (a) Photograph of Sicoya's EPIC transceiver[78]. (b) Illustration of NMD modulator. Its mirrors are formed by two 1D-photonic crystals, and the p^+, n^+ doped areas are located in the nodes of the resonator standing wave[78].

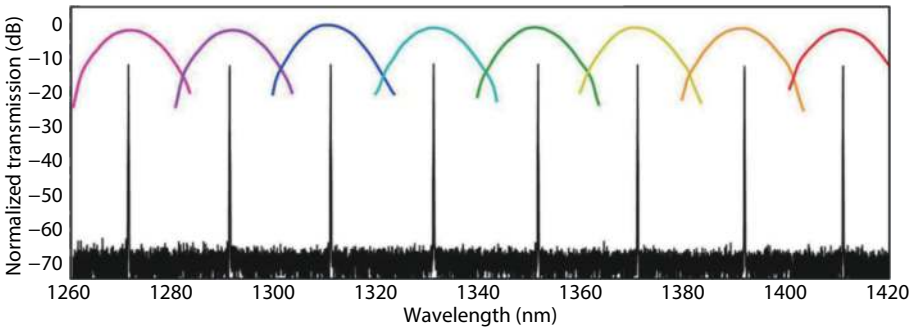

Fig. 18. (Color online) 8 channels of the Si MUX passband overlaid with the normalized output spectra of the CWDM8 transmitter[82].

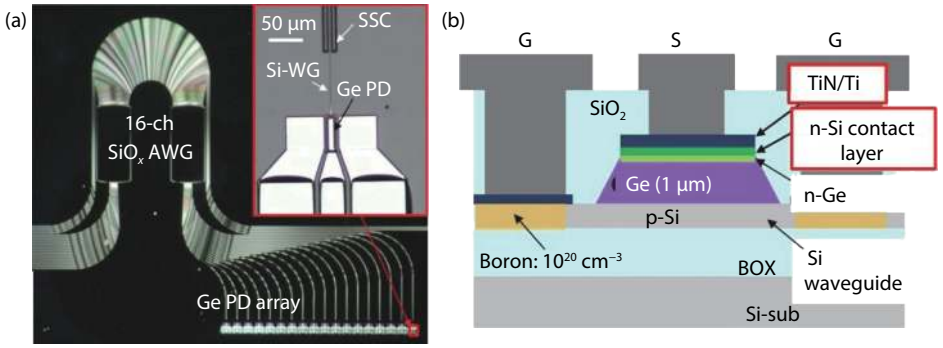

Fig. 19. (Color online) (a) Top view of demultiplexer, 16-ch AWG and Ge PD array. (b) Cross section of Ge PD[13].

semiconductor optical amplifier is used to amplify the optical signal at the output. The Tx transmission spectrum is plotted in Fig. 20(b), together with the filtered MLL spectrum featuring eight selected carriers aligned to the RRMs within the passband of the filter.

Increasing the number of channels for optical communication will inevitably increase the packaging area. The advanced modulation format can increase the total bandwidth by increasing the amount of data carried per baud. Four-level pulse-amplitude modulation (PAM-4)[84], phase division multiplexing (PDM) technology[85], and coherent optical communications[86, 87] have attracted wide attention in recent years and they have gradually been developed.

3.3. Four-level pulse-amplitude modulation

The 100 Gb/s link pluggable modules in DCs (such as the PSM4 and CWDM4 mentioned above) have adopted the NRZ modulation format, which transmits single bit per baud. In comparison, each amplitude in PAM-4 transmits two bits per baud. As the interconnection rate increases from 100 to 400 Gb/s in DCs, PAM-4 direct detection format becomes the standard for DR4 and FR4 modules[88]. A single-channel 53 Gb/s PAM-4 transmission has been achieved within a range of up to 40 km[89]. A 5.02 mW/Gbps low-power PAM-4 transceiver is reported, each channel can transmit up to 64 Gb/s in the short-range (SR) transmission range[90]. SiFotonics has offered an avalanche photodiode (APD) array receiver for the PAM-4 400G DR4/FR4[91].

A novel compact silicon photonics transmitter that uses binary driven GeSi electro-absorption modulators (EAMs) in an interferometer topology has been demonstrated[84]. The topology consists of two intensity modulators in interferometer with 90° phase difference, where the LSB/MSB coding is realized through a 33 : 66 power ratio, as shown in Fig. 21(a). Fig. 21(b) shows a more detailed explanation of the PAM-4 amplitude optical operation using a vector diagram. It is beneficial to reduce power consumption because two NRZ drivers are more energy efficient than one multi-level driver. This transmitter first achieved real-time 64Gbaud PAM-4 transmission over more than 1 km of SSMF in a chip-

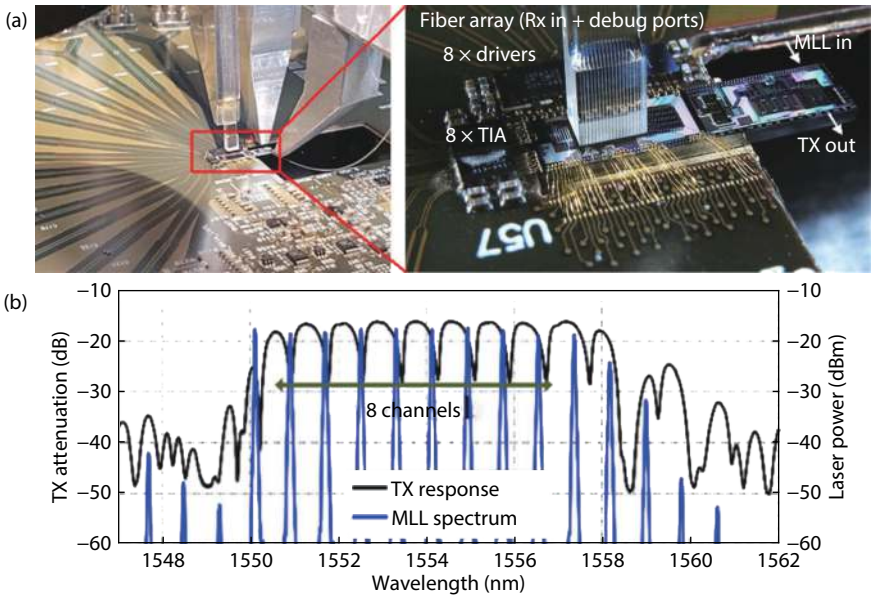

Fig. 20. (Color online) (a) Photograph of transceiver board with optical I/O and only two fibers are used in the fiber array during system test. (b) Tx transmission and filtered MLL spectra at 25 °C and 257 mA showing 8 RRMs aligned within the passband of the filter[83].

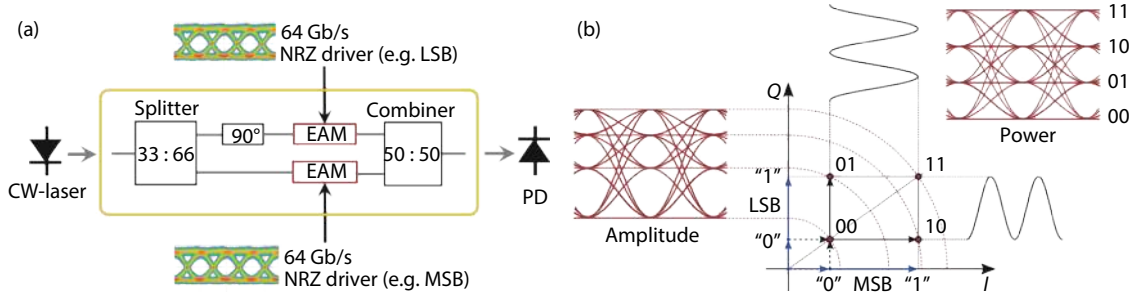

Fig. 21. (Color online) (a) Two-bit optical DAC consisting of two EAMs. (b) Vector and eye diagram of the proposed topology optical PAM-4 generator[84].

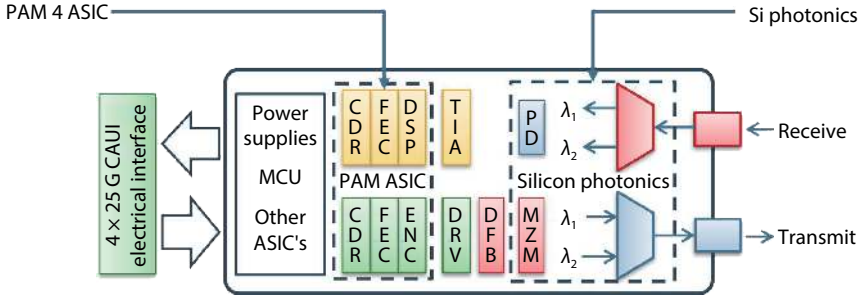

Fig. 22. (Color online) Pluggable QSFP28 module which combine 4 × 25 Gb/s channels into two 50 Gb/s PAM-4 streams[92].

to-chip link without any electrical analog-to-digital converter (ADC), digital-to-analog converter (DAC) or digital signal processing (DSP).

The pluggable QSFP28 module is based on a highly integrated silicon photonic chip and a PAM-4 ASIC[92]. As shown in Fig. 22, four 25 Gb/s signals are input into the main front error correction (FEC) and then combined into two streams of 50 Gb/s PAM-4. Finally, two PAM-4 streams which can transmit 50 Gb/s are obtained.

3.4. Coherent optical technology

In contrast from short-distance transmission, which commonly adopts intensity modulation and direct detection (IM-DD), coherent optical communication is required when it is applied to long-distance communication, such as interconnection between DCs, metro area network and backbone network. Because of the high cost of long-distance optical fiber, enterprises attempt to carry as much information on each optical fiber as possible. Coherent optical communication technology can load information to different characteristics of the light, such as polarization (PDM[85], DP-DQPSK[93]), phase (high-order constellation[94, 95]). These technologies can meet the demands of enterprises.

Acacia demonstrated a silicon-based PIC which integrated a complete vector modulator and coherent transceiver

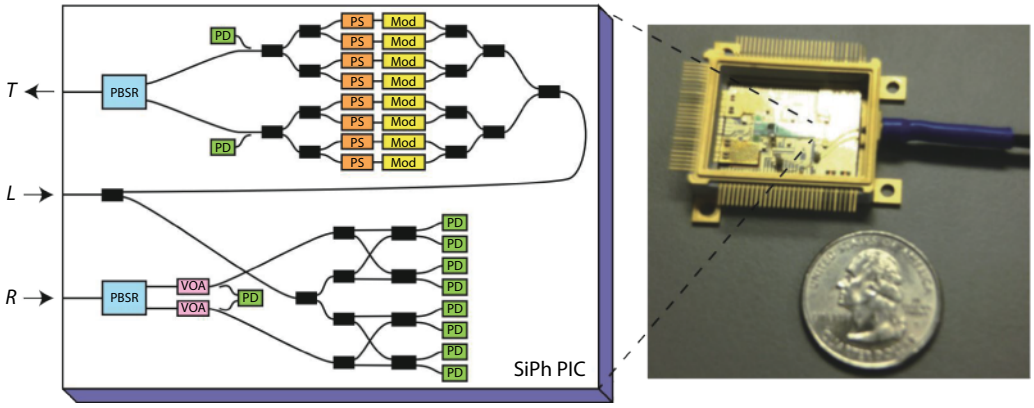

Fig. 23. (Color online) Block diagram of silicon photonic coherent PIC demonstrated by Acacia[86].

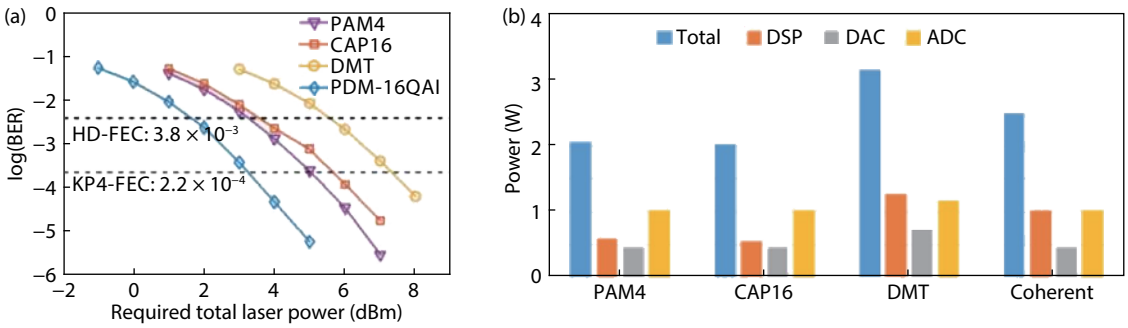

Fig. 24. (Color online) (a) BER against required total laser power for coherent and IMDD systems. (b) Estimated ASIC power consumption for PAM4, CAP16, DMT and coherent schemes based on 5 nm CMOS[96].

on a 2.7 × 11.5 mm² single chip[86], as shown in Fig. 23. The module is connected to three optical fibers: a laser input which is distributed between the transmitter and receiver, a transmitter output, and a receiver input. Three fibers are packaged in a gold box with four drivers and four transimpedance amplifiers without any temperature control in the range of –5 to 80 °C. The total power consumption is 4.5 W. Finally, a single-chip 100 Gb/s coherent transceiver in silicon photonic is implemented, which includes all necessary optics except light source.

Researchers in Alibaba experimentally evaluated the performance of 400 G coherent and IMDD transceivers for DC optical interconnection[96]. Fig. 24(a) shows the relationship between the BER and required total laser power, which demonstrates that PDM-16QAM has the best performance with the lowest total laser power at the same BER. In addition to performance, the ASIC power consumption also needs to be evaluated. For short-distance interconnection in DC, the coherent DSP complexity would be reduced. Besides, the ASIC power consumption is expected to decrease substantially with rapid development of CMOS technology. The ASIC power consumption at 5 nm CMOS technology for coherent and IMDD systems are estimated, as shown in Fig. 24(b). This scheme illustrates that the ASIC power consumption of coherent system is comparable to those of IMDD systems, and it is a little bit higher than that of PAM-4 system at an acceptable level. These results indicate that coherent optical communication has a huge potential of low cost and high energy efficiency in application for short and medium distance interconnection in DCs in the future.

4. Conclusion

For present DCs, it is technically important to increase the speed of transceivers, as well as to reduce their cost and power consumption. The optical interconnects technique is necessary for the further development of the information age, it also provides enormous bandwidth and low power consumption. Silicon photonics transceivers would take advantage of the high integration, high reliability, and low cost of the CMOS process platform to create high bandwidth, low delay, and low power consumption photonic components. The high-speed transceivers for DCs are significantly optimized in cost and performance. Optical interconnects based on VCSEL and MMF dominate short range (< 300 m) optical links thanks to their low cost, technical simplicity, and low power consumption. Edge emitting LD plays a significant role when distance beyond this range. The various LDs integration schemes have their own coupling methods. Meanwhile, due to its unique excellent characteristics, the QD-LD has shown great potential as light sources on Si, whether to adopt bonding method or monolithic integration. We believe that QD-LDs directly grown on Si would be the last piece of the puzzle of monolithic integrated silicon photonic chip. Three types of Si modulator have their own merits and drawbacks, and a suitable one can be used according to the application. Ge PD is more suitable for silicon photonics than Si, and the PIN configuration is currently the most commercially successful. Utilizing the spatial multiplexing capability of light, WDM technology further increases the transmission speed of the transceiver and a single fiber. At present, PSM and WDM technology implemented with NRZ modulation format are the

mainstream in 100 G transceiver modules. Due to their ability to transmit multiple bits per baud per channel, PAM-4 modulation and coherent optical communication technology would play significant roles in 400 G and 1 TB transceiver modules in the future, as long as the performance and cost can be optimized. These transceiver modules also require their DSPs to develop better structures and algorithms to reduce the bit-error rate and the power consumption.

Acknowledgments

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