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Journal of Semiconductors
(2020) 41, 012101
doi: 10.1088/1674-4926/41/1/012101

Surface traps-related nonvolatile resistive switching memory effect in a single SnO_2:Sm nanowire

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Abstract: For nanostructure SnO_2, it is very difficult for its electric properties to accurately control due to the presence of abundant surface states. The introduction of Sm can improve the traps in surface space charge region of SnO_2 nanowires, resulting in a controllable storage charge effect. For the single nanowire-based two-terminal device, two surface state-related back-to-back diodes are formed. At a relatively large voltage, electrons can be injected into the traps in surface space charge region from negative electrode, resulting in a decrease of surface barrier connected with negative electrode, and contrarily electrons can be extracted from the traps in surface space charge region into positive electrode, resulting in an increase of surface barrier connected with positive electrode. The reversible injection and extraction induce a nonvolatile resistive switching memory effect.

Key words: nanowire; surface state; trap; memory effect

Citation: H Y Zhou, H P Shi, and B C Cheng, Surface traps-related nonvolatile resistive switching memory effect in a single SnO_2:Sm nanowire[J]. *J. Semicond.*, 2020, 41(1), 012101. http://doi.org/10.1088/1674-4926/41/1/012101

1. Introduction

For one-dimensional (1D) nanostructure semiconductors, a large number of dangling bonds can be formed owing to the damage of the lattice periodicity on their surfaces, and accordingly surface states are generated[1, 2]. These surface states will have a strong impact on the performance of nanostructures[3–11]. In addition, quantities of impurity, interstitial atom, and vacancy defects exist in lattice, forming different energy levels. For the defects of deep energy levels, they can generally capture and store charges, resulting in the formation of traps. For the traps, their filling degree will intensively affect their electric transport. For surface traps, moreover, the filling and emptying of charges can be controlled by external stimuli, such as acoustic, optical, electrical, magnetic and heating, thereby obtaining unique properties that are different from those of bulk materials[12–14]. When constructing a two-terminal nanodevice, in addition, a large number of surface states will form two back-to-back connected diodes at the interfaces between semiconductor material and two metal electrodes, and moreover the barrier of surface state-related diodes can also be adjusted at both ends, which will have a great impact on the performance of nanodevices[15–18]. Therefore, the modulation of the surface states of nanosemiconductors has become a hot issue in the field of nanodevices.

For wide bandgap semiconductor, the difference of electronegativity between anion and cation ions can lead to the existence of anion vacancies. These vacancies level may be very deep, resulting the formation of traps which can capture and store charges. The performance of electron transport is intensively determined by the filling and emptying of traps as well, and thus, abundant surface states and traps will play a vital role in the physical properties of nanostructures[19–22]. To meet the demand in device function, it is imperative to tailor the properties by designing trap-related surface states of nanostructures[23–25] or modulating the surface barrier[26–28].

For the nanostructures with large specific surface area, their surface free energy is relatively high. It is very easy for doped ions to segregate on the surface to reduce free energy. The segregated doping ions can adjust the structure of surface defects, which may improve the surface-related performance of nanostructures[29–31].

Here, Sm, served as a dopant, was introduced in nanostructure SnO_2. It can improve the traps in surface space charge region, resulting in a controllable storage charge effect. At the two ends connected with electrodes, their surface barriers can be reversibly modulated by the injection and extraction of electrons in the traps located in surface space charge region. A nonvolatile resistive switching (RS) memory can be obtained effectively.

2. Experiment

2.1. Sample preparation

SnO_2:Sm nanowires were synthesized by an in-situ chemical vapor reaction. First, $Sn(NO_3)_4$ and $SmCl_3$ were dissolved in deionized water. Then, a proper amount of citric acid and ethylene glycol was added to the solution. After the solution was stirred for 1 h, it was placed in an oven at 80 °C to form a sol. Subsequently, the gel was polymerized at 150 °C for 10 h. The solid resin was prepyrolyzed at 400 °C to form a Sn–Sm–C–O composite precursor.

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Received 8 OCTOBER 2019; Revised 28 OCTOBER 2019.

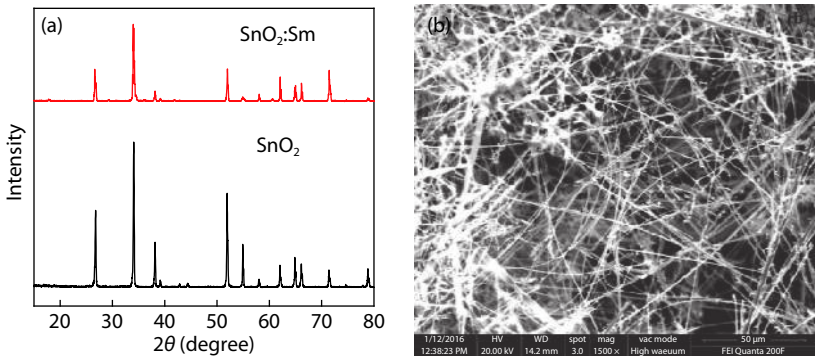

Fig. 1. (Color online) Structure and morphology characterization of as-synthesized product. (a) XRD pattern. (b) FESEM image.

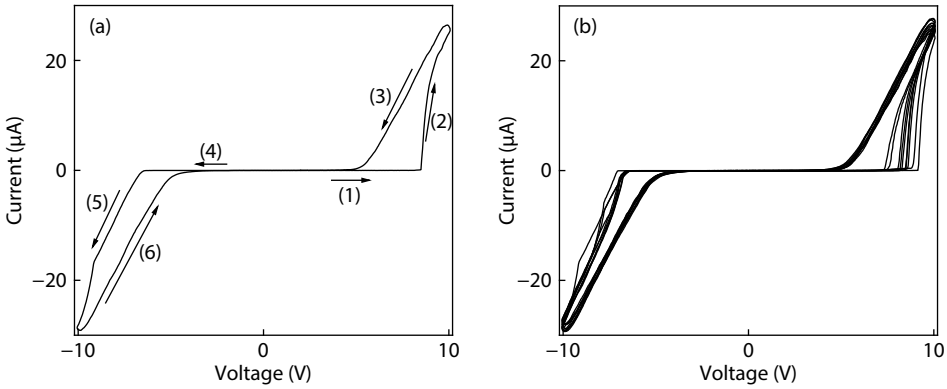

Fig. 2. *I*–*V* characteristics of an individual SnO_2:Sm nanowire-based two-terminal device at 10 V bias voltage. (a) Typical *I*–*V* cyclic curve. The numbered arrows 1–6 indicate the direction of voltage sweeping. (b) 10 consecutive *I*–*V* cyclic curves, showing an excellent stability and repeatability.

The resulting precursor mixture was ground, and transferred to a small ceramic boat. Then, the ceramic boat is placed in the middle of a tubular furnace. After that, the tube furnace was heated to 1200 °C and kept for 2 h under N_2 atmosphere. After reaction, the tubular furnace is cooled to room temperature. The white cotton-like product was obtained.

2.2. Characterization

The structure and morphology of as-synthesized product was characterized by X-ray diffraction (XRD; RIGAKU D/max-3b), and field emission environmental scanning electron microscopy (FESEM, FEI Quanta 200F), respectively.

2.3. Fabrication and electrical measurement of device

For the preparation of device, a single SnO_2:Sm nanowire was transferred on an insulation substrate and then Ag electrodes were fabricated at two ends by semi-dried silver paste. Subsequently, a post-annealing was required to minimize the contact resistance under high pure N_2 atmosphere at 400 °C for 10 min. Finally, the devices were packed by polydimethylsiloxane (PDMS). The electrical measurement was performed using a synthesized function generator (Stanford Research System Model DS345) and a low-noise current preamplifier (Stanford Research System Model SR570).

3. Results and discussion

The structure and morphology of as-synthesized product were analyzed by XRD and FESEM, respectively, as shown in Fig. 1. In Fig. 1(a), all the diffraction peaks can be indexed to tetragonal rutile structure of SnO_2, which is highly consistent with the standard PDF card [41-1445]. No impurity peaks were found in the diffraction patterns. From Fig. 1(b), it can be seen that the prepared sample is a non-smooth linear structure with a diameter of about 300 nm to several microns and a length of several hundred to several millimeters, indicating that wire-like one-dimension nanostructures are obtained.

To study the resistance properties of SnO_2:Sm nanowires, *I*–*V* characteristics of a single nanowire were measured at 10 V bias voltage, as ascribed in Fig. 2. Fig. 2(a) shows a typical *I*–*V* cyclic curve. It can be seen that the device current is very small at a relatively low bias voltage, indicative of a non-conductive state. When the externally applied voltage increases to the set voltage of device, the output current suddenly increases at a voltage of about 7–8 V, and correspondingly the resistance changes from high resistance state (HRS) to low resistance state (LRS). When the voltage increases in backward direction, the same phenomenon appears as well. The *I*–*V* curve presents two symmetrical hysteresis loops with counterclockwise circulation in forward and backward directions. The device exhibits typical RS behavior at 10 V cyclic sweeping bias voltage. Fig. 2(b) shows that 10 consecutive *I*–*V* cyclic curves at 10 V bias voltage. It can be seen that the *I*–*V* curves have an excellent stability and repeatability.

For the stage curve before and after current mutation, it is fitted by Fowler-Nordheim (FN) tunneling mechanism[32, 33], as ascribed in Fig. 3. For the curve before current mutation, it increases gradually between $\ln(I/V^2)$ and $1/V$, indicating a direct tunneling mechanism, and the device is an HRS. For the curve after current mutation, however, it decreases. Moreover, a linear relationship can be obtained between

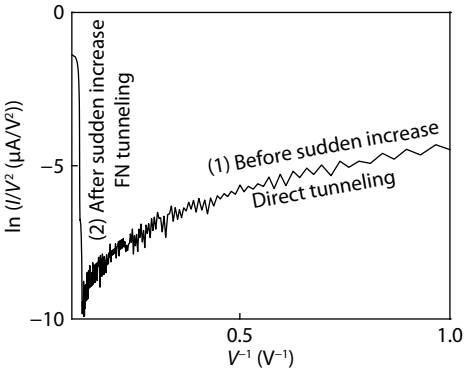

Fig. 3. For the step (1) and (2) curve in Fig. 2(a), the fitted plot by FN tunneling mechanism.

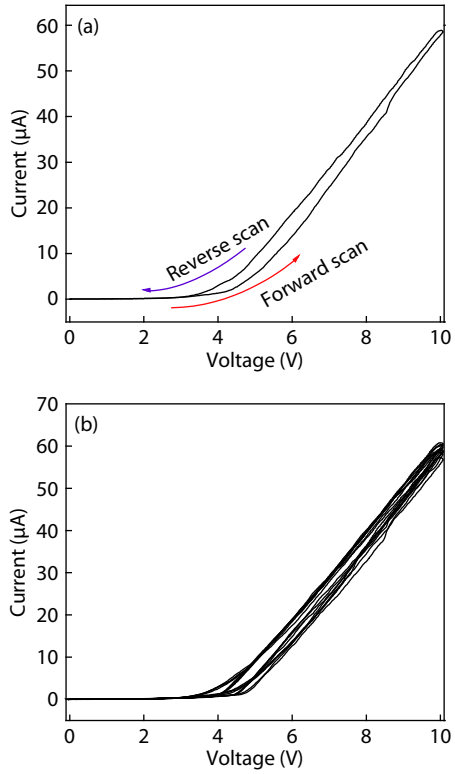

Fig. 4. (Color online) Under only unidirectional voltage sweeping at a forward-biased bias from 0 to +10 V, *I*–*V* characteristics of an individual SnO_2:Sm nanowire-based two-terminal device. (a) One typical *I*–*V* cyclic curve. (b) 10 consecutive *I*–*V* cyclic curves.

$\ln(I/V^2)$ and $1/V$. Therefore, it is a typical FN tunneling mechanism, and the device have transited into an LRS.

To further verify the relationship between RS properties and voltage polarity, the electric transport of a single nanowire-based device was measured by a unidirectional forward-biased sweeping voltage from 0 to +10 V, as illustrated in Fig. 4. It can be seen that the current varies monotonously with voltage, and the current mutation and hysteresis loop vanishes. Moreover, the back-and-forth curves can basically coincide. In addition, the threshold voltage of current increase is only about 4 V, which is lower than that of bidirectional sweeping. This result indicates that the hysteresis loop can appear only when a relatively large bidirectional sweeping voltage is applied.

To verify the hypothesis that the hysteresis loops come from the large reverse bias-induced polarity, the electric transport of a single nanowire-based device was further measured at a relatively low bias voltage of 2 V, as represented in Fig. 5. It can be seen that the back-and-forth curves can completely coincide. For the current mutation and hysteresis loop effect, neither do they appear as well. For the threshold voltages, moreover, there is a difference between forward and backward directions.

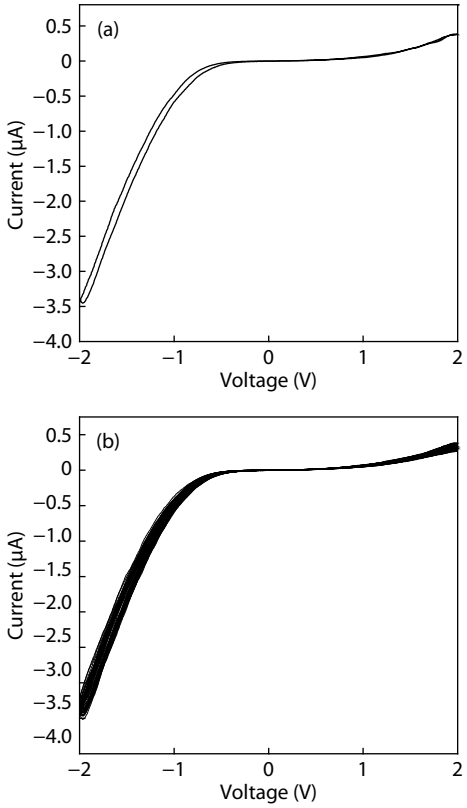

Fig. 5. *I*–*V* characteristics measured at a relatively low bias voltage of 2 V. (a) One *I*–*V* cyclic curve. (b) Consecutive 80 *I*–*V* cyclic curves, showing a superior repeatability.

At a relatively large cyclic bias voltage, the existence of two symmetric hysteresis loops indicates that the device has an RS feature. To investigate the RS-related memory characteristics of the individual nanowire-based device, the reading, writing and erasing performance were tested by continuous cycles, as shown in Fig. 6. The purple curve represents the loaded voltage, and the red curve corresponds to the response of current. Fig. 6(b) shows a magnified view of the dotted line frame in Fig. 6(a) which can reveal a detailed reading, writing and erasing process. The reading, writing and erasing voltages are set as +6.5, +10 and −10 V, respectively. After being applied +10 V voltage, the device resistance decreases at +6.5 V reading voltage, and conversely it increases after being applied −10 V voltage. The on/off ratio of the device current is about 230 at the reading voltage of 6.5 V. In addition, the transition speed is very fast between LRS and HRS.

To further verify the reading-writing-erasing ability of the device, +7 V reading voltage was selected for comparison, as shown in Fig. 7. The response law is the same as the above experimental result shown in Fig. 6. However, the on/off ratio of current can achieve about 940, indicating that the device has a better memory windows at 7 V reading voltage.

To verify the difference of device resistance at +7 V reading voltage after being applied +10 and −10 V, respectively, two different consecutive pulse voltages of (+7)–(+10) and

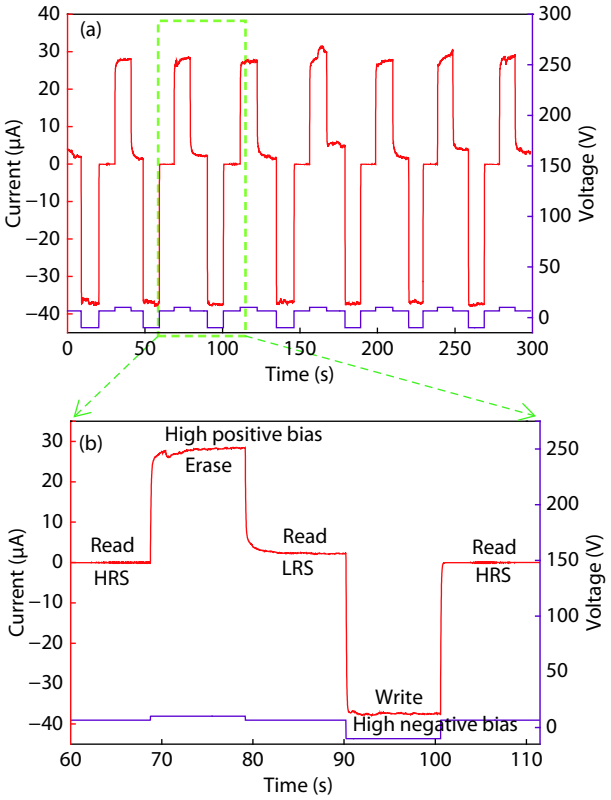

Fig. 6. (Color online) Memory properties of a single nanowire-based device. (a) 7 consecutive writing-reading-erasing-reading cycles, where +6.5, +10, and −10 V are selected as reading, writing and erasing voltage, respectively. (b) An enlargement of a dotted frame in (a).

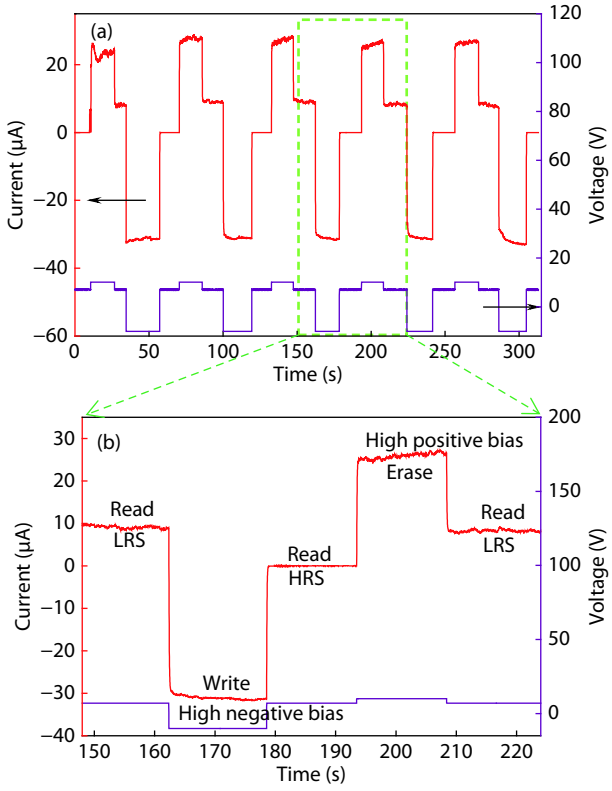

Fig. 7. (Color online) Memory properties of a single nanowire-based device. (a) 7 consecutive writing-reading-erasing-reading cycles, where +7, +10, and −10 V are selected as reading, writing and erasing voltage, respectively. (b) An enlargement of a dotted frame in (a).

(+7)–(−10) V were applied to test the device resistance, as shown in Fig. 8. As seen from Fig. 8(a), the device resistance is about 16 MΩ at +7 V voltage when (+7)–(+10) pulse voltage is applied. As seen from Fig. 8(b), however, the device resistance is about 4.2 MΩ at +7 V voltage when (+7)–(−10) pulse voltage is applied. Their resistances exist obvious difference at the same reading voltage after being applying a relatively large voltage with opposite direction. The results can further reveal that the device presents an LRS at a relatively low reading voltage after a relatively large bias voltage is given with the same direction, and contrarily it shows an HRS after a relatively large bias voltage is given with an opposite direction.

To investigate the stability of SnO_2:Sm nanowires memory effect, the HRS and LRS currents of device are continuously monitored at 6.5 V reading voltage, respectively, as shown in Fig. 9. It can be seen that, the HRS and LRS currents can both show a good stability after 3000 s, which firmly proves that the device has a good nonvolatile memory performance.

For SnO_2 nanowires, there are affluent surface states due to the interruption of lattice periodicity on their surfaces. Due to the electronegativity difference between Sn and O, moreover, lots of oxygen vacancies exist in SnO_2 lattice, and therefore SnO_2 presents n-type conductivity. For the wide bandgap SnO_2, the energy level of oxygen vacancies is relatively deep, and therefore they can serve as traps centers, which can capture and store charges. Due to the existence of surface states, surface space charge region is depleted, and correspondingly the traps located in surface space region are emptied. For a single nanowire-based two-terminal device, two surface state-related back-to-back diodes are formed. At a relatively low operation bias voltage, the device is both reverse-biased for the diode connected with negative electrode, and hence it is nonconductive. With increasing operation voltage, electrons can be injected into traps located in surface space charge region from negative electrode, resulting in a decrease of surface barrier height connected with negative electrode. As a consequence, the device can conduct at a relatively large voltage. On a contrary, the electrons can be extracted from traps in surface space region into positive electrode at a relatively large operation voltage, resulting in an increase of surface barrier height connected with positive electrode. At room temperature and low operation, the trapped electrons in surface space charge region cannot be excited and injected spontaneously, and hence the modulated surface barrier height can be maintained. If a relatively low forward voltage is loaded, subsequently, the diode with a low barrier is reverse-biased, and conversely the diode with a high barrier is reverse-biased if a relatively low backward voltage is loaded. After being applied a relatively large bias, therefore, the device resistance is lower when a low forward reading voltage is loaded than that being loaded a low reverse reading voltage. After being applied a relatively large bias voltage, the sustainable asymmetry of surface barrier height leads to nonvolatile RS properties. If a relatively large reverse bias voltage is loaded, electrons can be injected into traps when the height of energy band tilting induced by electric field surpasses that of trap barrier, resulting in a reverse injection and extraction. Therefore, *I*–*V* curves can show

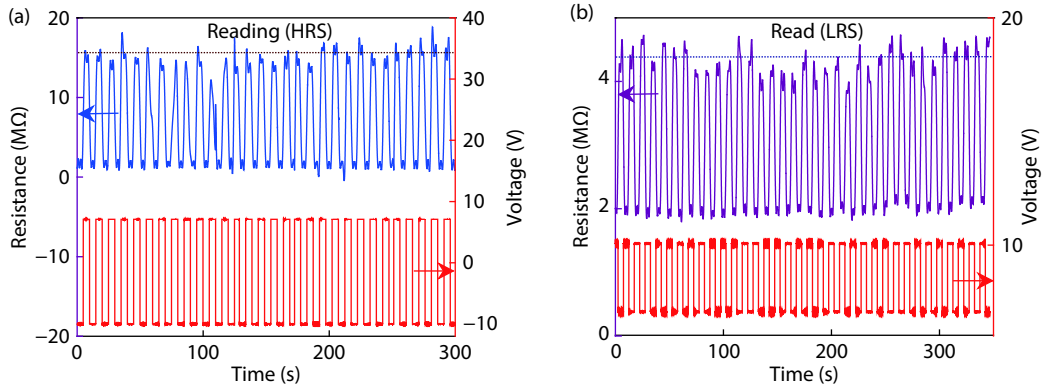

Fig. 8. (Color online) Under different pulse voltages, the response curves of the device current. (a) Consecutive pulse between +7 and +10 V. (b) Consecutive pulse between +7 and −10 V.

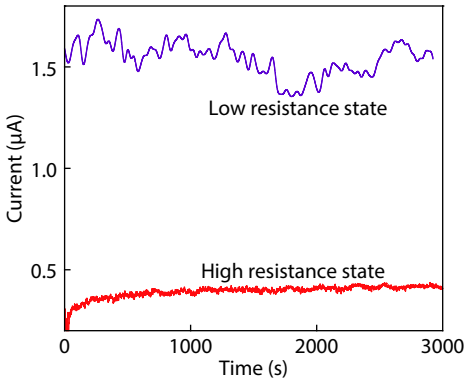

Fig. 9. (Color online) Stability of device current in LRS and HRS at a reading voltage of 6.5 V.

a sudden increase companied with hysteresis loop. For the two-terminal device, the effect is reversible, and *I*–*V* curves can show two almost symmetrical hysteresis loops at forward and backward directions. For pure SnO_2, surface states are complex, the nonvolatile memory effect is relatively poor. When Sm dopants are introduced into SnO_2 lattice, they can easily segregate on the surface to reduce surface free energy. Moreover, Sm can exist in +3 and +4 valence. The introduction of Sm can effectively improve the traps in surface space charge region, resulting in a relatively excellent nonvolatile RS memory effect.

4. Conclusion

In summary, SnO_2:Sm nanowires were prepared by an in-situ chemical vapor reaction. The introduction of Sm can improve the traps in surface space charge region. For a single nanowire-based two-terminal device, two surface state-related back-to-back diodes are formed. At a low operation bias voltage, it is nonconductive. At a relatively large voltage, however, electrons can be injected into the traps in surface space charge region from negative electrode, resulting in a decrease of surface barrier connected with negative electrode, and contrarily electrons can be extracted from the traps in surface space charge region into positive electrode, resulting in an increase of surface barrier connected with positively electrode, and contrarily electrons can be extracted from the traps in surface space charge region connected with positive electrode. The electrons in traps cannot be injected and extracted spontaneously at a relatively low operation bias voltage and room temperature. The sustainable asymmetrical surface barrier, triggered by a relatively large bias voltage, leads to a nonvolatile RS memory effect.

Acknowledgements

This work was financially supported by the National Natural Science Foundation of China (No. 51571107) and the Key Project of Hunan Provincial Department Education (No. 17A222).

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