REVIEWS

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Reducing the power consumption of two-dimensional logic transistors

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Abstract: The growing demand for high-performance logic transistors has driven the exponential rise in chip integration, while the transistors have been rapidly scaling down to sub-10 nm. The increasing leakage current and subthreshold slope (SS) induced by short channel effect (SCE) result in extra heat dissipation during device operation. The performance of electronic devices based on two-dimensional (2D) semiconductors such as the transition metal dichalcogenides (TMDC) can significantly reduce power consumption, benefiting from atomically thin thickness. Here, we discuss the progress of dielectric integration of 2D metal–oxide–semiconductor field effect transistors (MOSFETs) and 2D negative capacitance field effect transistors (NCFETs), outlining their potential in low-power applications as a technological option beyond scaled logic switches. Above all, we show our perspective at 2D low-power logic transistors, including the ultra-thin equivalent oxide thickness (EOT), reducing density of interface trap, reliability, operation speed etc. of 2D MOSFETs and NCFETs.

Key words: 2D materials; dielectric integration; interface; NCFETs; subthreshold slope; low power

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1. Introduction

The gradual geometrical scale down of logic devices has successfully approached the ultimate performance of silicon transistors in the past 60 years[1]. In state-of-the-art technology node, more and more additional performance boosters are introduced into the processes for higher performance and lower power consumption[2–4]. However, with the process complexity increasing and the ultimate scale approaching, the undesirable phenomena such as increasing leakage current and subthreshold slope (SS) induced by short channel effect (SCE) cannot be suppressed through new process alone[5]. The International Technology Roadmap for Semiconductors (ITRS 2.0) indicates that new materials beyond silicon will be an effective route towards continuing the scale and address the formidable challenges of transistor scaling after 7 nm technology node, the so-called "More Moore" approach[6].

2D semiconductors, especially transition metal dichalcogenides (TMDC), have a satisfied thickness-dependent bandgap of 1–2 eV, which can enable lots of fascinating device applications in field-effect transistors (FETs) with the extraordinary on/off current ratio (> 10^8) and off-state current (< 1 pA), and atomically thin body thickness, which gives new opportunities to improve gate control and reduce the SCE main issues in ultra-scaled devices[7–12].

The static and dynamic power consumption of logic transistors are proportional to operating voltage (V_{dd}) and quadratic of V_{dd}, respectively[11, 13, 14]. Therefore, reducing the operating voltage will effectively shrink the power consumption[14].

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More directly, on the device level, the reducing SS to realize steeper switch will translate into reduction of V_{dd}.

$$\mathrm{SS} = \ln 10\frac{kT}{q}\left(1+\frac{C_{it}}{C_{ox}}\right) = 60\left(1+\frac{C_{it}}{C_{ox}}\right), \quad (1)$$

According to the Boltzmann tyranny, the SS of MOSFETs at room temperature will not be lower than $\ln 10\frac{kT}{q} \approx$ 60 mV/dec[15]. From the Eq. (1) of the mathematical analysis of SS, the main strategies to reduce SS for metal–oxide–semiconductor field effect transistors (MOSFETs): (1) to enhance the dielectric capacitance (C_{ox}) of the device; (2) to improve the interface quality and suppress the interface capacitance (C_{it}), thereby to achieve a near-ideal SS (60 mV/dec at room temperature). Recently, some researches have shown that intrinsic ferroelectrics can provide negative capacitance during the switching process between two polarization states and importantly, with the matching of capacitance, the switching barrier could be lowered. Referring to Eq. (1), a negative capacitance could lower $\left(1+\frac{C_{it}}{C_{ox}}\right)$ below 1, make a sub-60 SS, and thus, improve the energy efficiency of conventional electronics just beyond fundamental limit of Boltzmann tyranny[16, 17]. So far, negative capacitance field effect transistors (NCFETs) using ferroelectric as gate dielectric have demonstrated extraordinary performance of steep SS down to 20 mV/dec[16, 18]. However, the research of NCFETs is still in infancy, while the physical origin of NC effect is still controversial, and the researches on device speed and reliability are still way off.

Here, we will summarize the latest progress of 2D low-power logic transistors from the following aspects. First, we will give a brief discussion of the ultra-thin dielectric integration on 2D TMDC, together with analysis of interface quality from different interface passivation. Then, novel NCFETs will

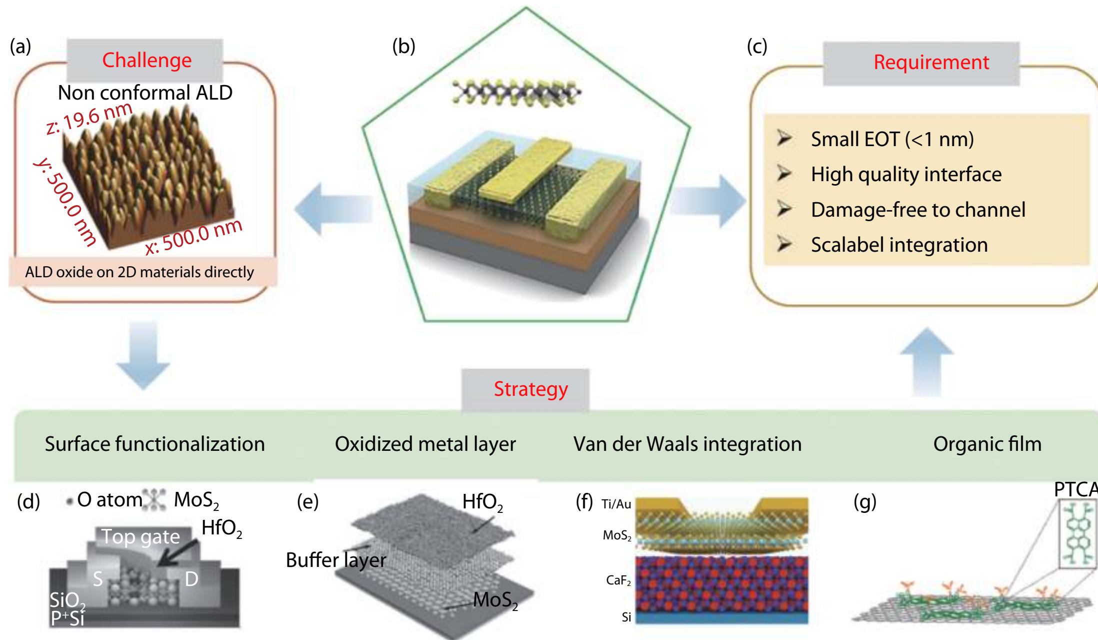

Fig. 1. (Color online) Integrating ultra-thin high-κ dielectric on 2D materials. (a) The 3D AFM image of HfO_2 deposited directly on MoS_2 by ALD technique forms an island structure[26]. (b) Schematic of top gate FET based on monolayer 2D TMDC[7]. (c) Requirement of high-κ dielectric on 2D materials for low power device; (d) Device schematic of the top-gated MoS_2 FET with HfO_2 dielectric deposited by ozone pretreatment[31]. (e) Structural schematic of few layer MoS_2 covered with the metal oxide buffer layer and HfO_2 film[33]. (f) Illustration of the atomic structure of the bilayer MoS_2 FETs with a CaF_2 gate dielectric[35]. A quasi-van der Waals interface is formed between the F-terminated CaF_2 (111) and the MoS_2 channel. (g) PTCA coated graphene. PTCA selectively adheres to graphene on SiO_2 surfaces, providing binding sites for ALD deposition. Inset is a top view of PTCA structure[38].

be discussed, including the working mechanism and device progress. Moreover, a perspective for sub-1 nm EOT and NCFETs will be discussed in the last paragraph of the corresponding section.

2. Integration of ultrathin dielectric on 2D materials

In the early days of the semiconductor industry, SiO_2 has been used as a gate dielectric of MOSFETs for decades due to nearly ideal interface between Si and SiO_2[19]. As logic transistors scaling down, the thickness scales SiO_2 has steadily decreased to 2 nm, and leakage current owing to direct tunneling increases drastically, leading to much higher power consumption and dramatically reduced device reliability[20, 21]. Replacing SiO_2 with high-κ dielectric at 45 nm technology node, such as HfO_2, allow improved gate capacitance without the associated leakage current problem[21, 22].

So far, the most controllable approach in semiconductor industry for low cost, high-quality, scalable dielectric deposition is atomic layer deposition (ALD)[23, 24]. In the most advanced Si MOSFETs (e.g. Intel 14 nm Fin-FET), the physical thickness of HfO_2 is 2.6 nm, corresponding to 0.9 nm EOT[25]. In addition, the gate leakage and interface state density (D_{it}) required for low-power CMOS is 1.5×10^{-2} A/cm^2 and ~10^{10} cm^{-2}eV^{-1}[25]. These performance serves as important benchmarks for any emerging technologies. Due to the ultra-clean interface without dangling bond on the 2D materials, the dielectric deposition via ALD on 2D materials remains great challenging (Fig. 1(a))[26]. To achieve high quality dielectric integration on 2D materials for top gate FET (Fig. 1(b))[7], many active processes have been developed for uniform deposition of high-κ dielectric on 2D materials, mainly including surface functionalization (such as plasma[27, 28], ozone[29–31], electron beam irradiation[32]), metal seeding layer[33, 34], van der Waals integration[35–37] and organic seeding layer[38–41] and so on.

The surface of 2D material is pretreated by high-activity units such as plasma, ozone and electron beam to increase the nucleation sites for ALD. However, these processes involve high-energy and reactive species which will introduce the overmuch defects and interface states[42]. Wang *et al.* reported that top gate few-layer MoS_2 FETs with ~10 nm HfO_2 deposited by ozone pretreatment are fabricated (Fig. 1(d)), showed large D_{it} of ~5×10^{12} cm^{2}eV^{-1} due to undesirable damage of MoS_2 interface[31]. Metal seeding layer which is evaporated onto 2D materials followed by oxidation is the most extensive technique to achieve ALD deposition on 2D materials[43]. Subject to the thickness and roughness of the seeding layer, this method is difficult to achieve ultra-thin EOT with smooth enough interface. Zou *et al.* presented that 1 nm Y as seeding layer for ALD nucleation sites could improve the coverage of high-quality dielectrics on MoS_2 channels (Fig 1(e))[33]. The statistical results showed average mobility and SS of 47.7 cm^2/(V·s), 120 mV/dec, respectively. When the HfO_2 thickness down to 9 nm (corresponding EOT is about 4 nm) with optimized fabrication processes, a reduced SS of 65 mV/dec was achieved, indicating the improved interface quality. More recently, Illarionov *et al.* used epitaxial calcium fluoride (CaF_2) as dielectric to build up back gate 2D transistors (Fig. 1(f)). Bilayer MoS_2 transistors were achieved by transferring MoS_2 film onto 2.2 nm CaF_2 dielectric, corresponding EOT of which is less than 1 nm. The devices exhibit SS down to 90 mV/dec, which are among the leading values reported for back-gated devices[35]. It is worth noting that, the greatest challenge of CaF_2 as a dielectric is how to achieve top gate dielectric integration.

Besides, using organic film as the seeding layer to realize the conformal deposition of oxide on 2D materials, which is more amicable than the above surface functionalization and oxidized metal layer method to 2D materials because of ultra-smooth interface of organic crystal and damage-free van der Waals interaction[38, 40]. Organic film buffer layer usually contains many hydroxyl groups, carboxyl groups or other hydrophilic groups, serve as ideal reaction sites for ALD[38–40]. Wang *et al.* firstly used perylene tetracarboxylic acid (PTCA, a kind of carboxylate-terminated perylene molecule) to functionalize graphene with densely packed functional groups and achieved uniform ultrathin Al_2O_3 deposition on graphene. PTCA is selectively coated graphitic surfaces owing to its planar, conjugated ring system and its symmetrically arranged, negatively charged terminal carboxylates (Fig. 1(g))[38]. Sangwan *et al.* showed that using perylene-3,4,9,10-tetracarboxylic dianhydride (PTCDA) organic film as seeding layer to deposit Al_2O_3 and HfO_2 stacks exhibited high uniformities (Weibull parameter β > 25) and large breakdown strengths (Weibull parameter E_{BD} > 7 MV/cm), which are comparable to dielectrics on Si substrate[40]. However, the most of current organic seeding layers are thick organic films, resulting in decreased overall gate capacitance and a reduced effective dielectric constant, which cannot achieve 1 nm EOT even below.

Although some new techniques applied, compared with the advanced technology, high-κ dielectric with larger EOT and inferior interface quality are still one of the biggest obstacles to the application of 2D MOSFETs. Fig. 1(c) shows the requirement of high-quality dielectric on 2D materials, including smaller EOT and D_{it}, potential of scalable integration and so on. The organic seeding layer is one of the most promising techniques for implementing large-scale 2D integrated circuits due to damage-free interface and scalable integration potential, which are the great advantages beyond other technologies. Recent developments indicate that some organic molecules can self-limited assemble on 2D materials by van der Waals interaction with thickness of only single atomic layer[39–41]. These molecules are likely to be a very good option for integrating ultra-thin dielectric while avoiding reduction in overall capacitance due to increased thickness of seeding layer. In the following development, combination of monolayer hydrophilic organic molecules as seeding layer which can self-limited grow on 2D interface and higher dielectric constant oxide (such as La_2O_3, etc.) will hopefully achieve sub-1 nm EOT on scalable 2D logic transistors.

3. Ultra-low power NC-FET based on 2D TMDC

The dielectric, as we all know, comprises a significant contribution to the power dissipation of nano devices and integrated circuits. Different from boosting gate capacitance, ferroelectric NCFETs[17] preforms an internal voltage amplification and thus sub-60 SS, which can effectively lead to reduce V_{dd} and eventually low power consumption.

The phenomenological formalism for the double-well Gibb's free energy U_f of a single-domain ferroelectric capacitor is given as a function of the spontaneous polarization P_s: $U_f = \alpha P^2 + \beta P^4 + \gamma P^6$, known as the Landau–Ginzburg–Devonshire (LGD) theory[44]. The polarization–voltage (P–V) curve of ferroelectrics (FE), by mathematical deduction, could be plotted as a S-shape and a negative capacitance zone emerges near $P \approx 0$, which is energetically unstable (blue lines in Figs. 2(b) and 2(c)). While a linear dielectric capacitor shows a simple quadratic U_f–P, a linear P–V curve (yellow lines in Figs. 2(b) and 2(c)) and constant positive capacitance, the NC region may be stabilized by a series linear dielectric (DE)[17]. One would see that a well-matched ferroelectric-dielectric (FE-DE) stack (Fig. 2(a)) shows a steep swing P–V shape and a capacitance enhancement near $P \approx 0$ (green lines in Figs. 2(b) and 2(c)).

According to Eq. (1), the first term $1 + \dfrac{C_{it}}{C_{ox}}$, often called the 'body-factor', is always larger than 1 due to positive C_{ox} and C_{it}. Salahuddin *et al.* proposed that the negative capacitance zone, where the $-1 < \dfrac{C_{it}}{C_{ox}} < 0$, helps to realize SS of sub-60 mV/dec, reduce switching energy, and thus decrease the power consumption of FETs. Of note, a FE-DE stack as well as a resistor are always used to perform a pulse test as a proof of existence of NC effect, known as transient NC measurements[45–47]. However, the origin and physical mechanism of NC effect are still confusing and controversial, which are beyond the scope of this paper.

For ferroelectric materials in NCFETs application, traditional perovskite ferroelectrics like $PbZrO_3$ (PZT), $BaTiO_3$ (BTO), or polymers like polyvinylidene fluoride-trifluoroethylene (PVDF-TrFE) obviously become out of place due to their poor thickness scalability and CMOS process compatibility. Fortunately, ferroelectric polycrystalline $HfZrO_2$ (HZO)[48] (Fig. 2(d)), which can be obtained through *in situ* alternating deposition of ZrO_2 and HfO_2 via ALD, provides an appealing proposal to construct NCFETs using Si[25, 49, 50], Ge[51–53], and TMDC[16, 18, 54–57] as channel. The composition of HZO could be achieved by controlling the ratio of ZrO_2 and HfO_2 and the ferroelectricity is enhanced through a rapid thermal annealing followed. There is no doubt that HZO is considered as the most industry-relevant ferroelectric material currently.

Recent researches have shown that 2D semiconductors using ferroelectric as gate dielectric exhibit excellent performance, such as reduced SS and V_{dd}, etc. Yu *et al.* fabricated n-type MoS_2 NCFETs[16] using the structure shown in Fig. 2(e), with layered MoS_2 mechanically exfoliated onto ALD deposited Al_2O_3/HZO gate stack. The MoS_2 NCFETs devices exhibited ultra-low SS of 23 mV/dec, sub-60 mV/dec over 6 orders of the drain current, nearly hysteresis-free up to V_{DS} = 1 V. Importantly, they could modulate 5 orders of I_{DS} using a gate drive of 232 mV, clearly demonstrating the potential of MoS_2 NCFETs for low-power logic applications. Furthermore, compared to normal MoS_2 FETs with 11.2 nm EOT, the NCFETs achieve 60% improvement in current density (250 μA/μm) and 4 times improvement in transconductance. Moreover, they further study the high frequency operation and show that sub-60 mV/dec is maintained at least to 10 kHz without signs of degradation. For current CMOS technology, p-type transistors are also very important for low power application. Wang *et al.* realized hysteresis-free p-type WSe_2 NCFETs[57] by using van der Waals Pt-WSe_2 contact and HZO/Al_2O_3 as the dielectric layer with reduced SS for both forward and reverse gate voltage sweep (the minimum $SS_{forward}$ and $SS_{reverse}$ of 18.2 and 44.1 mV/dec, respectively). Also, drain current could be modulated by 5×10^4 within small gate voltage of 220 mV.

The SS-Hysteresis phase diagram (Fig. 2(f)) summarizes representative reported works of 2D NCFETs with comparison

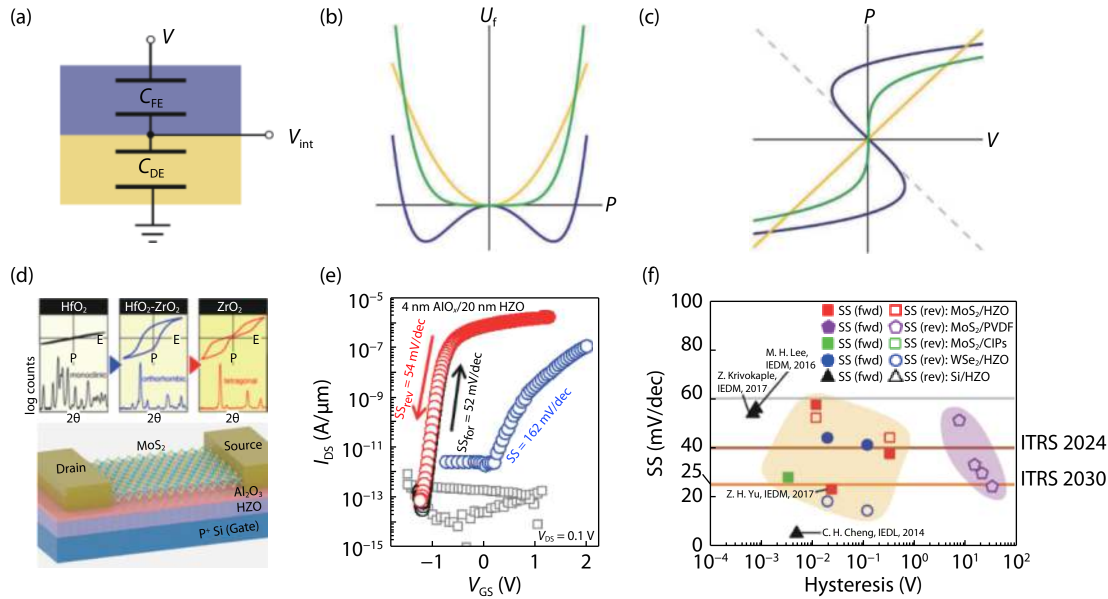

Fig. 2. (Color online) Basic concept of NC and ultra-low power NCFETs based on 2D TMDC. (a) Schematic of two capacitors in series. V_{int} is the voltage at the interface, equaling to the radio of gate voltage V and body factor m. (b) Gibb's free energy-polarization (U–P) diagram[58] of FE, DE, and a series of them for capacitance matching and stabilization of negative capacitance. (c) Polarization–Voltage (P–V) curves deducted from U–P curves in (b). An S-shaped curve of FE is shown. (d) Polarization–electric field (P–E) loop of ferroelectric HZO and the schematic of back gate MoS_2 NCFETs. (e) I_D–V_{GS} curves of a MoS_2 NCFET[16] on 4 nm AL_2O_3/20 nm HZO (black: forward sweep, red: reverse sweep, grey: gate leakage) and control device with the same channel length of 1.7 μm on 25 nm Al_2O_3 (blue) at V_{DS} = 0.1 V. (f) A brief summary of representative SS-hysteresis data of reported 2D NCFETs, including MoS_2 FETs with HZO[16, 18, 54, 55], PVDF[59], CIPs[60, 61], and WSe_2 FETs with HZO dielectric[56, 57], while three typical works based on Si are selected for comparation. According to ITRS 2.0[6], the requirements for scaled SS, 40 mV/dec in 2024, 25 mV/dec in 2030, are plotted respectively.

with the advanced Silicon technology and ITRS requirements. According to ITRS 2.0 requirements of logic transistors released in 2015, SS will decrease to 40 mV/dec in 2024, and 25 mV/dec in 2030, shown in Fig. 2(f). Of note, apart from large hysteresis of MoS_2/PVDF cases (in purple shadow), several 2D NCFETs can satisfy ITRS requirement of 40 mV/dec (even 25 mV/dec), while the difference of SS between forward and reverse sweep and hysteresis in transfer curves remain to be reduced.

Although results above have demonstrated excellent isolated device performance, NCFETs applications still face several major problems: physics behind NC effect, the highest operating frequency of NCFETs, and the fatigue characteristics and reliability of ferroelectric materials such as HZO. Recently, transient NC measurements[45–47] were reported, including that S-shaped P-E loop predicted by Landau was obtained from an ultrafast pulse test on FE/DE stack[47], revealing that the ferroelectric does possess a differential negative capacitance in a certain region around $P \approx 0$. These works all underline the importance of the frequency dependence of ferroelectrics, which helps to understand the physical mechanism of ferroelectric NC, but they are not identical to quasi-static NC behavior observed in FETs measurement. According to the NC theory, the appearance of the NC effect is still related to the ferroelectric switch. Therefore, the maximum operating speed of the NCFETs may be subject to dynamics of polarization in ferroelectrics instead of CV/I as MOSFET. Krivokapic *et al.* from Global Foundries reported ring oscillators[25] based on 14 nm Si FinFET using Si-doped HfO_2 with competitive performance. However, the controversy still exists in this result that the performance improvement is derived from higher dielectric constant than NC effect. More works focused on device speed should be continued in the future. Another challenge is the reliability of ferroelectrics, due to ion movement and degradation from ferroelectric fatigue and imprint. The endurance of FE-HfO_2 as memory is about 10^4–10^5, which is far from reliability requirements of logic transistors[62]. In addition, reducing oxygen vacancies of doped HfO_2 is also one of the key technologies to improve reliability[63]. Therefore, although NCFETs have significant advantages in low-power logic transistors, the application still goes a long way.

4. Conclusion

2D semiconductors are promising candidates for low-power logic transistors due to their inherent advantages, such as ultimate body thickness, dangling bond free, sizable and tunable bandgap, and reasonable mobility. However, the application of 2D semiconductors remains in infancy, and more specific techniques for 2D characteristics have been developed. In this paper, low-power 2D logic transistors using ultra-thin high-κ dielectric and NCFETs are overviewed. Some recent progresses of techniques for gate dielectric with related advantages and disadvantages are reviewed. Moreover, a perspective discussion for realization of sub-1 nm EOT was followed. Then, the performance of typical 2D NCFETs are analyzed, and more researches on 2D NCFETs are summarized. At last, a prospect for further development for NCFETs is addressed.

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