ARTICLES

Journal of Semiconductors
(2019) 40, 052901
doi: 10.1088/1674-4926/40/5/052901

A novel design approach of charge plasma tunnel FET for radio frequency applications

Shivendra Yadav†, Alish Pamnani, Dheeraj Sharma, Anju Gedam, Atul Kumar, and Neeraj Sharma

Abstract: In this paper, the impact of extra electron source (EES) and dual metal gate engineering on conventional charge plasma TFET (CP-TFET) have been done for improving DC and analog/RF parameters. CP-TFET structure is upgraded to double source CP-TFET (DS-CP-TFET) by placing an EES below the source/channel junction for enhancing the device performance in terms of driving current and RF figures of merit (FOMs). But, in spite of these pros, the approach is having cons of higher leakage current similar to MOSFET and negative conductance (inherent nature of TFET). Both the issues have been resolved in the double source dual gate CP-TFET (DS-DG-CP-TFET) by gate workfunction engineering and drain underlapping respectively. Additionally, for getting the optimum performance of DS-DG-CP-TFET, the device sensitivity has been investigated in terms of position of EES, length of drain electrode and workfunction of gate electrode 1 (GE1).

Key words: ambipolar current; charge plasma; EES and dual metal gate engineering

Citation: S Yadav, A Pamnani, D Sharma, A Gedam, A Kumar, and N Sharma, A novel design approach of charge plasma tunnel FET for radio frequency applications[J]. *J. Semicond.*, 2019, 40(5), 052901. http://doi.org/10.1088/1674-4926/40/5/052901

1. Introduction

With the advent of MOSFET, technology over the past few decades has reached to new heights. The dimensions of MOSFET in the last decade has been reduced by three orders of magnitude in order to attain high performance integrated circuits[1]. Shrink in the technology also increases switching speed, device density, reduces power dissipation, cheaper fabrication cost and improved RF performances[1]. According to past few researches, downscaling of channel length below 32 nm results in the short channel effects[2]. This has great impact on gate oxide tunneling, parasitic effects and have poor reliability due to the hot carrier effect[2]. Downscaling of device increases the electric field which results in charge leakage with adverse effect on I_{ON}/I_{OFF} ratio. As an alternative of MOSFET, various novel devices came into existence. Emerging transistor like fin field effect transistor (FinFET) is invented in order to overcome various performance issues of planar MOSFETs. FinFETs have less short channel effects and better control over channel but, vertical structure of its fin causes corner effects, parasitic capacitance degrade performance of the integrated circuits (ICs)[3]. Carbon nano tube field effect transistors (CNTFET) are also having efficient thermal conductivity, high tensile strength, better field emission but have lower life time, limited power handling capacity and larger potential is needed for field emission[3].

According to international technology roadmap for semiconductors (ITRS) 2005, to overcome these critical issues, tunnel FET (TFET) has proved itself to be a best alternative of MOSFET[4]. TFET has p–i–n structure and is based on band-to-band tunneling (BTBT) phenomenon and has gained much attention and attraction of research community[5]. TFET has many advantages which include steep slope in I_D versus V_{GS} graph in conduction state (subthreshold swing (SS) $<$ 60 mV/decade) and low OFF state current, improved threshold voltage, fabrication process similar to MOSFET etc[5].

Physically doped TFET suffers from random dopant fluctuations (RDFs) at nano scale regim. RDFS is defined as movement of dopant atoms across the junction and it has sever effects on TFET as compared to MOSFET[6–8]. RDFs leads to reduction of abruptness near tunneling junction which causes an undesirable variation in threshold voltage, drain current and increment in OFF-state current[6]. Abrupt junction is paramount requirement for efficient tunneling at source/channel region but, it is tedious to maintain because of RDFs at source/channel junction[8]. Thus, the introduction of charge plasma concept is useful in providing the sharp junction profile[9]. In charge plasma technique the formation of drain (n^+) regions and source regions (p^+) are executed by using metal electrodes of appropriate work-function (WF); there is no physical junction formed. Through the charge plasma sufficient carrier concentration is achieved below electrodes which are intact in the form of plasma[9]. But, the presence of a barrier between control gate (CG) and source electrode at source/channel junction is responsible for degradation of its performance.

In this concern, EES is deposited below the source/ channel junction of the CP-TFET which improves its DC and RF performances. This leads to the formation of new device double source charge plasma TFET (DS-CP-TFET). But, this device faces the problem of static power dissipation and negative conductance[10] which needs to be resolve. DS-CP-TFET uses drain underlap technique[11] and dual metal gate engineering to supress ambipolarity and leakage current respectively. The novel device double source dual gate charge plasma TFET (DS-DG-CP-TFET) is proposed as a final structure. There are several techniques of deposition the dual metal CG, like first metal can be interdiffused into second one as reported in Ref. [12]. On the oth-

Correspondence to: S Yadav, shivendra1307@gmail.com
Received 8 FEBRUARY 2019; Revised 18 MARCH 2019.
©2019 Chinese Institute of Electronics

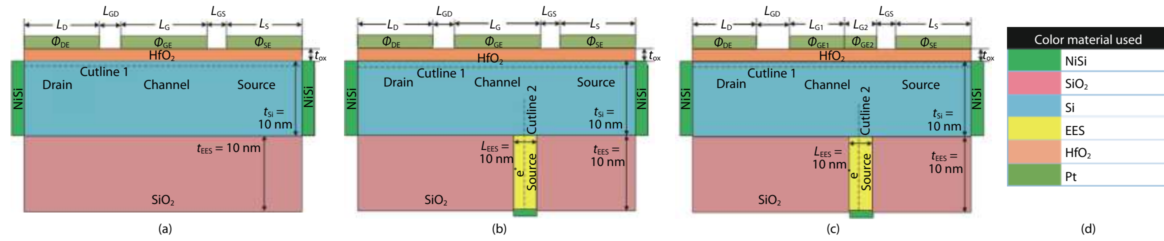

Fig. 1. (Color online) Cross sectional view (a) CP-TFET, (b) DS-CP-TFET, (c) DS-DG-CP-TFET, and (d) color bar of materials.

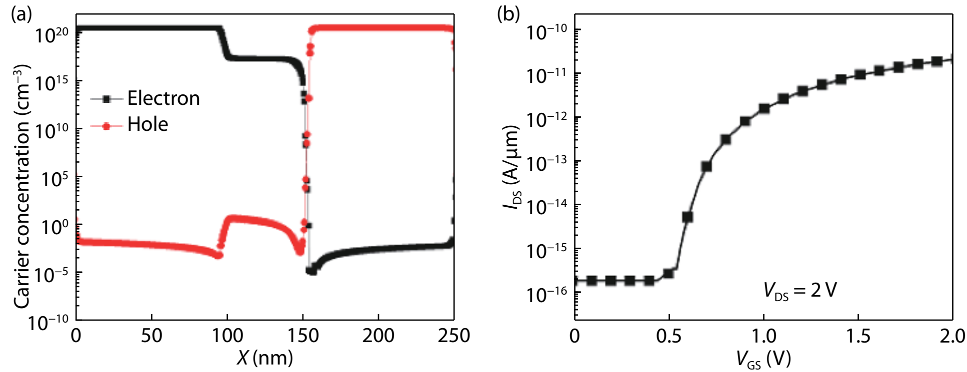

Fig. 2. (Color online) (a) Carrier concentration of DS-DG-CP-TFET as reported in Refs. [20, 21], and (b) TC of conventional TFET.

er hand, atomic layer deposition (ALD) is also one of the advanced fabrication technique by virtue of which single fine layers of Pt by using (methylcyclopentadienyl) trimethylplatinum (MeCpPtMe3) can be deposited easily[13]. For dual metal work function, platinum (Pt) is used which, allows variable WF by inducing halogen adsorption on Pt(111) as a function of the coverage without affecting the integrity of dielectric[14]. Electronegativity of halogen adsorption is related with movement of charge from metal to adsorption layer which causes increase in the WF of Pt. However, by choosing iodine (I) for adsorption, opposite flow of charges can be observed which leads to reduction in Pt WF[14]. So by using a single metal we can achieve dual workfunction metal (4.5 and 5.2 eV) as CG.

2. Device structure and simulation

Figs. 1(a)–1(c) depicts the cross sectional view of device CP-TFET, DS-CP-TFET and DS-DG-CP-TFET. Fig. 1(d) shows the color bar of materials used in different color regions. A lightly doped silicon layer of concentration 10^{15} cm^{-3} is used for the substrate for all the three devices. The metal electrode of different WF 3.4 eV (Hf) and 5.93 eV (Pt) is used to form n$^+$ and p$^+$ region respectively[15]. A thin oxide layer of HfO_2 is used to control the formation of silicide between the metal electrode and substrate[16]. Nickel silicide (NiSi) has low resistivity, low formation temperature and has a WF of 4.5 eV which is used for source and drain contacts with 0.44 eV barrier height[17]. EES is introduced in the source region with doping concentration 10^{19} cm^{-3}.

For all three devices, length of source electrode (L_S) = 50 nm, CG length (L_G) = 50 nm, silicon body thickness (t_{Si}) = 10 nm, oxide thickness (t_{ox}) = 2 nm, EES thickness (t_{EES}) = 10 nm, WF of electrical drain (ϕ_{DE}) = 3.4 eV and WF of electrical source (ϕ_{SE}) = 5.93 eV. For CP-TFET and DS-CP-TFET length of drain electrode (L_D) = 50 nm, drain spacer length (L_{GD}) = 5 nm, length of EES (L_{EES}) = 10 nm and WF of CG (ϕ_{GE}) = 4.5 eV. Furthermore for DS-DG-CP-TFET: L_D = 35 nm, L_{GD} = 20 nm, ϕ_{GE1} = 5.2 eV and ϕ_{GE2} = 4.5 eV. The simulations of device have been accomplished with 2-D SILVACO ATLAS simulator[18, 19]. The models used to process the simulations are non-local BTBT model, Fermi-Dirac statistical model and Shockley-Read-Hall Recombination (SRH) model. BTBT is used to account the tunneling generation rate of charge carriers at source/channel and drain/channel junctions. This non-local model uses Fermi and SRH model to calculate the tunneling probability and numerical solutions. Meshing is kept very fine across all regions.

3. Results and discussion

This section describes relative comparison of performances among three devices i.e. CP-TFET, DS-CP-TFET and DS-DG-CP-TFET in terms of their DC characteristics and Analog/RF parameters.

3.1. DC characteristics

Conventional physically doped TFET has ON state current in nano ampere range and OFF state current in femto ampere range at V_{DS} = 2 V as mentioned in Refs. [20, 21]. The conventional CP-TFET is first calibrated with above mentioned literature and the carrier concentration mentioned is achieved by charge plasma technique as reposted in Ref. [20] as shown in Fig. 2(a). Further, Fig. 2(b) shows the transfer characteristics (TC) of the calibrated CP-TFET with Ref. [20]. It can be observed that the calibrated CP-TFET achieves nearly same ON state current but, slightly lower OFF state current because of dopingless nature of the device.

Electric field distribution along the channel is shown in Fig. 3(a). All the three devices have the same peak which shows that the tunneling probability is almost same for all the three devices. This is further supported by Fig. 3(b), which shows the energy band diagram (EBD) along cutline 1. Fig. 3(b)

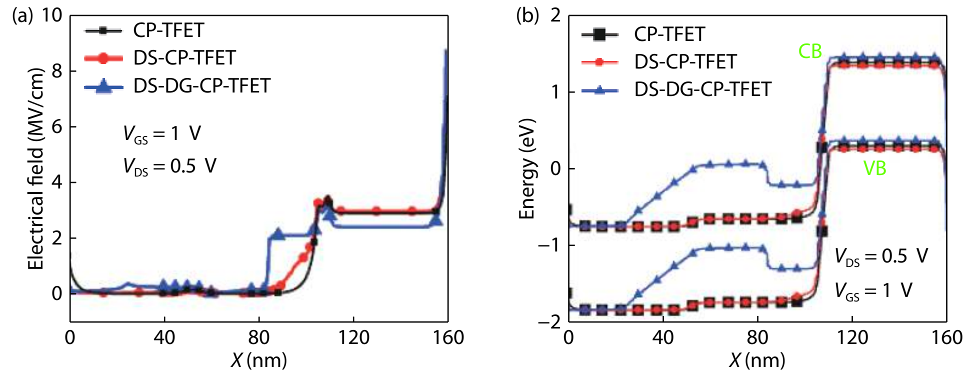

Fig. 3. (Color online) (a) Electrical field and (b) EBD along cutline 1 in ON state.

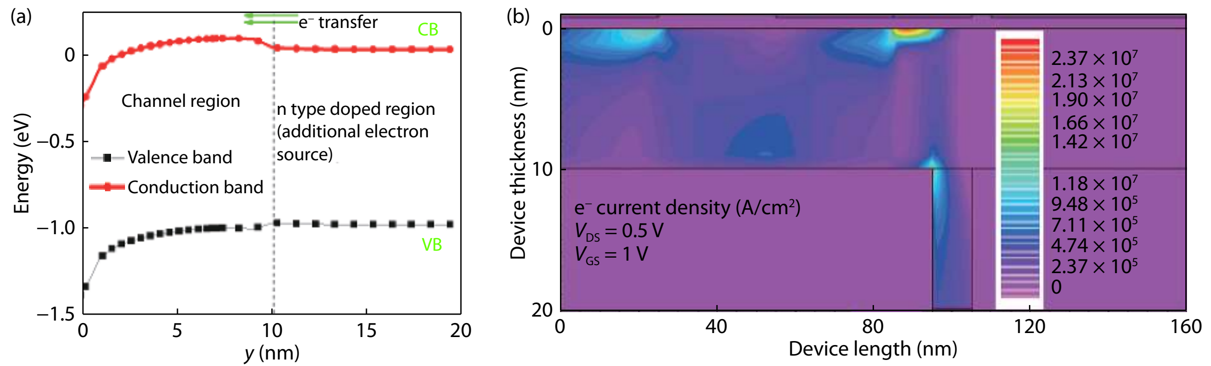

Fig. 4. (Color online) (a) EBD along cutline 2 and (b) contour plot of current density in ON state.

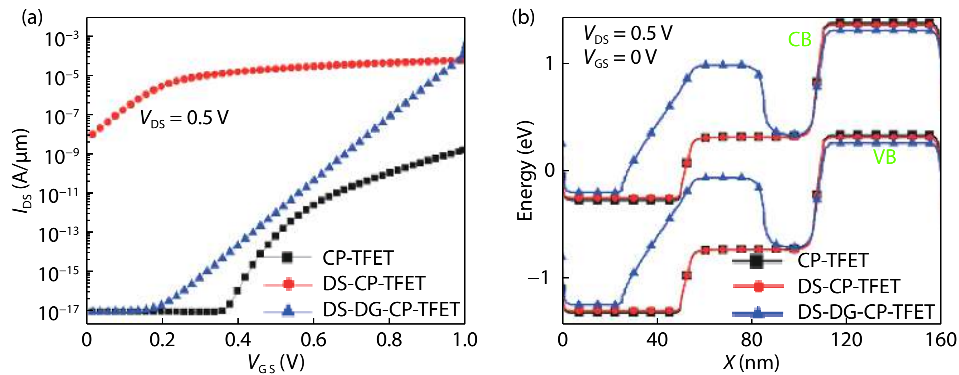

Fig. 5. (Color online) Variation of (a) TC in ON state and (b) EBD along cutline 1 in ambipolar state.

shows almost similar tunneling width for all three devices. Both of these observations clearly indicate that the increase in ON state current in DS-CP-TFET and DS-DG-CP-TFET is due to EES placed below the channel. Fig. 4(a) shows the EBD in ON state along cutline 2 and it can be observed that the electrons move from the EES to the channel over the barrier through thermionic emission. When the positive gate and drain voltage is applied on device a resultant positive voltage exist over the EES and other end of EES is connected with ground source. Since, EES is heavily doped so electrons came out easily from EES into the channel region through over the barrier. This is also evident from Fig. 4(b) in which the electron current density in ON state has been investigated by contour plot which indicates that additional current density is provided by the EES. Therefore, there is significant increase in ON state current in case of DS-CP-TFET and DS-DG-CP-TFET which can be seen from Fig. 5(a). From Fig. 5(a), it can also be observed that DS-CP-TFET has high leakage current. This has been rectified by employing dual metal gate engineering in DS-DG-CP-TFET. Fig. 5(b) shows EBD in OFF state along cutline 1 and it can be seen that there is an uplift in the energy band under GE1 causes the formation of potential well and restricts the movement of leaky charge carriers in the channel. Apart from this Fig. 6(a) indicates EBD in ambipolar state, where drain underlapping in DS-DG-CP-TFET clearly illustrates that tunneling width is getting wider as compared to other two devices. The advantageous impact of wider tunneling width at drain/channel junction can be visualized in terms of suppressed ambipolar current in proposed structure in Fig. 6(b). The figure is showing distribution of drain current for negative gate voltage in comparative manner in ambipolar state.

A relative study of DC characteristics is shown in Table 1.

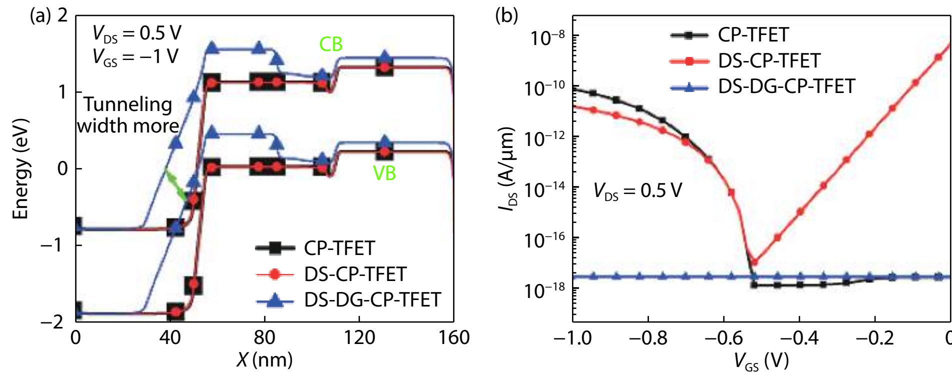

Fig. 6. (Color online) Variation of (a) EBD along cutline 1 in OFF state and (b) TC in ambipolar state.

Table 1. DC parameters of devices.

Parameters name/Unit	CP-TFET	DS-CP-TFET	DM-DG-CP-TFET
V_{th} (V)	0.12	0.96	0.99
ON current (A/μm)	1.067×10^{-9}	3.794×10^{-5}	3.238×10^{-4}
OFF current (A/μm)	5.078×10^{-18}	6.013×10^{-9}	5.219×10^{-18}
Ambipolar current (A/μm)	9.184×10^{-11}	1.983×10^{-11}	5.204×10^{-18}
SS (mV/dec)	28.8	61.6	59.8

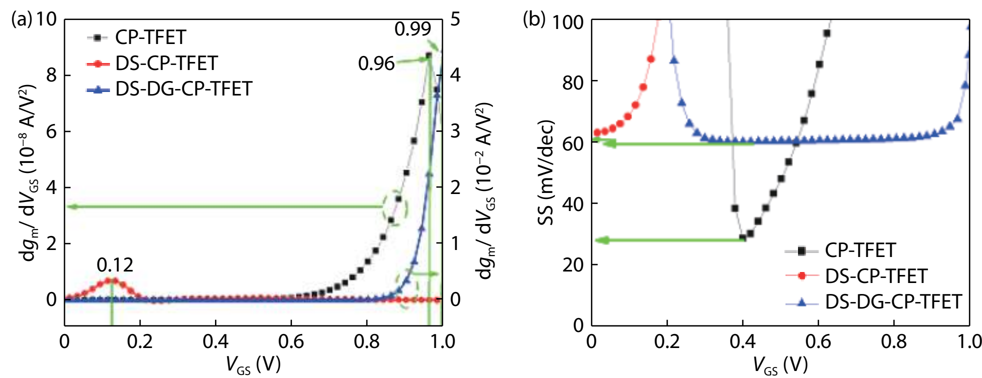

Fig. 7. (Color online) (a) V_{th} and (b) SS of all three devices.

In the table, reported values of V_{th} have been calculated by second derivative method reported in Ref. [22]. In Fig. 7(a), value of V_{th} has been verified by differentiating g_m with respect to V_{GS}[22]. Also, SS has been numerically calculated by reported methodology in Ref. [23] and is shown in Fig. 7(b) along V_{GS}. Figure shows the minima of *SS* curve of different devices which again validates the values obtained from Table 1.

3.2. RF analysis

In the present-day framework, RF figures of merit are critical parameters for determining the performance of the device. For elucidating analog performances of device there are various fundamental characteristics such as transconductance (g_m), gate-to-drain capacitance (C_{gd}), cut-off frequency (f_t), maximum oscillating frequency (f_{max}), gain bandwidth product (GBP), intrinsic gain (IG), transconductance generation factor (TGF).

Transconductance (g_m) is the ratio of change in drain current (I_{DS}) to change in input voltage. DS-CP-TFET and DS-DG-CP-TFET have nearly 10^4 and 10^5 time higher g_m as compared to conventional one. Gate-to-drain capacitance (C_{gd}) is also known as Miller capacitance is indispensable for high frequency designing of circuits. C_{gd} behaves as inversion capacitance ($C_{gd,inv}$) for higher values of V_{GS} and as parasitic capacitance for lower values of V_{GS}[24, 25]. It should always be lower for higher switching speed. It can be seen from the Fig. 8(b) that C_{gd} for DS-DG-CP-TFET is approximately same but for DS-CP-TFET it is 10 times bigger than convention CP-TFET.

Cut-off frequency (f_t) is the frequency at which the amplifier's gain rolls off to unity. Fig. 9(a) shows the variation of f_t as a function of V_{GS}. It can be noticed from the figure that as V_{GS} increases f_t rises because of increment in g_m. Over particular range, DS-DG-CP-TFET has higher f_t by 100 and 1000 times for DS-CP-TFET and DS-DG-CP-TFET than CP-TFET which show relevancy of proposed structure at high frequency range. Gain bandwidth product (GBP) is the product of gain and bandwidth and follows the same tendency as f_t. From Fig. 9(b) it can be concluded that DS-CP-TFET and DS-DG-CP-TFET have 10^4 times elevated GBP as compared to CP-TFET. Intrinsic gain (IG) is the product of g_m and output resistance (R_o); in other words it is the maximum possible voltage gain of the device[26]. Fig. 10 shows IG with respect to V_{GS} which reflects after threshold voltage IG has been suddenly increased; DS-DG-CP-TFET has nearly value of IG is 64 whereas DS-CP-TFET and CP-TFET have

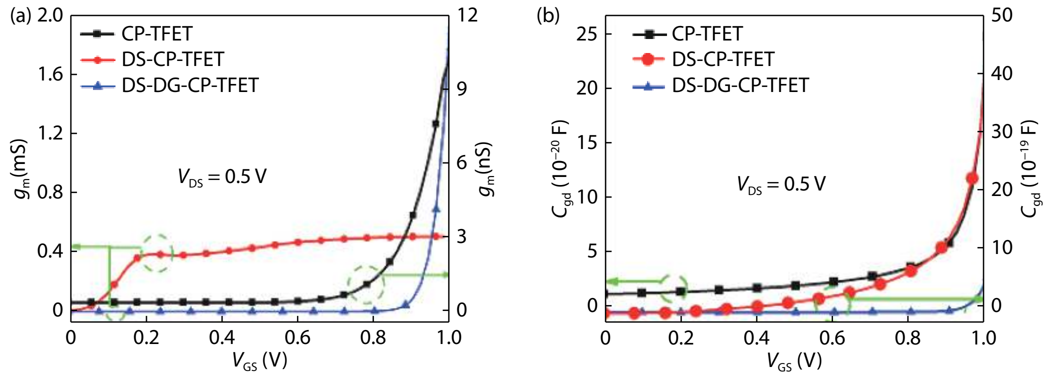

Fig. 8. (Color online) Variation of (a) g_m and (b) C_{gd} with V_{GS}.

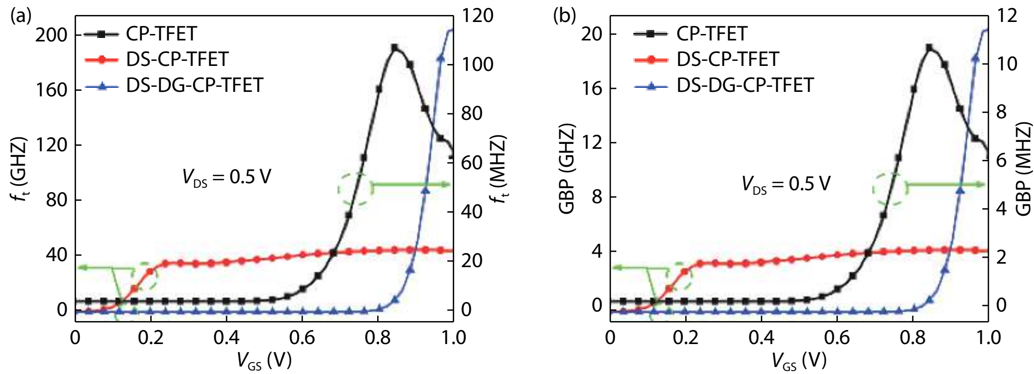

Fig. 9. (Color online) Variation of (a) f_t and (b) GBP with V_{GS}.

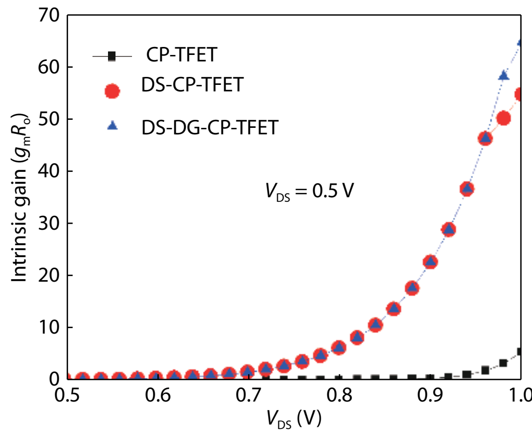

Fig. 10. (Color online) Variation of IG with V_{GS}.

IG of 54 and 5 respectively at V_{GS} 1 V. Maximum oscillating frequency (f_{max}) is the frequency at which power gain is 1. It can be calculated as :

$$f_{max} = \sqrt[2]{\frac{f_t}{8\pi C_{gd} R_{gd}}}. \tag{1}$$

It can be seen from Fig. 11(a) that f_{max} rises with V_{GS}. DS-DG-CP-TFET, DS-CP-TFET and CP-TFET have 15.58 MHz, 7.19 MHz and 16.58 kHz respectively as their maximum (f_{max}) values. Both DS-DG-CP-TFET and DS-CP-TFET show nearly 1000 times increment with respect to CP-TFET. Transconductance generation factor (TGF) shows the efficiency to convert DC parameter (I_{DS}) into AC parameter (g_m). It gives the extent to which a device optimises I_{DS} for better amplification with low power dissipation[27]. It is formulated by the ratio of g_m to I_{DS} and in subthreshold region I_{DS} is negligible so the graph is drawn after 0.5 V. DS-DG-CP-TFET has highest TGF of 41.97 V^{-1} as compared to DS-CP-TFET of 2.77 V^{-1} and CP-TFET of 35.73 V^{-1}, but further increment in V_{GS} cause a fall in TGF for all devices as can be seen from Fig. 11(b).

4. Optimisation

In this section, we are trying to select the appropriate values of ϕ_{GE1}, drain spacer length (L_{GD}) and position of EES in the DS-DG-CP-TFET. In this concern, the device sensitivity in terms of DC and RF parameters (f_t) are investigated for different values of these parameters. As we move EES towards the drain region from source/channel junction, the leakage current starts increasing which can be depicted in Fig. 12(a). The value f_t shown in Fig. 12(b) also degrades due to the shifting of the EES towards the drain region. The graph of f_t shows significant degradation for the position variation of EES. Therefor, position optimization of EES is one of the important task while placing it below the channel.

Dual metal gate engineering is used in DS-DG-CP-TFET to reduce the leakage current. Fig. 13(a) shows the TC for different value of ϕ_{GE1}. As ϕ_{GE1} increases, the ON state current as well as OFF state current decreases. The value of f_t decreases with increase in ϕ_{GE1} shown in Fig. 13(b). So, appropriate value of ϕ_{GE1} is required for the optimised performance of the proposed device. Therefore, ϕ_{GE1} = 5.2 eV in used in DS-DG-CP-TFET where the leakage current reaches in the range of 10^{-19} A/μm with negligible effect in the ON state current.

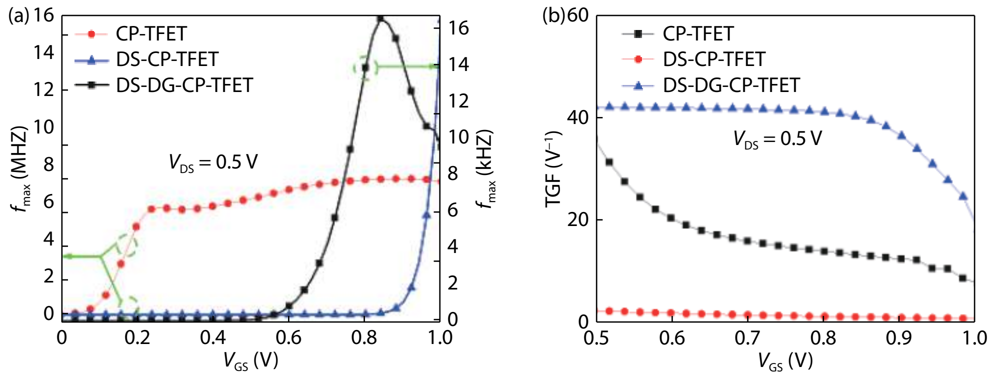

Fig. 11. (Color online) Variation of (a) f_{max} and (b) TGF with V_{GS}.

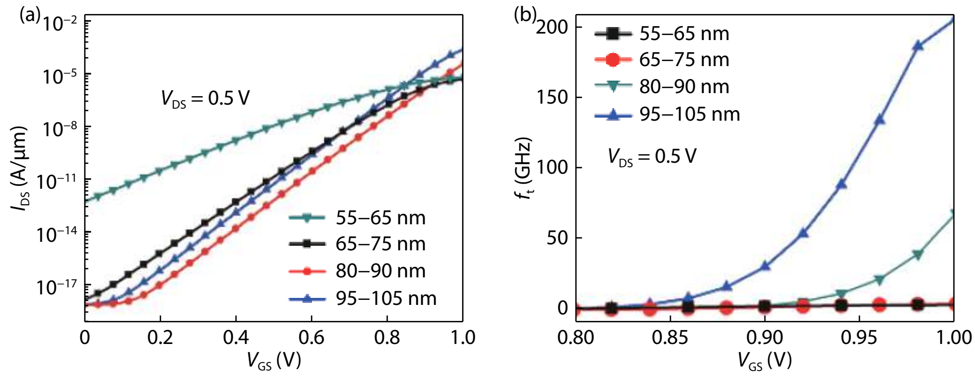

Fig. 12. (Color online) (a) TC and (b) f_t of DS-DG-CP-TFET for different location of dual source with V_{GS}.

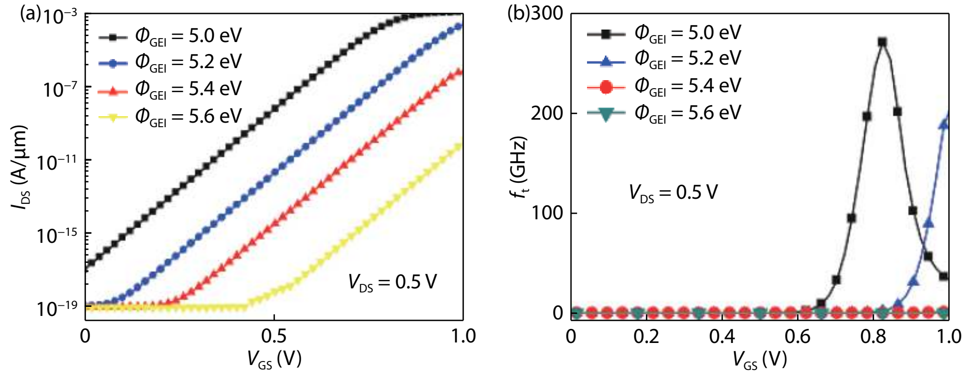

Fig. 13. (Color online) (a) TC of DS-DG-CP-TFET for different WF of GE1 and (b) variation in cutoff frequency with V_{GS}.

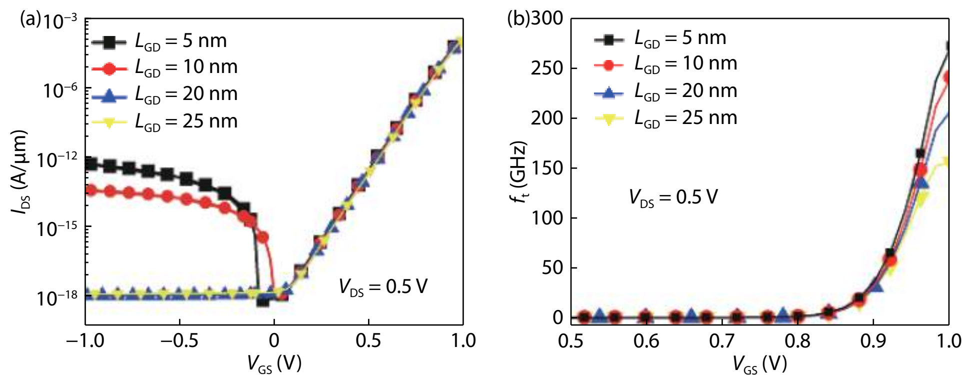

Fig. 14. (Color online) (a) TC of DS-DG-CP-TFET for different spacer length (L_{GD}) and (b) variation in cutoff frequency with V_{GS} at different spacer length (L_{GD}).

Supression of negative conductance is very important in circuit level performances. TC for different values of L_{GD} in DS-DG-CP-TFET is shown in Fig. 14(a). As value of L_{GD} increases, ambipolarity is supressed. Variation of f_t is shown in Fig. 14(b), which reflects degradation while increasing L_{GD}. So, the suitable value of L_{GD} is chosen for optimized performance of proposed structure.

5. Conclusion

CP-TFET has low ON state current and poor RF performance. To resolve these issues DS-CP-TFET has been formed to increase ON state current by using EES but on the other hand it has issue of ambipolarity and leakage current. Therefore, a novel device DS-DG-CP-TFET has been proposed which improves device performance in terms of DC and Analog/RF parameters. It uses EES for increasing ON state current, dual metal gate engineering for lowering leakage current and drain underlapping technique for reducing ambipolarity. Further, optimizations are done in the position of EES, WF of GE1 and L_{GD} in DS-DG-CP-TFET to improve the over all performances of state-of-the-art.

References

[1] Dennard R H, Gaensslen F H, Yu H N, et al. Design of ion-implanted MOSFET's with very small physical dimensions. IEEE J Solid-State Circuits, 1999, 87, 668

[2] Gopalakrishnan K, Woo R, Jungemann C, et al. Impact ionization MOS (I-MOS)-Part II: Experimental results. IEEE Trans Electron Devices, 2005, 52, 77

[3] Hajare R, Lakshminarayana C, Raghunandan G H, et al. Performance enhancement of FINFET and CNTFET at different node technologies. Microsyst Technol, 2016, 22, 1121

[4] International Technology Roadmap for Semiconductors (ITRS).[Online]. Available: www.itrs2.net

[5] Koswatta S O, Lundstrom M S, Nikonov D E. Performance comparison between p-i-n tunneling transistors and conventional MOSFETs. IEEE Trans Electron Devices, 2009, 56, 456

[6] damrongplasit N, Kim S H, Liu T J K. Study of random dopant fluctuation induced variability in the raised-Ge source TFET. IEEE Electron Device Lett, 2013, 34, 184

[7] damrongplasit N, Shin C, Kim S H, et al. Study of random dopant fluctuation effects in germanium-source tunnel FETs. IEEE Trans Electron Devices, 2011, 58, 3541

[8] Jhaveri R, Nagavarapu V, Woo J C S. Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor. IEEE Trans Electron Devices, 2011, 58, 80

[9] Kumar M J, Nadda K. Bipolar charge-plasma transistor:a novel three terminal device. IEEE Trans Electron Devices, 2012, 59, 962

[10] Kroemer H. Negative conductance in semiconductors. IEEE Spectrum, 1968, 5, 47

[11] Yadav S, Sharma D, Chandan B V, et al. A novel hetero-material gate-underlap electrically doped TFET for improving DC/RF and ambipolar behaviour. Superlattices Microstruct, 2018, 117, 9

[12] Polishchuk I, Ranade P, King T J, et al. Dual work function CMOS gate technology based on metal interdiffusion. U.S. Patent, no. US 20040238859A1, 2004

[13] Aaltonen T, Ritala M, Sajavaara T, et al. Atomic layer deposition of platinum thin films. Chem Mater, 2018, 15, 1924

[14] Gossenberger F, Roman T, Tonigold K F, et al. Change of the work function of platinum electrodes induced by halide adsorption. Beilst J Nanotechnol, 2014, 5, 152

[15] Rajasekharan B, Hueting R J E, Salm C, et al. Fabrication and characterization of the charge-plasma diode. IEEE Electron Device Lett, 2010, 31, 528

[16] Kumar M J, Janardhanan S. Doping-less tunnel field effect transistor: Design and investigation. IEEE Trans Electron Devices, 2013, 60, 3285

[17] Lahgere A, Sahu C, Singh J. Electrically doped dynamically configurable field-effect transistor for low-power and high-performance applications. Electron Lett, 2015, 51, 1284

[18] Awadhiya B, Pandey S, Nigam K, et al. Effect of ITC's on linearity and distortion performance of junctionless tunnel field effect transistor. Superlattices Microstruct, 2017, 111, 293

[19] ATLAS Device Simulation Software. Silvaco Int., Santa Clara, 2014

[20] Boucart K, Ionescu A M. Double-gate tunnel FET with high-*k* gate dielectric. IEEE Trans Electron Devices, 2007, 54, 1725

[21] Wang P F, Hilsenbeck K, Nirschl T, et al. Complementary tunneling transistor for low power application. Solid State Electron, 2004, 48, 2281

[22] Raad B R, Tirkey S, Sharma D, et al. A new design approach of dopingless tunnel FET for enhancement of device characteristics. IEEE Trans Electron Devices, 2017, 64, 1830

[23] Pahwa G, Dutta T, Agarwal A, et al. Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance Part II: model validation. IEEE Trans Electron Devices, 2017, 63, 4986

[24] Cho S, Lee J S, Kim K R, et al. Analyses on small-signal parameters and radio-frequency modeling of gate-all-around tunneling field-effect transistors. IEEE Trans Electron Devices, 2011, 58, 4164

[25] Yang Y, Tong X, Yang L T, et al. Tunneling field-effect transistor: Capacitance components and modeling. IEEE Electron Device Lett, 2010, 31, 752

[26] Goswami Y, Ghosh B, Asthana P K, et al. Analog performance of Si junctionless tunnel field effect transistor and its improvisation using II–IV semiconductor. R Soc Chem, 2014, 4, 10761

[27] Madan J, Chaujar R. Gate drain-overlapped-asymmetric gate dielectric-GAA-TFET: a solution for suppressed ambipolarity and enhanced ON state behavior. Appl Phys A, 2016, 122, 973