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A novel 4H-SiC trench MOSFET with double shielding structures and ultralow gate-drain charge

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Abstract: A new ultralow gate–drain charge (Q_{GD}) 4H-SiC trench MOSFET is presented and its mechanism is investigated by simulation. The novel MOSFET features double shielding structures (DS-MOS): one is the grounded split gate (SG), the other is the P^+ shielding region (PSR). Both the SG and the PSR reduce the coupling effect between the gate and the drain, and transform the most part of the gate–drain capacitance (C_{GD}) into the gate–source capacitance (C_{GS}) and drain–source capacitance (C_{DS}) in series. Thus the C_{GD} is reduced and the proposed DS-MOS obtains ultralow Q_{GD}. Compared with the double-trench MOSFET (DT-MOS) and the conventional trench MOSFET (CT-MOS), the proposed DS-MOS decreases the Q_{GD} by 85% and 81%, respectively. Moreover, the figure of merit (FOM), defined as the product of specific on-resistance ($R_{on,\,sp}$) and Q_{GD} ($R_{on,\,sp}Q_{GD}$), is reduced by 84% and 81%, respectively.

Key words: SiC trench MOSFET; reverse transfer capacitance; gate-drain charge; figure of merit

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1. Introduction

4H-silicon carbide (4H-SiC) MOSFETs are attractive for converters and inverters which require fast switching speed and low specific $R_{on,\,sp}$, owing to superior properties of SiC material and unipolar operation mechanism of MOSFETs[1–4]. SiC trench MOSFETs have high MOS-channel density and high channel mobility on trench sidewalls[5–10]. However, the trench corner suffers from a high electric field in the gate oxide in the blocking mode, which significantly influences the BV value and device reliability. In order to relieve the electric field in the gate oxide, the conventional trench MOSFET (CT-MOS) adopts a PSR under the trench gate[11–16], the double-trench MOSFET (DT-MOS) introduces a PSR to constitute a trench source[17]. Meanwhile, the PSR could also reduce Q_{GD}, which improves the switching behavior. To further reduce Q_{GD} and make the SiC trench MOSFETs more suitable for the application towards high frequency, efforts must be made to decrease the Q_{GD} and improve the dynamic characteristics of SiC trench MOSFETs.

In this paper, a novel trench MOSFET with double shielding structures (DS-MOS) is proposed. Sentaurus TCAD simulation demonstrates that the DS-MOS shows ultralow C_{GD} and Q_{GD}. Moreover, the switching loss of the DS-MOS, CT-MOS and DT-MOS is also discussed in this paper.

2. Device structure and mechanism

Fig. 1(a) shows the schematic structure of the proposed DS-MOS. It features a grounded SG and a trench PSR. The PSR surrounds the trench source and the SG is below the trench control gate. T_{ox} is the distance from the SG to the oxide bottom of trench, and L_{ox} is the distance from the SG to the sidewall of oxide trench. Figs. 1(b) and 1(c) show the schematic structures of the DT-MOS and CT-MOS, respectively. For DS-MOS and the DT-MOS, L_s represents the length of P-base region. For CT-MOS, L stands for the lateral space between the PSR and the gate oxide boundary. The doping concentration and thickness of the drift region are 6×10^{15} cm^{-3} and 10 μm, respectively. The other parameters are shown in Table 1.

Fig. 2 illustrates the operation mechanism of double shielding structures. The structure in Fig. 2(a) is the trench gate MOSFET without the SG and the PSR[18]. The structure in Fig. 2(b)[18, 19] is the split gate MOSFET with the SG and the structure in Fig. 2(c) is the DT-MOS with the PSR. The DS-MOS has both SG and the PSR as shown in Fig. 2(d). On one hand, the SG acts as a shielding region between the gate and drain, and transforms part of the C_{GD} into the C_{DS1} and C_{GS1} in series, as illustrated in Fig. 2(b), the C_{GD} of split trench gate MOSFET can be demonstrated as: $C_{GD} = (C_{GS1}{}^{-1} + C_{DS1}{}^{-1})^{-1} + C_{GD3}$. On the other hand, the PSR reduces the C_{GD} by partially transforming the C_{GD} to C_{GS2} and C_{DS2} in series, as illustrated in Fig. 2(c), the C_{GD} of DT-MOS can be demonstrated as: $C_{GD} = (C_{DS2}{}^{-1} + C_{GS2}{}^{-1})^{-1} + C_{GD4}$. Under combination of the SG and PSR, the C_{GD} of DS-MOS can be demonstrated as: $C_{GD} = (C_{GS3}{}^{-1} + C_{DS3}{}^{-1})^{-1} + C_{GD5} + (C_{GS4}{}^{-1} + C_{DS4}{}^{-1})^{-1}$, as shown in Fig. 2(d). Under the same structure parameters, Fig. 3 compares the simulation results of C_{GD} of the four structures shown in Fig. 2. The results verify the significant improvement of the double shielding structures on C_{GD}. It is obvious that the C_{GD} of the trench MOSFETs with only one shielding structure (Fig. 2(b) and Fig. 2(c)) are smaller than that of the trench MOSFET without shielding structures (Fig. 2(a)). More importantly, the proposed DS-MOS obtains the lowest C_{GD} owing to the interacting shielding effect induced by the double shielding structures.

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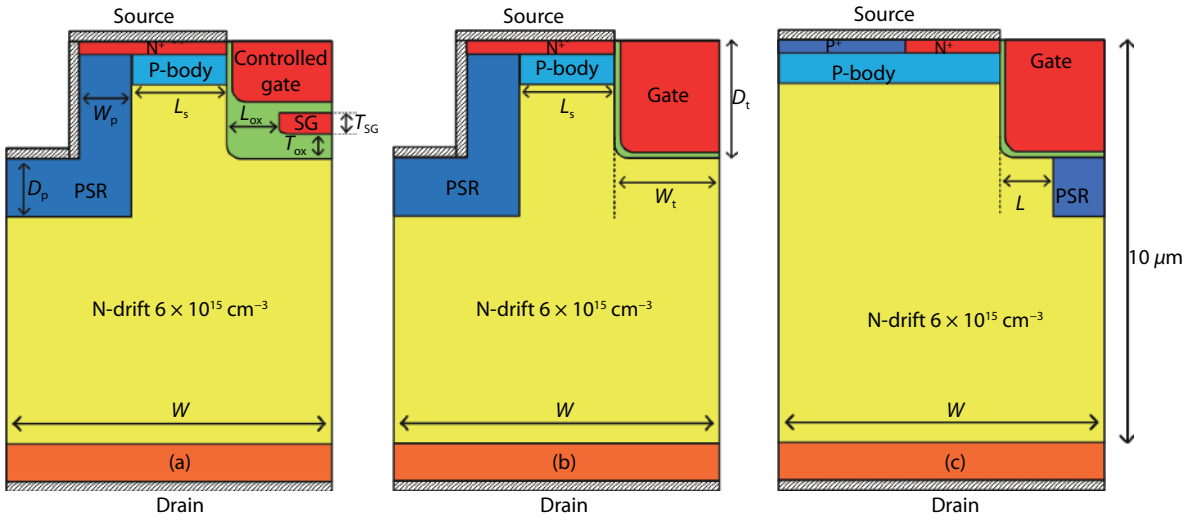

Fig. 1. (Color online) Schematic cross section of the (a) proposed DS-MOS, (b) DT-MOS, and (c) CT-MOS.

Table 1. Simulation parameters of the proposed structure and contrastive structures.

Symbol	Description	Value (μm)
D_p	Vertical implantation depth of the PSR	1.5
W_p	Later implantation width of the PSR	0.2
D_t	Depth of the trench	1.5
T_{SG}	Thickness of split gate	0.2
W	Width of half cell	3.5
W_t	Width of half trench	0.5

3. Results and discussion

In order to ensure good static characteristics of DS-MOS, T_{ox} and L_{ox} should be optimized. In this paper, the breakdown voltage (BV) is defined as the drain voltage at which either the impact ionization integral equals to unity or the electric field in the gate oxide reaches 3 MV/cm, and $R_{on,\,sp}$ is estimated at V_{GS} = 20 V and V_{DS} = 1 V. The channel mobility is set as 15 cm^2/(V·s). Figs. 4(a)–4(c) show the influence of L_s, T_{ox} and L_{ox} on BV, $R_{on,\,sp}$ and FOM (BV^2/$R_{on,\,sp}$) for the DS-MOS. With the

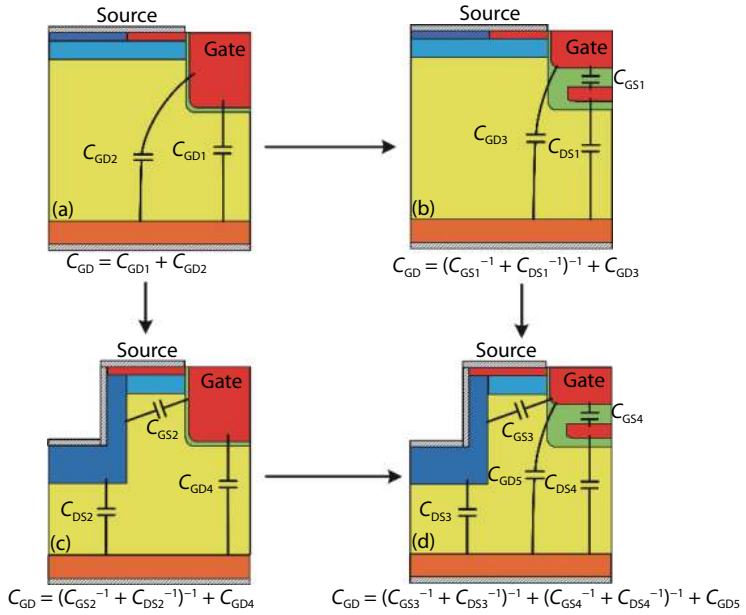

Fig. 2. (Color online) Capacitance distribution for (a) trench gate MOSFET without SG & PSR, (b) split trench gate MOSFET with SG, (c) DT-MOS, and (d) DS-MOS.

increase in L_s, the BV of DS-MOS decreases because the shielding effect of the PSR on gate oxide is weakened and thus the gate oxide breakdown is more likely to occur. In addition, larger L_s widens the current flow path and leads to lower $R_{on,\,sp}$. Therefore, to obtain a desirable trade-off between BV and $R_{on,\,sp}$, ie, the highest FOM = BV^2/$R_{on,\,sp}$ value, the optimum L_s = 1.1 μm is chosen. Fig. 4(d) depicts the influences of the T_{ox} and L_{ox} on the electron density. In the on state, the SG, oxide and N-drift form the MIS structures (marked by the black dotted line in Fig. 4(d)). The MIS structure forms depletion regions in the drift region (the depletion region boundaries are marked by the white line), and then JFET resistance is generated. High L_{ox} and T_{ox} values will weaken the lateral depletion effect of the MIS structure and maintain wide electron current path, which contributes to a low $R_{on,\,sp}$. Therefore, the optimized L_{ox} is 0.3 μm. Under the optimized L_s and L_{ox}, T_{ox} will also affect the

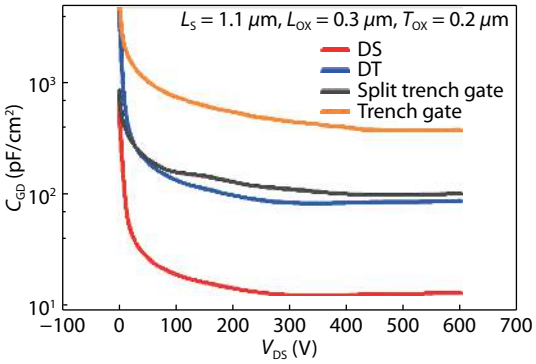

Fig. 3. (Color online) C_{GD} of the four structures in Fig. 2.

length of the accumulation channel (marked by the two-way arrow). Considering the BV of DS-MOS, the optimized T_{ox} and L_{ox} are 0.2 and 0.3 μm, respectively. In conclusion, the optimized $R_{on,\,sp}$ is 4.08 mΩ·cm² (denoted as point "A") and BV is 1435 V (denoted as point "B") in Fig. 4(b).

Fig. 5 shows the dependences of C_{GD} on L_s, T_{ox} and L_{ox} for DS-MOS. The C_{GD} slowly increases with the increase in T_{ox}, the reason is that the shielding effect is weakened if the distance between the SG and controlled gate electrode shortens. For L_s, the increasing L_s weakens the shielding effect of the PSR against the gate–drain coupling, thus the C_{GD} increases. Obviously, the C_{GD} is more sensitive to L_{ox} than T_{ox} at the same L_s, which means reducing the overlap of the gate–drain is more important than the location of the SG. Owing to the weakened

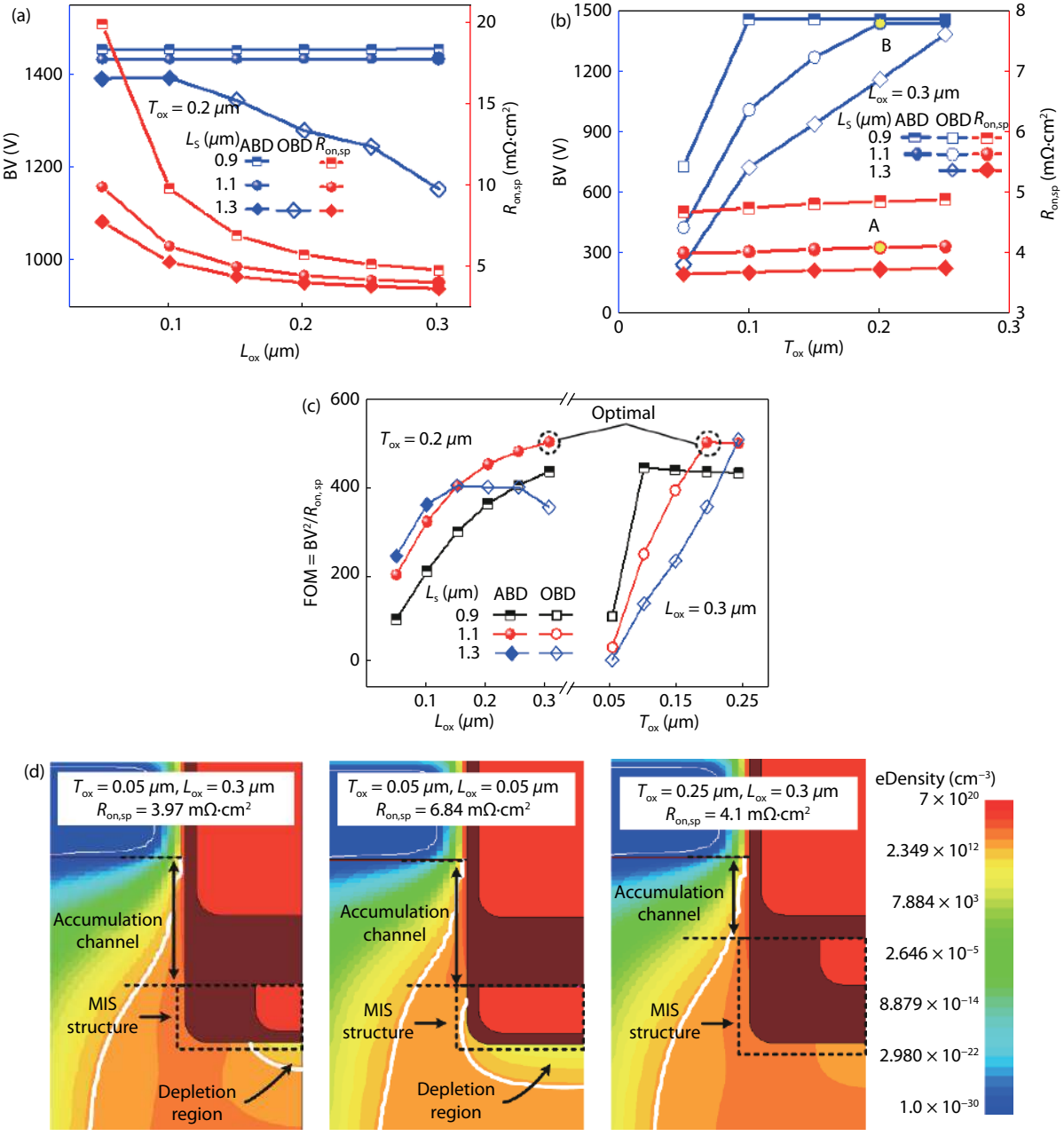

Fig. 4. (Color online) Tradeoff between $R_{on,\,sp}$ (@V_{GS} = 20 V, V_{DS} = 1 V) and BV(@V_{GS} = 0 V) for the DS-MOS (a) with varied L_{ox} as the function of L_s, T_{ox} is set as 0.2 μm and (b) with varied T_{ox} as the function of L_s, L_{ox} is set as 0.3 μm. OBD means oxide breakdown and ABD means avalanche breakdown. Optimized $R_{on,\,sp}$ = 4.08 mΩ·cm² (denoted as "A") and BV_R = 1435 V (denoted as "B"). (c) Influence of T_{ox}, L_{ox}, and L_s on FOM. (d) On-state depletion boundary (@V_{GS} = 20 V, V_{DS} = 1 V) and electron density with varied T_{ox} and L_{ox} at L_s = 1.1 μm. The white lines are the depletion boundaries.

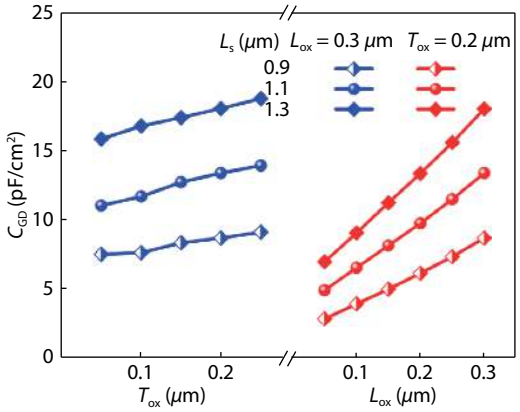

Fig. 5. (Color online) Dependence of C_{GD} (@V_{DS} = 600 V) on L_s, T_{ox} and L_{ox} for DS-MOS.

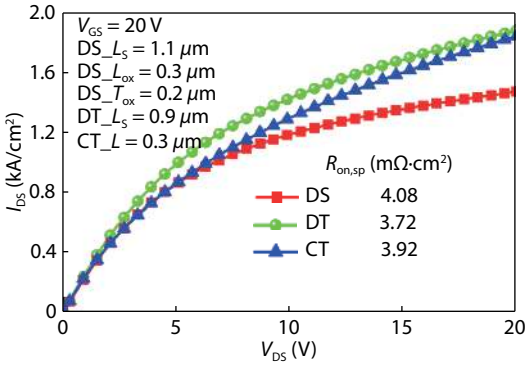

Fig. 6. (Color online) On-state output characteristic curves of the three devices at V_{GS} = 20 V.

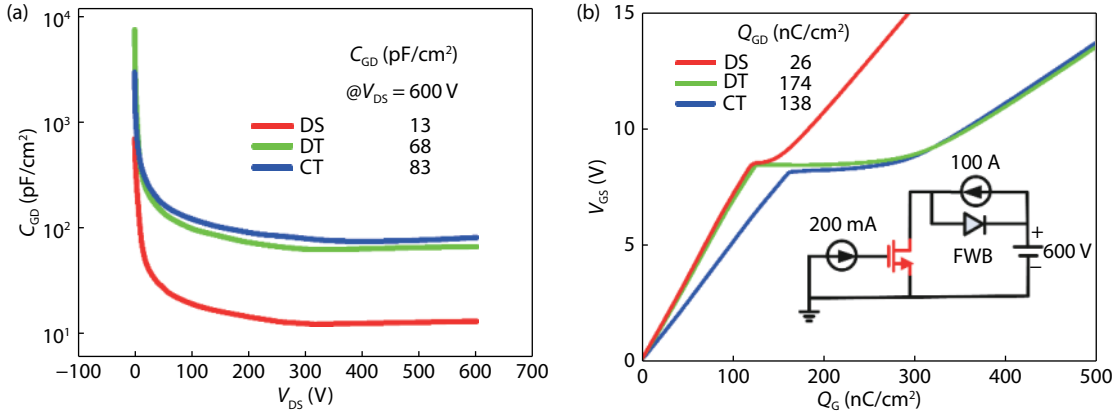

Fig. 7. (Color online) Comparison of (a) C_{GD} and (b) Q_{GD} of the DS-MOS, DT-MOS and CT-MOS. The extracted Q_{GD} is 26, 174 and 138 nC/cm², respectively. The inset is the simulation circuit.

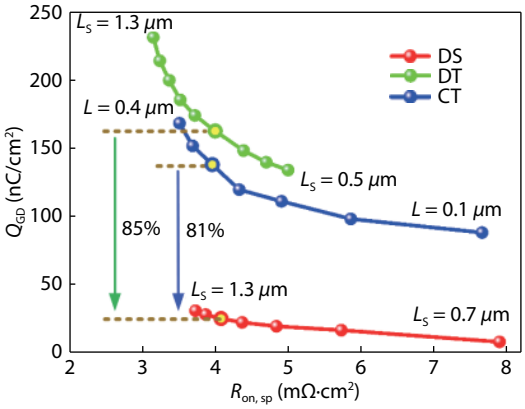

Fig. 8. (Color online) Tradeoff between $R_{on,sp}$ (V_{GS} = 20 V, V_{DS} = 1 V) and Q_{GD}.

shielding effect of the PSR on C_{GD} with the increase in L_s, the influence of the L_{ox} on C_{GD} becomes more important.

Fig. 6 shows the on-state output characteristic curves of the DS-MOS, DT-MOS and CT-MOS. To obtain the highest FOM ($BV^2/R_{on,sp}$), the optimized values of L_s = 0.9 μm and L = 0.3 μm are chosen for the DT-MOS and CT-MOS. The $R_{on,sp}$ values of DS-MOS, DT-MOS and CT-MOS are 4.08, 3.72 and 3.96 mΩ·cm², respectively. The $R_{on,sp}$ of the proposed device is a little bit higher than the other devices because of the JFET resistance generated by the SG and PSR, as shown in Fig. 4(d). With the increase in V_{DS}, the JFET resistance increases and then the DS-MOS shows the lowest saturation current. Therefore, the DS-MOS is constructive to improve the short circuit capability of the device.

Fig. 7 compares the C_{GD} and Q_{GD} of the DS-MOS, DT-MOS and CT-MOS. Owing to the shielding effect of the SG and PSR, the DS-MOS has the lowest C_{GD} compared with other two devices. The C_{GD} (@V_{DS} = 600 V) of the DS-MOS, DT-MOS and CT-MOS are 13, 68 and 83 pF/cm², respectively. The DS-MOS exhibits the shortest Miller platform and smallest Q_{GD} of 26 nC/cm² compared with the DT-MOS and CT-MOS, as shown in Fig. 7(b). Compared with the DT-MOS and CT-MOS, the Q_{GD} of DS-MOS is reduced by 85% and 81%, respectively.

Fig. 8 shows the tradeoff between $R_{on,sp}$ and Q_{GD} for the DS-MOS, DT-MOS and CT-MOS. A large L_s and L can reduce the JFET resistance and the $R_{on,sp}$. For the DS-MOS and the DT-MOS, the effect is weakened as L_s and L increase. The increase in L_s results in an increase in C_{GD} and Q_{GD} because the shielding effect is weakened. The higher L directly causes a larger overlap area between the gate electrode and the drain electrode for the CT-MOS, and thus higher C_{GD} and Q_{GD} are obtained. What's more, the protection on gate oxide caused by the PSR becomes weak. Under the almost same $R_{on,sp}$, the Q_{GD} of the DS-MOS is reduced by 85% and 81% compared with that of DT-MOS and CT-MOS, respectively.

Figs. 9(a) and 9(b) show the turn-off waveforms and simulation circuit of the three MOSFETs. The MOSFETs turn off at t = 20 μs and the devices are all 1 cm². A SiC junction barrier Schot-

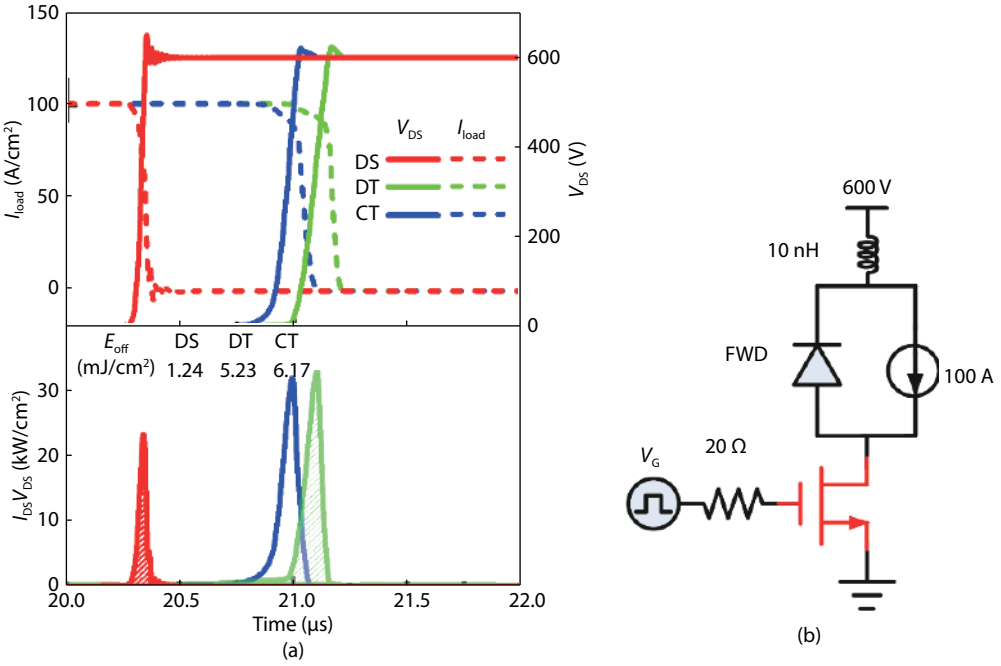

Fig. 9. (Color online) (a) Turn-off waveforms of the DS-MOS, DT-MOS and CT-MOS, respectively. (b) Simulation circuit of the turn-off characteristics.

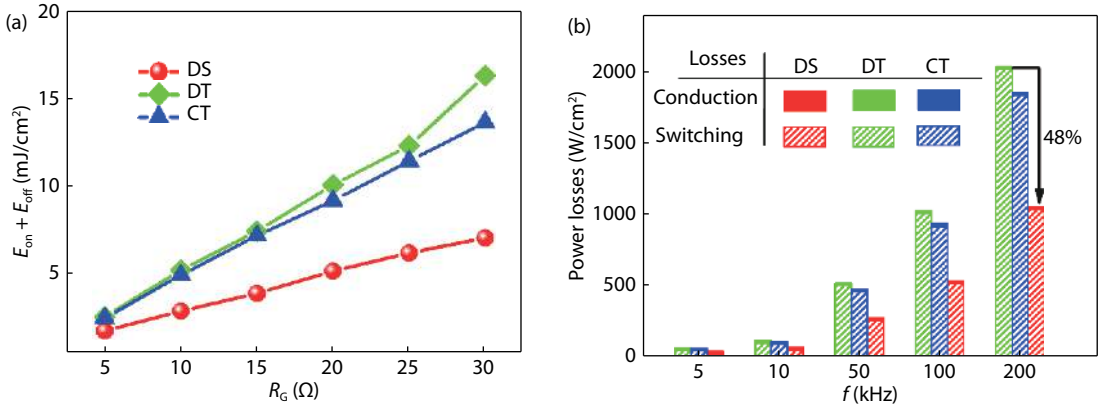

Fig. 10. (Color online) (a) Dependence of $E_{on} + E_{off}$ on R_G (V_{DS} = 600 V, V_{GS} = 0/20 V, I_{load} = 100 A/cm²). (b) Comparison of power losses as a function of switching frequency f (R_G = 20 Ω).

Table 2. Performance comparison of the three MOSFETs.

Parameter	DS-MOS	DT-MOS	CT-MOS
dV/dt (kV/μs)	16.1	4.7	5.5
dI/dt (kA/μs)	2.6	2.2	1.6
Q_{GD} (nC/cm²)	26	174	138
C_{GD} (pF/cm²) (@V_{DS} = 600 V)	13	68	83
$R_{on,sp}$ (mΩ·cm²)	4.08	3.72	3.96
$R_{on,sp}Q_{GD}$ (mΩ·nC)	106	647	546
V_{BR} (V)	1435	1460	1233

tky diode (JBS) is used as the freewheeling diode and the gate resistor (R_G) is set as 20 Ω. Owing to ultralow Q_{GD} for the DS-MOS, the high dV/dt and dI/dt values are obtained, leading to 76% and 80% reduction in turn-off losses (E_{off}) compared with that of the DTMOS and CT-MOS, respectively. The specific dV/dt and dI/dt of the three MOSFETs are shown in Table 2.

Fig. 10(a) shows the influence of the R_G on switching loss (E_{on} + E_{off}) in one switching cycle. Compared with the DT-MOS and the CT-MOS, the DS-MOS exhibits the lowest switching loss at different R_G. As the R_G increases, the difference of the switching loss among the three MOSFETs increases. The total power losses P_t of the device consist of conduction losses and switching losses, and can be calculated using[20, 21]:

$$P_t = dR_{on,sp}I_d^2 + f(E_{on} + E_{off}),$$

where d stands for the duty cycle which defined as the ratio of the time the MOSFET conducts to a switching period, and f is the switching frequency. Fig. 10(b) shows the power losses as a function of switching frequency and the duty cycle is set as 0.5. With the increasing switching frequency, switching losses become the dominant power dissipation and the advantage of switching performance of DS-MOS increases. When operating at 200 kHz, the DS-MOS realizes 48% and 43% reduction in the power losses compared with the DT-MOS and the CT-MOS. Table 2 summarizes the performance parameters for the three devices. Obviously, the DS-MOS obtains better performance than other two MOSFETs.

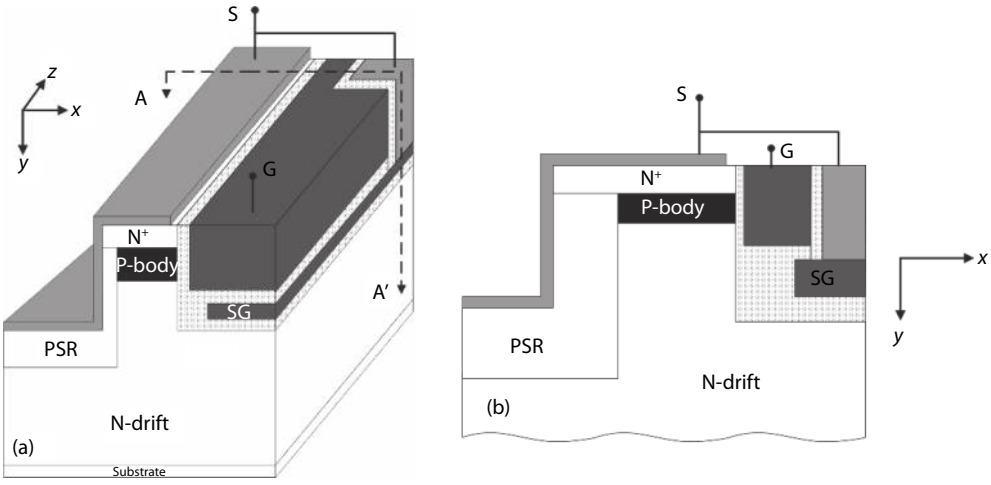

Fig. 11. (a) 3-D view of DS-MOS. (b) Schematic cross section along the cut line AA′.

Fig. 11(a) shows the 3-D view of DS-MOS. The SG is grounded through the contact holes along the *z* axis and the schematic cross section along the cut line AA′ is shown in Fig. 11(b). To avoid the electric connection between the gate and SG, there is a dielectric layer between them.

4. Conclusion

A novel 4H-SiC trench MOSFET with double shielding structures is proposed in this paper. The double shielding structures include a split gate and a trench P^+ shielding region. The Q_{GD} of the proposed DS-MOS reduced by 85% and 81% compared with that of DT-MOS and CT-MOS without sacrificing BV, leading to a significantly improvement in the switching performance. Furthermore, the FOM defined as $R_{on,\,sp}Q_{GD}$ of the DS-MOS is decreased by 84% and 81% in comparison with that of the DT-MOS and CT-MOS, respectively, and thus the power dissipation is reduced, which makes the DS-MOS suitable for the high frequency and high power applications.

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