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Research for radiation-hardened high-voltage SOI LDMOS

Yanfei Li†, Shaoli Zhu, Jianwei Wu, Genshen Hong, and Zheng Xu

The 58th Research Institute of China Electronics Technology Group Corporation, Wuxi 214035, China

Abstract: Based on the silicon-on-insulator (SOI) technology and radiation-hardened silicon gate (RSG) process, a radiation-hardened high-voltage lateral double-diffused MOSFET (LDMOS) device is presented in this paper. With the gate supply voltage of 30 V, the LDMOS device has a gate oxide thickness of 120 nm, and the RSG process is effective in reducing the total ionizing dose (TID) radiation-induced threshold voltage shift. The p-type ion implantation process and gate-enclosed layout topology are used to prevent radiation-induced leakage current through a parasitic path under the bird's beak and at the deep trench corner, and the device is compatible with high-voltage SOI CMOS process. In the proposed LDMOS, the total ionizing dose radiation degradation for the ON bias is more sensitive than the OFF bias. The experiment results show that the SOI LDMOS has a negative threshold voltage shift of 1.12 V, breakdown voltage of 135 V, and off-state leakage current of 0.92 pA/μm at an accumulated dose level of 100 krad (Si).

Key words: radiation-hardened; RGS; total ion dose; threshold voltage shift

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1. Introduction

As critical components, lateral double-diffusion MOSFETs (LDMOS) play an important role in analog switches and high voltage driver ICs applied to space and military electronic systems such as spacecraft and satellites, which shows a strong sensitivity to ionizing radiation[1–3]. The generation of charges by ionizing radiations in CMOS materials may induce stable defects in dielectrics[4–6] used in the fabrication process. According to Refs. [7, 8], this phenomenon results in degradation of modern CMOS integrated circuits, such as threshold voltage shifts, intense leakage currents and formation of parasitic conduction paths[9, 10]. Compared with the low-voltage integrated circuits, the high-voltage MOSFET is more sensitive to the total ionizing dose (TID) due to the thicker gate oxide.

Many efforts have been made to mitigate the radiation-induced leakage current and very high levels of radiation hardness have been achieved, such as enclosed layout transistors (ELTs) to eliminate drain to source leakage or p-type diffusion guard rings to block inter-device leakage paths[11, 12]. Moreover, advanced silicon-on-insulator (SOI) technology[13–16] is effective in eliminating the radiation-induced junction leakage and neighboring transistors' leakage, as well as the single event latch-up (SEL). Based on high-voltage MOSFET technology, a substantial number of radiation-hardened products for hi-reliability and space marketplaces have been developed. Nevertheless, there is no radiation-hardened high voltage circuit products reported at home.

In this work, a high-voltage SOI LDMOS device is reported based on the SOI technology and radiation-hardened silicon gate (RSG) process, together with p-type ion implantation process and gate-enclosed layout. The proposed technique reduces the threshold voltage shift and eliminates the TID radiation-induced leakage current, particularly the isolation leakage. With the techniques, we have designed and fabricated the high-voltage LDMOS device in order to evaluate the TID radiation characteristic. Details will be presented in Section 2 and Section 3.

Correspondence to: Y F Li, mama_1015@163.com
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2. Device and experimental techniques

Fig. 1 shows a band diagram of a MOS structure with a positive applied gate bias. During the total ionizing radiation, the massive electron-hole pairs are generated in the oxide layers. Due to the high mobility, the electrons are quickly swept out the oxide layers by the applied electric field and are absorbed by the power. However, some of the holes which escape initial recombination will transport through the oxide toward the SiO_2/Si interface by hopping through localized states in the oxide. As the holes approach the interface, some fraction will be captured, forming a positive oxide-trapped charge[17–20]. These trapped charges cause a negative voltage shift, while the radiation-induced buildup of interface traps right at the Si/SiO_2 interface, which decrease the mobility of carriers and increase the threshold voltage of n-channel MOS transistors. According to the mechanism, the threshold voltage shift results from the creation of both oxide-trapped charges and interface traps during irradiation.

Radiation-induced oxide-trapped charges and interface-trapped charges will also occur in field oxides, buried oxides, and deep trench isolation oxides in the SOI device, which causes device degradation and circuit failure. In this work, the SOI LDMOS device was designed by the radiation-hardened high-voltage SOI CMOS process, as shown in Fig. 2. With the gate supply voltage of 30 V, the radiation-induced threshold voltage shift becomes more intense owing to the high gate oxide thickness of 120 nm. The radiation-hardened silicon gate process was used to address the problem and improve the ability of anti-radiation, which also applies to the field oxide layer.

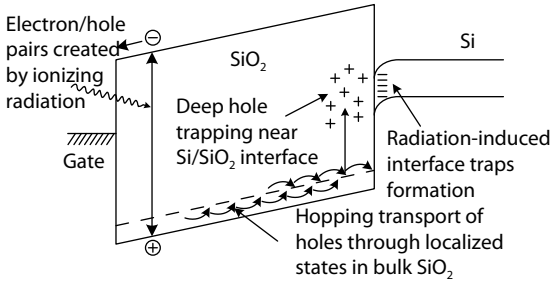

Fig. 1. Band diagram for MOS structure with positive gate bias, indicating main processes for radiation-induced charge generation.

Table 1. Values of main structure parameters for the proposed SOI LDMOS device.

Parameter	Value
Gate oxide thickness	120 nm
The thickness of p-type epitaxial film	8 μm
The thickness of buried oxide layer	3 μm
The resistivity of p-type epitaxial film	10–20 Ω·cm
Width/length	100 μm/4 μm
Device structure	Gate-enclosed layout

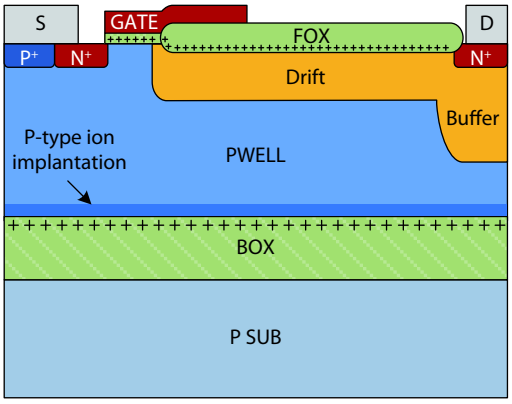

Fig. 2. (Color online) The proposed radiation-hardened high-voltage LDMOS after TID radiaiton.

The p-type ion implantation process is applied to restrain the formation of an inversion layer underneath the top silicon layer because of the radiation-induced positive charge along the deep trench isolation oxide and buried oxide, which results in back gate leakage current. To avoid large electronic field peak near the drain N$^+$/PWELL junction leading to decrease of breakdown voltage, an n-type buffer layer is designed for the device. Table 1 presents the values of several main structure parameters. According to the influence of single event gate rupture effect, the thickness of radiation-hardened gate oxide is 120 nm, as well as the channel length of 4 μm due to the single event gate burnout effect. The thickness of top silicon layer is the key factor, which directly affects the breakdown voltage and TID characteristics. Based on the ion implantation process and epitaxial process, the p-type ion implantation is implemented in the thick top silicon layer. The gate-enclosed layout together with guard rings is used in radiation environments to prevent the leakage current through a radiation-induced lateral path under the bird's beak and at the deep trench corner.

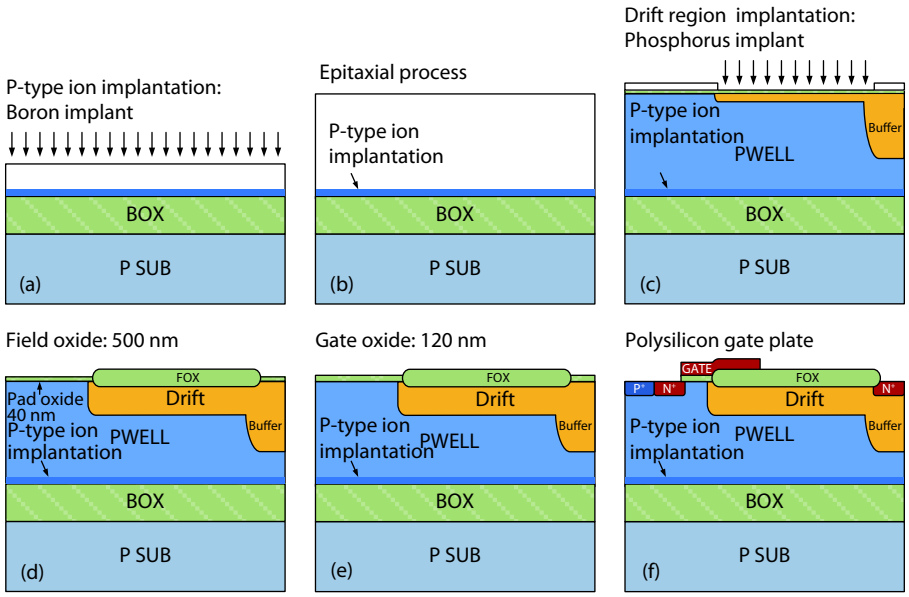

Fig. 3. (Color online) Major process steps of the SOI LDMOS device.

Fig. 3 shows the major process steps of the proposed SOI LDMOS device. To restrain TID radiation-induced back channel inversion and leakage current, p-type impurity is introduced underneath the thin top silicon layer, and the diffusion process is applied to ensure the most impurity at the Si/SiO$_2$ interface (Fig. 3(a)). Based on an epitaxial technique, the thick p-type epitaxial film of 8 μm is fabricated on p-type top silicon substrate, shown in Fig. 3(b). For the reported LDMOS, a suitable junction depth of the buffer layer is achieved by ion implantation and anneal, which mitigate the electronic field peak at the drain region. But, too large junction depth causes the decrease of breakdown voltage due to the radiation-induced punch-through. After the self-aligned phosphorus ion implant is performed (Fig. 3(c)), the radiation-hardened field oxide of 500-nm thickness is grown with low oxidation temperature and excellent ambient, shown in Fig. 3(d). The radiation-hardened gate oxide of 120-nm thickness is obtained with low radiation-induced oxide-trapped and interface-trapped char-

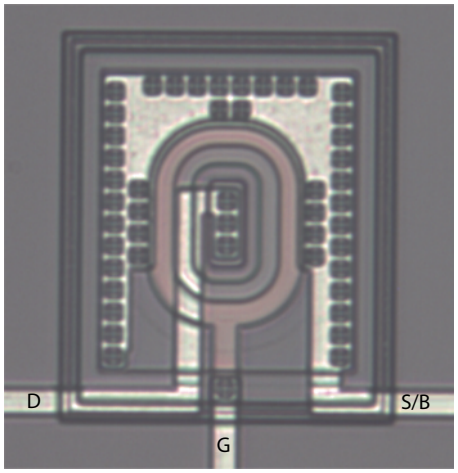

Fig. 4. (Color online) The chip photo of the proposed LDMOS.

Table 2. Bias conditions definition.

Bias state	V_D (V)	V_G (V)	V_{BS} (V)	V_{SUB} (V)
ON bias	0	30	0	0
OFF bias	100	0	0	0

ges, which reduces threshold voltage shift after irradiation (Fig. 3(e)). Meanwhile, the polysilicon gate plate is used to improve the breakdown voltage without increasing process cost (shown in Fig. 3(f)). Fig. 4 presents the chip photo of the SOI LDMOS device, which is designed and fabricated in this process to fully evaluate the radiation-hardened technique.

3. Results and discussion

The n-type SOI LDMOS samples were fabricated by the radiation-hardened silicon gate process and SOI technology with

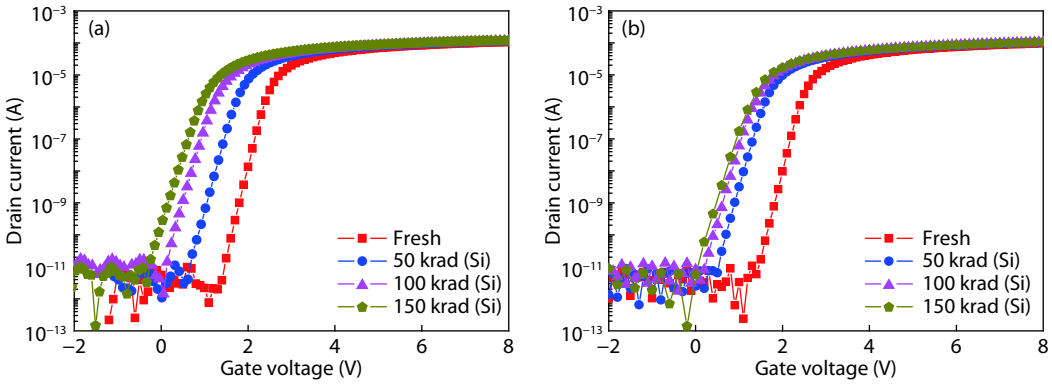

Fig. 5. (Color online) Sub-threshold curves for the LDMOS with W/L = 100 μm /4.0 μm. The experiment measurements were obtained with V_D = 0.1 V and $V_{BS} = V_{SUB}$ = 0 V. (a) ON bias. (b) OFF bias.

the field oxide thickness of 500 nm and the typical width/length of 100 μm/4 μm. To evaluate the total ionizing dose radiation response of the proposed technique, irradiation experiments have been performed with Co^{60} radiation source at a dose rate of 50 rad(Si)/s. Table 2 shows the bias conditions of the SOI LDMOS during TID irradiation. The body electrode is shorted to the source electrode, and the body-source bias voltage was named V_{BS}. The condition of ON bias was V_G = 30 V and $V_D = V_{BS} = V_{SUB}$ = 0 V, and the condition of OFF bias was V_D = 100 V and $V_G = V_{BS} = V_{SUB}$ = 0 V. With the bias conditions, the devices were irradiated with the different TID levels of 50, 100, and 150 krad (Si).

Fig. 5 shows the sub-threshold characteristics for the radiation-hardened SOI LDMOS irradiated under ON bias and OFF bias. The LDMOS has a typical threshold voltage about 2.35 V at the drain voltage of 0.1 V. After irradiation, the most significant change of the device is the threshold voltage shift due to positive charges accumulation in the thick gate oxide. With the increase of the radiation dose, the threshold voltage decreases, as well as the threshold voltage shift. Compared with the OFF bias, the ON bias is sensitive to the TID effect, and the threshold voltage shifts increase. The off-state leakage current in the transfer curves of the device remain almost constant because of the p-type ion implantation process together with gate-enclosed layout. The LDMOS has small sub-threshold slope degradation which implies that there are a few interface-trapped charges generated at the Si/SiO_2 interface highly dependent on oxide processing, applied field, and process temperature.

Fig. 6 exhibits the transconductance (g_m) curves before and after total dose irradiation. During irradiation, the transconductance curves greatly shift negatively for the ON bias and OFF bias, which comes from the oxide-trapped charges in the thick gate oxide. The phenomenon is similar to the sub-threshold curves as shown in Fig. 5. Simultaneously, the generation of radiation-induced interface-trapped charges at the thick gate oxide/top silicon interface reduces the transconductance. As the radiation dose increases, the maximal transconductance decreases. With TID levels up to 100 krad (Si), the maximal transconductance values reduce to 53.1 and 52.8 μS for the ON bias and OFF bias, respectively. This indicates that the radiation-hardened technique efficiently cuts down the radiation-induced interface-trapped charges and enhances the ability of anti-irradiation.

As we know, the threshold voltage shift (ΔV_{TH}) of the device results from both the radiation-induced oxide-trapped charge and the interface-trapped charge. Fig. 7 shows the threshold voltage shifts of the SOI LDMOS device extracted from the curves of Fig. 5. After irradiation, the threshold voltage has a negative shift along the voltage axis with ON bias and OFF bias. With the radiation dose of 50 krad (Si), the ΔV_{TH} for ON bias is obviously less than for OFF bias. However, for higher total radiation dose, the ON bias leads to more evident threshold voltage shifts due to the great effect of high electric field on the gate oxide. At a total dose of 100 krad (Si), the threshold voltage shifts are −1.12 and −1.01 V for the ON bias

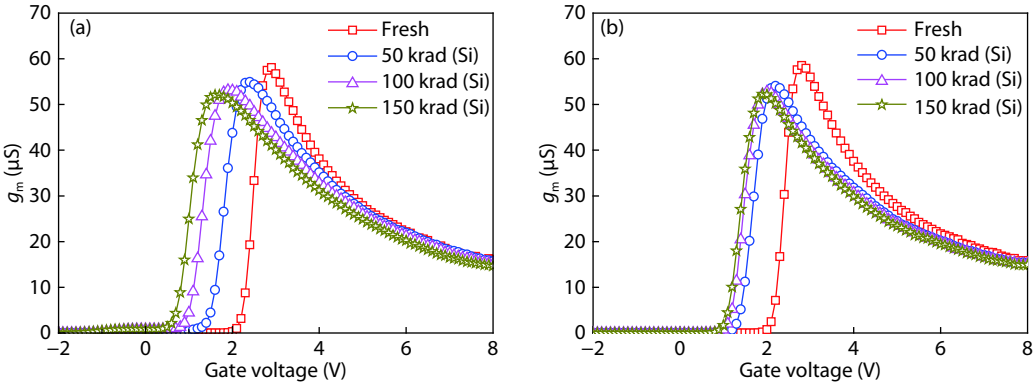

Fig. 6. (Color online) Transconductance curves for (a) ON bias and (b) OFF bias.

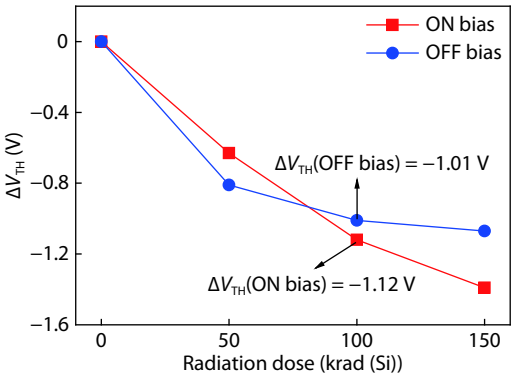

Fig. 7. (Color online) Threshold voltage shifts with radiation dose.

and OFF bias, respectively. For TID higher than 100 krad (Si), the main problem is severe threshold voltage shift owing the gate oxide thickness of 120 nm.

Figs. 8(a) and 8(b) show the output characteristic curves of the SOI LDMOS with different gate-source bias voltage (V_{GS}) for ON bias and OFF bias. After irradiation to 100 krad (Si), it can be seen that the curves integrally shift up, and the phenomenon appears more obvious for ON bias and the higher V_{GS}. With V_D = V_G = 30 V, the drain current shifts for ON bias and OFF bias are 15.9% and 9.44%, respectively. The increase of current can be attributed to two aspects, the influence of the gate oxide and the field oxide in the drift region. During exposure to ionizing irradiation, a mass of oxide-trapped charges

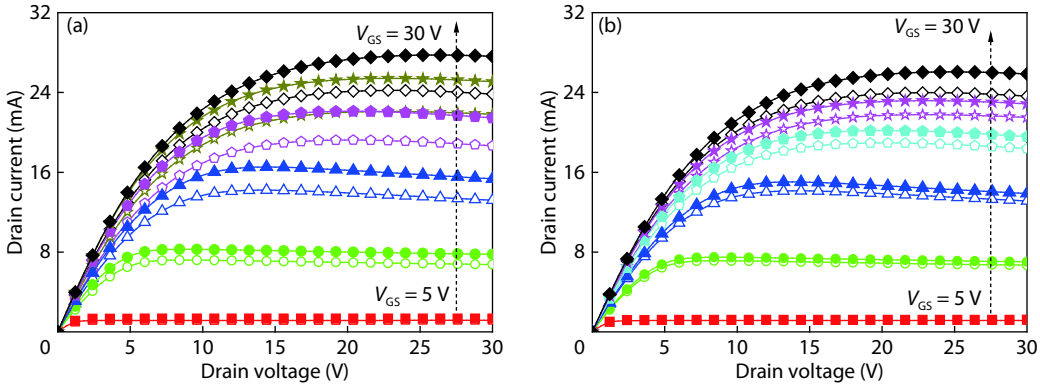

Fig. 8. (Color online) Output characteristics curves of the proposed SOI LDMOS with a dose level of 100 krad (Si). (a) ON bias. (b) OFF bias. The tests were performed at gate-source voltages of 5, 10, 15, 20, 25, and 30 V.

in the gate oxide increasing the electrons in the channel region, and the channel resistance is decreased. Simultaneously, much more oxide-trapped and interface-trapped charges generated at the field oxide because of its softer and thicker oxide layer, which also leads to the increase of the on-state drain current.

Fig. 9 shows the drain current as a function of the drain voltage before and after 100 krad (Si) irradiation. With n-type buffer layer at the drain region and the poly field plate, the SOI LDMOS device achieves a breakdown voltage of 179 V. Compared with gate oxide, more oxide-trapped charges and interface-trapped charges are induced in the field oxide due to thicker oxide layer. At the field region and back-gate, radiation-induced leakage channel is restrained by the p-type ion implantation and guard rings. The field oxide in the drift region introduces a mass of oxide-trapped charges and interface-trapped charges, which results in the more off-state leakage current of 92 pA with V_D = 100 V and a dose level of 100 krad (Si). Moreover, the degeneration of breakdown voltage comes from radiation-induced charges breaking the charge-balance in drift region. After irradiation of 100 krad (Si), the breakdown voltages of 135 and 176 V are obtained for ON bias and OFF bias, respectively. Obviously, OFF bias is more resistant to radiation damage than ON bias.

4. Conclusion

In the paper, the threshold voltage shift, leakage current, transconductance, and breakdown voltage of the proposed LDMOS designed by the radiation-hardened SOI process are evaluated before and after irradiation. For the SOI LDMOS device, the experimental results exhibit that the main problem of the total dose effect is the threshold voltage shift negatively and

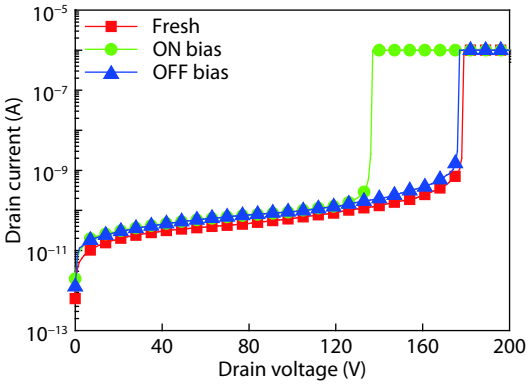

Fig. 9. (Color online) Drain current as a function of the drain voltage before and after irradiation of 100 krad (Si).

breakdown voltage degradation due to the much thicker gate oxide for the high supply voltage and field oxide of the drift region, respectively. The oxide-trapped and interface-trapped charges are responsible for the increase of the on-state current during irradiation. The experiment results also reveal that the TID radiation effects for the device have a strong dependence on bias conditions during radiation, and the ON bias is more sensitive to the TID radiation effect compared with OFF bias. The p-type ion implantation process together with gate-enclosed layout restrain the parasitic channel and sub-threshold leakage current, and the off-state leakage current at the drain voltage of 100 V increases by below one order of magnitude after 100 krad (Si) dose of irradiation.

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