Journal of Semiconductors
(2019) 40, May 2019 | JOS

NANOTECHNOLOGY

Scalable fabrication of geometry-tunable self-aligned superlattice photonic crystals for spectrum-programmable light trapping

Nano Energy, 2019, doi: 10.1016/j.nanoen.2019.01.074

Superlattice photonic crystals (SPhCs) possess considerable potentials as building blocks for constructing high-performance devices because of their great flexibilities in optical manipulation. From the prospective of practical applications, scalable fabrication of SPhCs with large-area uniformity and precise geometrical controllability has been considered as one prerequisite but still remains a challenge.

Recently, Lei Group developed an anodic aluminum oxide template-guided approach to realize Ni SPhCs with the maximum area (~500 mm^2). By virtue of the dual-pore self-alignment effect arising from the periodic anodization electric fields, uniform structures over large areas were obtained for Ni SPhCs. Meanwhile, the geometrical parameters for every array of nanopores in terms of pore depth, size, and morphology can be independently controlled due to the sequential pore-opening, thus leading to omnidirectional stably-strong (~95%) light absorption spectra. Optical simulations elucidated that surface plasmon resonance and cavity resonance are responsible for the superior light trapping. Notably, the fabrication technique is applicable to Ni SPhCs with different periodicities, leading to spectrally programmable light absorption spectra. With Ni SPhCs as solar absorber, the water evaporation efficiency of a solar steam generation system and the open circuit voltage of a solar thermoelectric generator demonstrated 2.3 and 2.5 times improvement, respectively.

Zhijie Wang (Institute of Semiconductors, CAS, Beijing, China)
doi: 10.1088/1674-4926/40/5/050201

AI PROCESSOR

Energy-efficient reconfigurable AI processor

IEEE J. Solid-State Circuits, **54**, 1120 (2018)

High computational energy-efficiency and rapid real-time response are the major concerns for applications of artificial intelligence in low-power mobile and Internet of Things devices with limited storage capacity. Due to the outstanding superiority of less memory requirement, low computation overhead and negligible accuracy degradation, deep neural networks with binary/ternary weights (BTNNs) have been widely adopted to replace traditional full-precision neural networks. Although previous hardware implementations have been proposed to accelerate the inference of BTNNs by utilizing the multiplication-free feature, some implicit characteristics in BTNN convolution, such as high arithmetic complexity and numerous redundant operations, are never exploited.

This paper proposes four optimization techniques to fully exploit these implicit characteristics for higher energy-efficiency in low-power devices. First, a feature-integral-based convolution (FIBC) method is proposed to reduce the arithmetic complexity of convolutional layers. Second, a kernel-transformation-feature-reconstruction (KTFR) convolution method is presented to remove redundant operations in BTNN convolution. Third, a hierarchical load-balancing mechanism (HLBM) is designed to eliminate zero value computation and improve resource utilization. Finally, a joint optimization approach for convolutional layers is proposed to search optimal calculation pattern for each layer. Based on the proposed four techniques, a reconfigurable processor in a 28-nm CMOS technology is designed to accelerate the inferences of BTNNs with flexible data bit-width. The four proposed techniques improve energy efficiency by 2.07×, 1.65×, 1.25× and 2.24× for BTNNs respectively, compared with the baseline implementation which disables the proposed techniques. Benchmarked with binary-weight AlexNet, the processor achieves an energy efficiency of 19.9 TOPS/W at 200 MHz and 0.9 V.

Nanjian Wu (Institute of Semiconductors, CAS, Beijing, China)
doi: 10.1088/1674-4926/40/5/050202

TOPOLOGICAL QUANTUM COMPUTING

A theoretical explanation of the decays of Majorana oscillations

Phys. Rev. Lett., 2019, doi: 10.1103/PhysRevLett.122.147701

Majorana zero modes in the hybrid semiconductor-superconductor nanowire is one of the promising candidates for topological quantum computing. Recently, in nanowires with a superconducting island, the signature of Majorana zero modes can be revealed as a subgap state whose energy oscillates around zero in magnetic field. This oscillation was interpreted as overlapping Majoranas. However, the oscillation amplitude either dies away after an overshoot or decays, sharply opposite to the theoretically predicted enhanced oscillations for Majorana bound states, as the magnetic field increases. Several theoretical studies have tried to address this discrepancy, but are partially successful. This discrepancy has raised the concerns on the conclusive identification of Majorana bound states, and has even endangered the scheme of Majorana qubits based on the nanowires.

Recently, this problem has been solved by a group led by Professor Hai-Zhou Lu and Professor X. C. Xie. They consider a non-uniform spin-orbit coupling strength along the nanowire, e.g. with a steplike distribution. The steplike spin-orbit coupling is reasonable because the gates apply a nonuniform electrostatic potential and spin-orbit coupling depends on the electrostatic fields perpendicular to the nanowire. Moreover, the presence of the superconductor can also modify the electrostat-

Journal of Semiconductors
(2019) 40, May 2019

ic field in the nanowire due to screening effect and work-function mismatch between the superconductor and semiconductor. Thus the spin-orbit coupling is well expected to be nonuniform from the nanowire covered with superconductor to the part (tunnel barrier region) without the superconductor. Additionally, they found that these decaying oscillations caused by the steplike spin-orbit coupling are ubiquitous, also present for trivial Andreev bound states. Though many previous works have addressed non-uniform chemical potential/pairing in nanowires, this work is the first to point out the crucial role of non-uniform spin-orbit coupling and its direct link to the decaying subgap state oscillations.

Dong Pan (Institute of Semiconductors, CAS, Beijing, China)
doi: 10.1088/1674-4926/40/5/050203

SPTRONICS

Artificial neuron and synapse in spintronics devices

Adv. Mater., 2019, doi: 10.1002/adma.201900636

Neuromorphic computing is the development of computing schemes inspired by the processing of information in the brain, which can execute complex tasks very efficiently using an architecture that is completely different from that of semiconductor chips. Recently, researchers from Tohoku University have realized an artificial neuron and synapse in spintronics devices, which are promising for future energy-efficient and adoptive computing systems, as they behave like the spiking neural network in human brains.

The research group had previously developed a functional material system consisting of antiferromagnetic and ferromagnetic materials. This time, they prepared artificial neuronal and synaptic devices microfabricated from the material system, which demonstrated fundamental behavior of biological neuron and synapse, i.e., "leaky integrate-and-fire" and "spike-timing-dependent plasticity", respectively, based on the dynamics of spin-orbit torque switching. The spintronics neuron and synapse could form a currently lacking hardware basis for neuromorphic computing, which would advance the fields of neuromorphic computation and neuroscience by enabling full-scale brain emulations, artificial intelligence, and human–machine interfaces.

Dahai Wei (Institute of Semiconductors, CAS, Beijing, China)
doi: 10.1088/1674-4926/40/5/050204

INTEGRATED OPTICAL BUFFER

Large-capacity and low-loss integrated optical buffer

Opt. Express, **27**, 11585 (2019)

Trapping light in a photonic integrated circuit can find many applications, such as optical storage, optical-packet switching, optical sensing and microwave photonics. Although there are many ways to implement an integrated optical buffer, such as the use of ring resonators, photonic crystals, Bragg gratings and spiral waveguides, it is still challenging to realize optical buffers with long storage time and low loss. Photonic integrated circuits with small size are of interest for implementing optical buffers. In general, three materials systems are employed to implement integrated optical buffers, silicon, silicon nitride and indium phosphide. However, it is hard to implement optical buffers with a storage time over tens of nanoseconds due to the intrinsic high loss of these materials.

Recently, a low-loss integrated optical buffer based on silica that can offer a long storage time has been proposed and demonstrated by a team led by Dr. Ming Li from the Institute of Semiconductors, CAS. They built an integrated optical buffer based on silica. By connecting four spiral waveguide delay lines with five thermo-optic switches, tunable time delay was achieved. By optimizing the fabrication process and introducing offsets between straight and bending waveguides, the transmission loss of the silica buffer was reduced to 1.08 dB/m. Given that the group refractive index of silica is around 1.46 and the total length of the delay lines in their fabricated chip is about 20 m, the maximum storage time is 100 ns. Moreover, a 10-ns step was accomplished in their experiment by the various combinations of four stair-like delay lines: 10, 20, 30, 40 ns. Their work may provide a valuable reference for fabricating more advanced optical buffers and might have significant impact on signals processing in optical communications networks and microwave photonics systems.

Jianping Yao (University of Ottawa, Ottawa, Canada)
doi: 10.1088/1674-4926/40/5/050205