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Influence of growth conditions of oxide on electrical properties of AlGaN/GaN metal–insulator–semiconductor transistors

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Abstract: AlGaN/GaN metal–insulator–semiconductor high-electron-mobility transistors (MIS-HEMTs) on a silicon substrate were fabricated with silicon oxide as a gate dielectric by sputtering deposition and electron-beam (EB) evaporation. It was found that the oxide deposition method and conditions have great influences on the electrical properties of HEMTs. The low sputtering temperature or oxygen introduction at higher temperature results in a positive equivalent charge density at the oxide/AlGaN interface (N_{equ}), which induces a negative shift of threshold voltage and an increase in both sheet electron density (n_s) and drain current density (I_D). Contrarily, EB deposition makes a negative N_{equ}, resulting in reduced n_s and I_D. Besides, the maximum transconductance ($g_{m\text{-}max}$) decreases and the off-state gate current density ($I_{G\text{-}off}$) increases for oxides at lower sputtering temperature compared with that at higher temperature, possibly due to a more serious sputter-induced damage and much larger N_{equ} at lower sputtering temperature. At high sputtering temperature, $I_{G\text{-}off}$ decreases by two orders of magnitude compared to that without oxygen, which indicates that oxygen introduction and partial pressure depression of argon decreases the sputter-induced damage significantly. $I_{G\text{-}off}$ for EB-evaporated samples is lower by orders of magnitude than that of sputtered ones, possibly attributed to the lower damage of EB evaporation to the barrier layer surface.

Key words: AlGaN/GaN MIS-HEMTs; sputtering deposition; electron-beam evaporation; silicon oxide; electrical properties

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1. Introduction

GaN and AlN alloys are good choices for the fabrication of optoelectronics and electronic devices, such as light-emitting diodes, ultraviolet detectors, and high-power and high-frequency electronic devices, due to their excellent material properties[1–9]. These applications lead to a huge market, which provides a strong impetus for research. By using superior material features, such as a large bandgap, high breakdown field, high electron mobility and large two-dimensional electron gas (2DEG) density, the AlGaN/GaN based high-electron-mobility transistor (HEMT) has been identified to be the most promising candidate for high-power and high-frequency applications. However, the facilitation of sufficient positive gate voltage swings and suppression of leakage current for the HEMTs are tasks still to be solved. Metal–insulator–semiconductor (MIS) structure is an attractive alternative to the conventional Schottky gate contact to solve the problems. Although numerous insulators, such as SiO_2, Al_2O_3, HfO_2, MgO, Ta_2O_5, Sc_2O_3, ZrO_2, AlN and Si_3N_4 have been studied as the gate dielectric for GaN-based HEMTs[10–24], silicon oxide remains popular due to its large band gap (~9 eV), large conduction band discontinuity (~3 eV) and high critical breakdown electric field (~ 15 MV/cm) in comparison with other gate insulators typically used[23, 24]. In addition, it is already consolidated in the Si-devices industry, and it is also applied to depress the dark current of GaN-based ultraviolet detectors[25]. A different quality of insulator and interface state of insulator/semiconductor could be obtained by different deposition techniques and deposition conditions, which strongly impact the electrical performance of the devices[22, 26]. Sputtering deposition and electron beam (EB) evaporation are nowadays well established as two important techniques for the preparation of thin silicon oxide films. Their advantages include lower deposition temperature and equipment cost, and secure working atmosphere without using the toxic metal–organic precursors and ammonia[27]. In addition, sputtering deposition can form thin films with good uniformity and good adhesion to the substrate surface without involving the complications of the target heating process[28]. In this work, we fabricated the MIS-HEMTs using sputtered and electron-beam evaporated silicon oxide as gate dielectric, and investigated the performance of devices under different deposition techniques and sputtering conditions.

2. Experimental

The HEMT structure consisted of unintentionally doped-$Al_{0.26}Ga_{0.74}N$ (25 nm)/unintentionally doped-GaN (1 μm)/super lattices (GaN/AlGaN)/buffer layer (AlGaN/AlN) grown by metal organic chemical vapor deposition (MOCVD) on a 4-inch silicon substrate. The fabrication of HEMTs and two-terminal circular diodes for capacitance–voltage (*C*–*V*) measurement started with device isolation by BCl_3 plasma reactive ion etching. Then silicon oxide was deposited by different deposition techniques and deposition conditions. After etching the silicon oxide with buffered HF solution, the ohmic contact was formed using Ti/Al/Ni/Au (15/72/12/40 nm) followed by rapid

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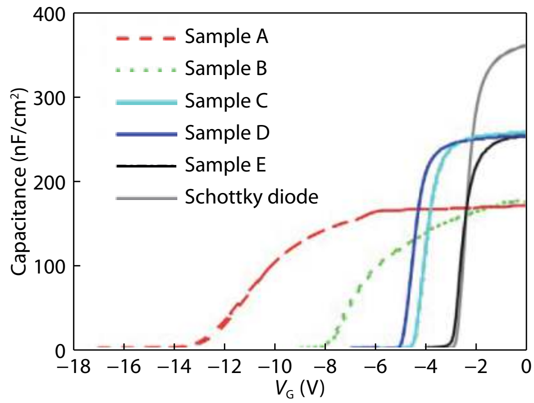

Fig. 1. (Color online) *C–V* characteristics at 1 MHz for all the diodes.

thermal annealing at 850 °C for 30 s in a N_2 atmosphere. The Ni/Ti/Au (40/20/60 nm) was deposited on silicon oxide as a gate electrode. Several samples have been fabricated in terms of oxide deposition. Oxides for samples A and B were deposited with similar thickness by RF sputter at room temperature (RT) and 150 °C, respectively, under Ar atmosphere. Oxides for samples C and D were deposited by RF sputter at 150 °C under Ar and Ar/O_2 atmosphere (Ar : O_2 = 1 : 1), respectively. The difference of sample B and sample C was the oxide thickness. Oxide for sample E was deposited by electron-beam evaporation at 150 °C under oxygen atmosphere. Oxides for samples C, D and E have a similar thickness. The target for sputter is silicon oxide. The gate length and width for HEMT devices is 1.5 and 15 μm, respectively. In order to calculate the carrier density and oxide thickness, Schottky diodes without silicon oxide for capacitance–voltage (*C–V*) measurement were also fabricated. The current–voltage (*I–V*) characteristics were measured on an Agilent 4156c semiconductor parameter analyzer. Capacitance–voltage (*C–V*) measurement was carried out using an HP4845 LCR meter.

3. Results and discussion

C–V characteristics for all the diodes at 1 MHz are shown in Fig. 1. The thicknesses of silicon oxide films for samples A to E were estimated to be around 11, 10, 3.8, 4.0 and 4.0 nm, respectively, based on the formula,

$$d_{\rm ins} = \varepsilon_{\rm ins}\varepsilon_{\rm o}(1/C_{\rm MIS} - 1/C_{\rm AlGaN}), \tag{1}$$

where $d_{\rm ins}$ is the thickness of silicon oxide, $\varepsilon_{\rm ins}$ is the relative dielectric permittivity of silicon oxide taken as 3.9, $\varepsilon_{\rm o}$ is the dielectric permittivity of a vacuum, and $C_{\rm MIS}$ and $C_{\rm AlGaN}$ are the unit-area capacitances of the MIS-diodes and the Schottky diode at 0 V, respectively. From *C–V* curves, the sheet carrier density ($n_{\rm s}$) could be estimated according to the expression,

$$n_{\rm s} = \int_{V_{\rm th}}^{0} C{\rm d}V, \tag{2}$$

where $V_{\rm th}$ is defined as the gate voltage at which the GaN buffer is depleted in the *C–V* curve. The $n_{\rm s}$ were calculated to be 1.2×10^{13}, 6.4×10^{12}, 6.3×10^{12}, 7.0×10^{12}, 3.6×10^{12} and 5.1×10^{12} cm^{-2} for samples A to E and Schottky diode, respectively. Considering the very low electron concentration in the GaN buffer compared with the electron density of 2DEG in channel and neglecting the interface states due to high-frequency (HF) capacitance, $n_{\rm s}$ could be regarded as the electron density of 2DEG. It should be noticed that $n_{\rm s}$ in sample A was more than twice of that in the Schottky diode, while sample E reduced 30% compared with the Schottky diode. According to Poisson's equation and the Schrödinger equation, $n_{\rm s}$ for 2DEG can be expressed as

$$n_{\rm s}^{\rm Schottky} = \frac{\sigma_{\rm p}}{q} - \frac{C_{\rm AlGaN}\left(\phi_{\rm b} - \frac{\Delta E_{\rm c}}{q} + \frac{\Delta E_{\rm F}^{\rm Schottky}}{q} - V_{\rm G}\right)}{q}, \tag{3}$$

for Schottky HEMTs, and

$$n_{\rm s}^{\rm MIS} = \frac{\sigma_{\rm p}}{q} - C_{\rm MIS}\frac{\phi_{\rm b}' - \frac{\Delta E_{\rm c}^{\rm ins}}{q} - \frac{\Delta E_{\rm c}}{q} + \frac{\Delta E_{\rm F}^{\rm MIS}}{q} - V_{\rm G}}{q} + C_{\rm MIS}\frac{qN_{\rm equ}}{C_{\rm ins}}, \tag{4}$$

for MIS-diode, where $\phi_{\rm b}$ and $\phi_{\rm b}'$ are the barrier height for Ni/$Al_{0.26}Ga_{0.74}N$ and Ni/SiO_2, taken as 0.9 V (obtained from the current-voltage curve of the Schottky diode) and 3.6 V[29], respectively. $\Delta E_{\rm c}^{\rm ins}$ and $\Delta E_{\rm C}$ are conduction band discontinuity taken as 3.1 and 0.3 eV for SiO_2/$Al_{0.26}$GaN and $Al_{0.26}$GaN/GaN, respectively. $C_{\rm MIS}$, $C_{\rm ins}$ and $C_{\rm AlGaN}$ are capacitance per unit of MIS-diode, oxide and Schottky diode, respectively. $\sigma_{\rm p}$ is the total polarization sheet charge density. $V_{\rm G}$ is applied to gate bias. $qN_{\rm equ}$ is defined as the equivalent charge density at the oxide/AlGaN interface, which includes the oxide/barrier interface trap ($N_{\rm it}$) and interfical fixed charge at the oxide/AlGaN interface ($Q_{\rm if}$) (including the polarization charge at the surface AlGaN barrier, the ionized donor density at AlGaN barrier surface and the fixed charge density of the silicon oxide at the oxide/barrier interface), as well as the equivalent charge density at the AlGaN/GaN interface generated by the charge density in oxide bulk ($Q_{\rm bulk}$). $\Delta E_{\rm F}^{\rm Schottky}$ and $\Delta E_{\rm F}^{\rm MIS}$ is the Fermi level with respect to the GaN conduction-band-edge energy at the AlGaN/GaN interface for Schottky HEMT and MIS-HEMT, respectively, and $\Delta E_{\rm F}$ is expressed as[30]

$$\Delta E_{\rm F} = E_1 + \frac{\pi\hbar^2}{m^*}n_{\rm s}, \tag{5}$$

$$E_1 = \left(\frac{9\pi\hbar q^2}{8\sqrt{8m^*}\varepsilon_0\varepsilon}n_{\rm s}\right)^{2/3}, \tag{6}$$

where m^* is the electron effective mass of GaN and taken as $0.22m_0$ (m_0 is the free electron mass). Therefore,

$$n_{\rm s}^{\rm MIS} = n_{\rm s}^{\rm Schottky} + \frac{C_{\rm AlGaN}\left(\phi_{\rm b} - \frac{\Delta E_{\rm c}}{q} + \frac{\Delta E_{\rm F}^{\rm Schottky}}{q} - V_{\rm G}\right)}{q} - C_{\rm MIS}\frac{\phi_{\rm b}' - \frac{\Delta E_{\rm c}^{\rm ins}}{q} - \frac{\Delta E_{c}}{q} + \frac{\Delta E_{\rm F}^{\rm MIS}}{q} - V_{\rm G}}{q} + C_{\rm MIS}\frac{qN_{\rm equ}}{C_{\rm ins}}. \tag{7}$$

Considering $n_{\rm s}^{\rm Schottky}$ of 5.1×10^{12} cm^{-2}, $n_{\rm s}^{\rm MIS}$ at gate bias 0 V could be estimated as 6.5×10^{12} cm^{-2} for samples A and B

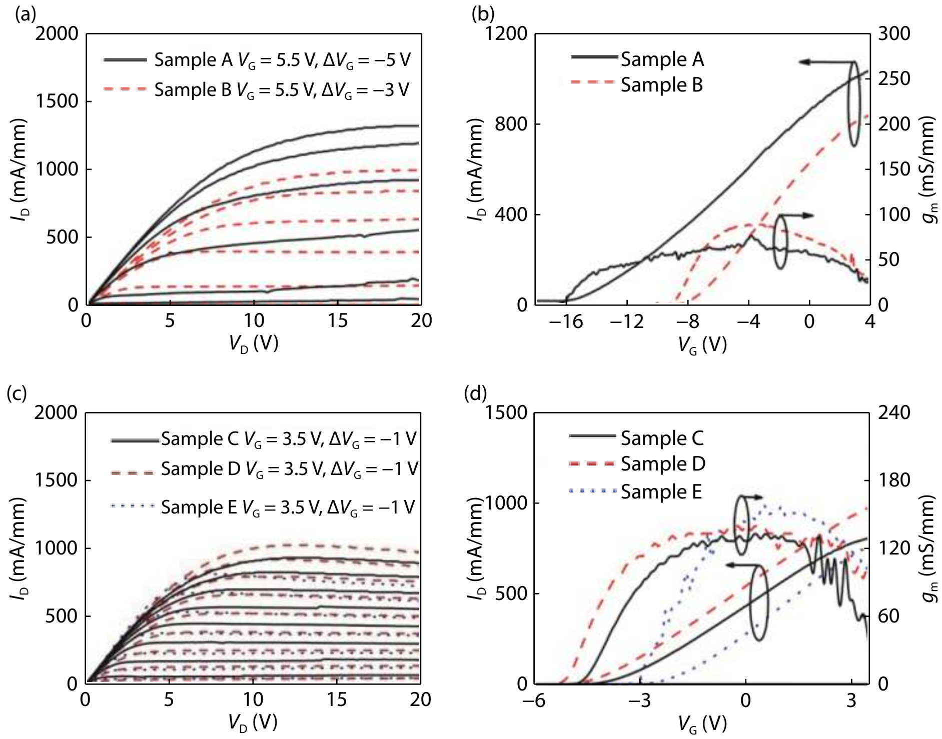

Fig. 2. (Color online) (a) The output characteristics and (b) the transfer characteristics for samples A and B. (c) The output characteristics and (d) the transfer characteristics for samples C, D and E.

and 6.2×10^{12} cm^{-2} for samples C to E, assuming N_{equ} is zero in MIS-diodes. Compared with the calculated value without N_{equ}, n_s obtained from C–V curves for sample A almost doubled and for sample D rised slightly, while for sample E it decreased to nearly half. This indicated that N_{equ} for sample A and D was positive, which increased the n_s. N_{equ} for EB-oxide (sample E) was negative, which reduced n_s. For samples B and C, the experimental value was very close to the calculated one, indicating that N_{equ} could be negligible. According to Eq. (7), N_{equ} could be estimated as 1.0×10^{13} and 2.8×10^{12} cm^{-2} for samples A and D, respectively, with positive charge and 8.8×10^{12} cm^{-2} for sample E with negative charge. That is, for sputtered samples, lower temperature or high temperature with oxygen introduction will resulte in positive N_{equ}. If N_{it} could be negeligible due to hf capacitance, Q_{if} and/or Q_{bulk} should be the main contribution to N_{equ}. Hence, the contribution of Q_{if} and Q_{bulk} could be ignored for the case of samples B and C due to negligible N_{equ} estimated above. Threshold voltage (V_{th}) could also be extracted for samples A to E and the Schottky diode from C–V measurements as −14.5, −7.8, −4.5, −4.9, −3.0 and −2.8 V, respectively, defined as the gate voltage at which the GaN buffer is depleted. Obviously, due to its larger positive charged N_{equ}, sample A showed a negative shift of V_{th} compared with sample B though their oxide thicknesses were similar. For the samples with similar oxide thickness, samples D and E showed negative and positive shift of V_{th} relative to sample C, due to the positive and negative charged N_{equ} in comparison with sample C, respectively.

Fig. 2 shows the drain current–drain voltage (I_D–V_D) curves and transfer characteristics for all the HEMTs. From Figs. 2(a) and 2(b), the drain current density for sample A was larger than that of sample B at the same gate voltage, which was due to larger n_s for sample A. The maximum current density ($I_{D\text{-max}}$) for samples A and B were 1323 and 1008 mA/mm, respectively, at the maximum applied gate voltage of 5.5 V. The maximum transconductance ($g_{m\text{-max}}$) for sample A and B were 77 and 90 mS/mm, respectively. The lower $g_{m\text{-max}}$ of sample A indicated that the mobility is lower compared with that of sample B, which is possibly because of electron scattering enhancement for sample A due to the highest electron density (exceeded 10^{13} cm^{-2} in 2DEG), the remote coulombic scattering enhancement by much more positive interfacial charge and higher sputtered-induced damage in the sputtering process for sample A[31]. The output characteristics and transfer characteristics for samples C, D and E were shown in Figs. 2(c) and 2(d). The I_D for sample C was smaller than that of sample D, but larger than that of sample E at the same gate voltage, which was due to the N_{equ}-induced similar change trends of n_s. For example, the $I_{D\text{-max}}$ for samples D, C and E were 1027, 933 and 812 mA/mm at the applied gate voltage of 3.5 V, respectively. The $g_{m\text{-max}}$ for samples C, D and E were 132, 147 and 160 mS/mm, respectively. The highest $g_{m\text{-max}}$ of sample E indicated that the mobility is highest among the three samples, which is possibly because, for sample E, the low electron density and no sputtering-induced surface damage[32] suppress the electron scattering.

Figs. 3(a) and 3(b) showed the drain current–gate voltage (I_D–V_G) curves and three-terminal gate current density on a semi-logarithmic scale. It can be seen that the off-state gate current density ($I_{G\text{-off}}$) is larger than the off-state drain current density ($I_{D\text{-off}}$), which indicates $I_{D\text{-off}}$ is a branch of $I_{G\text{-off}}$ for all HEMT devices within the gate voltage sweeping range. Considering the difference of $I_{G\text{-off}}$ between the devices is several orders of magnitude and much larger than the difference of $I_{D\text{-max}}$, the $I_{D\text{-on}}/I_{D\text{-off}}$ ratio mainly depends on $I_{G\text{-off}}$. We compared the $I_{G\text{-off}}$ value taken at the turn-around point in a logarithmic I_D–V_G

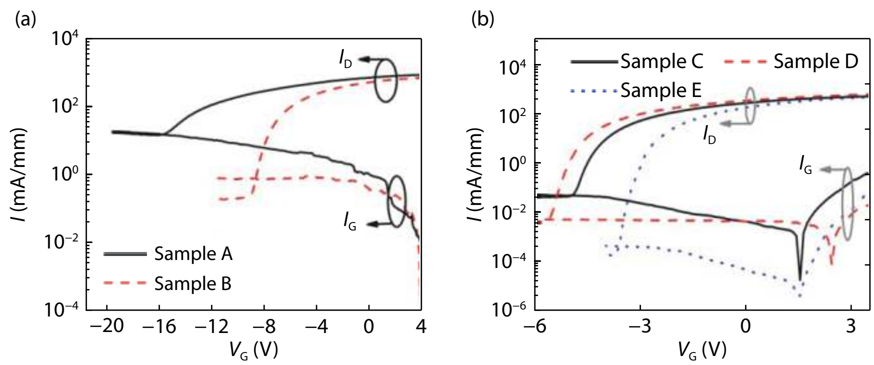

Fig. 3. (Color online) The I_D–V_G curves and three-terminal gate current density (I_G) in semi-logarithmic scale for (a) samples A and B and (b) samples C, D and E.

curve. $I_{G\text{-off}}$ on the order of 10 mA/mm for sample A is more than one order of magnitude larger than that of sample B (10^{-1} mA/mm), which is possibly due to the higher sputter-induced shallow donor-like N vacancies[32–34] and much more N_{equ} for oxide deposited at lower substrate temperature. $I_{G\text{-off}}$ for sample C is in the order of 10^{-2} mA/mm, which is also one order of magnitude larger than that for sample D (10^{-3} mA/mm). This inferred that the reduced Ar partial pressure and oxygen introduction could lead to lower sputter-induced N vacancies, which may be ascribed to the energy bombarded on the surface of the barrier layer being reduced because of the smaller atomic mass of O than Ar. In all the samples with sputtered oxides, the $I_{G\text{-off}}$ is orders of magnitude larger than that of sample E with EB-evaporated oxide (10^{-4} mA/mm), which suggested that the surface damage of the barrier layer by EB deposition was low and the carrier tunneling was suppressed by oxide.

4. Conclusions

In this paper, AlGaN/GaN based MIS-HEMTs were fabricated using EB-evaporated and sputtered silicon oxide as dielectric. It was found that the electrical properties were influenced by oxide deposition techniques and deposit condition. The high n_s and high drain current density as well as high gate leakage could be achieved using silicon oxide as the gate dielectric by RF-sputtering deposition at room temperature, while low n_s, positive shift of V_{th} and low gate leakage could be obtained using EB-evaporated oxide as the gate dielectric. That is, there is a tradeoff among the deposition methods and deposition conditions for the HEMT devices to achieve appropriate electrical properities.

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