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Second generation fully differential current conveyor based analog circuits

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Abstract: In this paper, we present a new voltage-mode biquad filter that uses a six-terminal CMOS fully differential current conveyor (FDCCII). The FDCCII with only 23 transistors in its structure and operating at ± 1.5 V, is based on a class AB fully differential buffer. The proposed filter has the facility to tune gain, ω_o and Q. A circuit division circuit (CDC) is employed to digitally control the FDCCII block. This digitally controlled FDCCII is used to realize a new reconfigurable fully-differential integrator and differentiator. We performed SPICE simulations to determine the performance of all circuits using CMOS 0.25 μm technology.

Key words: current conveyors; fully differential; digitally controlled; integrator; differentiator

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1. Introduction

Fully differential (FD)[1–4] circuits have become the most widely-used configurations in the design of electronic circuits and systems because they provide better elimination of clock feed through, charge rejection errors and power supply noises when compared to its single-ended counterparts[5]. The second-generation current conveyor (CCII) is a highly versatile single ended current-mode building block; however, high-performance analog integrated circuits today incorporate fully differential signal paths. In 2005, El-Adway *et al.* introduced a fully-differential current conveyor (FDCCII), which possess a larger output dynamic range, higher design flexibility, wide bandwidth, high slew rate, low power consumption and reduced harmonic distortion when compared to CCII. Consequently, analog designers were significantly boosted to realize FDCCII based circuits. Despite the known merits, comparatively little work has been accomplished using FDCCII as far back as 2005. The main reasons for refraining from their utilization are discussed in the following.

The FDCCII structures that were reported in the literature employed large supply voltages, as high as 5 V[6]. However, in 2014, Kumngern *et al.* introduced a low voltage structure[7] using the bulk driven technique[8]. The operating supply was reduced to 0.5 V. While the semiconductor industry races toward lower-technology nodes still in FDCC structures transistor technology, ranging from 0.35 μm to as large as 1.2 μm[5–6, 9]. This was scaled down to 0.18 μm as reported in Ref. [7], but this challenge remains. Since the FDCCII block comes with the inherent advantage of realizing multifunctional filters using a single block[4, 6, 10], this leads to an issue in the non-independent tuning of ω_o and Q. In these cases, the same parameter or code-word affects the Q factor, ω_o and sometimes gain concurrently. The reconfigurable feature of an analog cell is a prominent characteristic in several applications. Most of the existing FD circuits[11–13] utilize either op-amps, DXCCII, DVCCII, DDCC or some other variant. If a FDCCII block has been used to design an application, then only analog tuning has been discussed. Digital control of FDCCII block has not been explored, which leaves open the possibility to realize more digitally controlled FDCCII-based ASP applications.

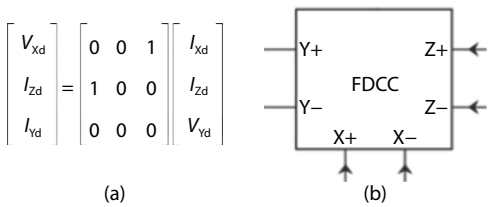
The motivation of this treatise is to present the facility of independent analog and digital tuning of FDCCII-based analog signal processing applications related to theser two concerns. The rest of this paper is structured as follows. The first section presents a fully differential second order low-pass/band-pass filter using a six terminal CMOS FDCCII. The FDCCII is then reconfigured through digital programmability by introducing a current division circuit. Finally, a new digitally controlled FDCCII integrator and differentiator are also presented in the last section.

2. CMOS FDCCII

FDCCII (see the block diagram of Fig. 1(b)) has two differential X, Y and Z terminals. The fully differential buffer forces V_{Xd} to follow V_{Yd}. The FDCCII structure (see Fig. 2) has only 23 transistors unlike the available fully differential structures with 39 transistors in Refs. [9, 14]. The FD buffer consists of two matched differential pair (M_{10}, M_{13}) & (M_{14}, M_{17}); matched biasing current source transistors (M_{15}, M_{16}) & (M_{11}, M_{12}); and class AB output stage (M_6–M_9) & (M_{18}–M_{21}). (M_1–M_3) forms the biasing of output stage and the input is applied at high impedance terminals of NMOS (M_{13}, M_{14}). The DC voltage characteristics of the differential X terminal and the transfer characterist-

$$\begin{bmatrix} V_{Xd} \\ I_{Zd} \\ I_{Yd} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{Xd} \\ I_{Zd} \\ V_{Yd} \end{bmatrix}$$

(a)



(b)

Fig. 1. (a) Matrix representation of FDCCII. (b) Symbol for FDCCII.

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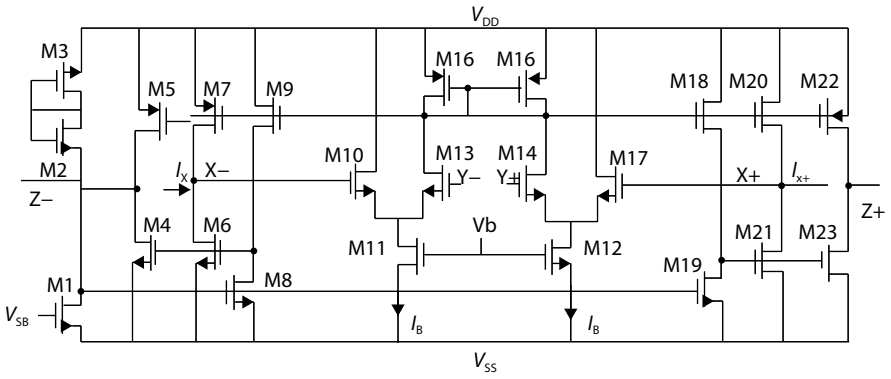

Fig. 2. CMOS FDCCII implementation.

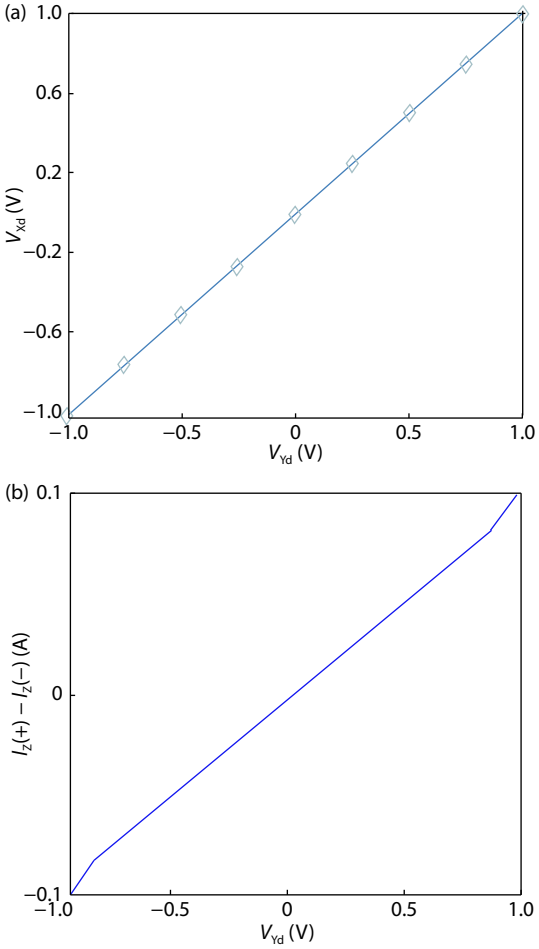

Fig. 3. (Color online) (a) DC voltage characteristics of differential X terminal. (b) DC current response of differential Z terminal.

ics of the differential Z terminal of FDCCII are depicted by Figs. 3(a) and 3(b) respectively. Voltage and current following actions of FDCCII, as shown by the terminal equations of Fig. 1(a), exhibit nearly rail-to-rail transfer between input and output terminals. The DC current range extends from −100 to 100 mA and the DC voltage range is −1 to 1 V. The characteristic values for the FD-CCII are given in Table 1. Transistor aspect ratios are shown in Table 2.

3. Proposed biquad realization and its comparison

The Sallen-Key filter,which is particularly valued for its simplicity, is a very popular active filter. It can be used to create 2nd order filter stages that can be cascaded together to form larger order filters. A Sallen-Key LP configuration has been presented in Ref. [15][#1] using an op-amp[*1] and DDA[*2] in Ref. [16][#1]. The authors in Ref. [9][#1] have implemented Sallen Key BP response using FBDDA[*1]. Realization of another Sallen Key BP filter using DDCCII[*1] is proposed in Ref. [17][#]. Sallen Key filter (LP, BP) response using (AD844) plus type CCII[*6] is presented in Ref. [13][#2]. However, these realizations are either non-CC based or non-fully differential. In our architecture[#2], we have realized a voltage mode second order filter using a six terminal CMOS Fully Differential CC, FDCCII[*3]. The proposed realisation is shown in Fig. 4. V_{o1} and V_{o2} are low-pass and band-pass responses respectively. Routine analysis yields following output functions:

$$\frac{V_{02}}{V_{in}} = -\frac{\dfrac{G_1 s}{C_1}}{s^2 + s\left(\dfrac{G_2}{C_1}\right) + \dfrac{G_4 G_3}{C_1 C_2}},$$

$$\frac{V_{01}}{V_{in}} = -\frac{G_1 G_3 / C_1 C_2}{s^2 + s\left(\dfrac{G_2}{C_1}\right) + \dfrac{G_4 G_3}{C_1 C_2}},$$

$$\omega_o = \sqrt{G_4 G_3 / C_1 C_2},$$

$$\omega_o / Q = \frac{G_2}{C_1},$$

$$Q = \frac{1}{G_2}\sqrt{C_1 G_4 G_3 / C_2}.$$

As evident from these equations, analog tuning of the gain can be achieved by using G_1, ω_o by setting C_1/C_2 and Q by using G_2. The filter gain can be expressed as: $H_{LP} = -G_1/G_4$,

Table 1. Main features of FDCCII.

V_{DD}, V_{SS}, V_{SB}, V_b	1.5, −1.5, −1.25, −0.787 V
No. of transistors	23
DC voltage range	−1 to 1 V
DC current range	−100 to 100 mA
−3 dB bandwidth: V_{Zd}/V_{Yd}	82 MHz
FOM$_1$ =(V_{inmax}/V_{DD}) × 100	66

* refers to number of active blocks.
\# refers to number of output available.

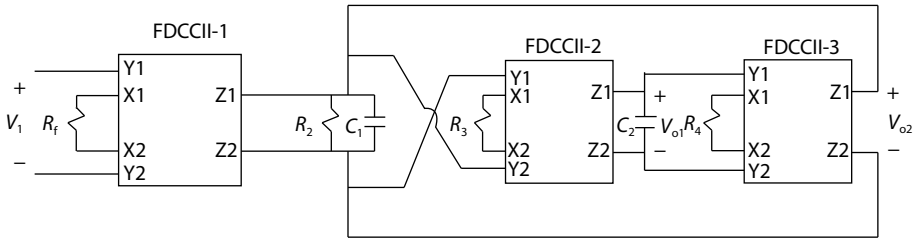

Fig. 4. Second order Filter realized using CMOS FDCCII (LP/BP response).

Table 2. Aspect ratios of MOS transistors.

Transistor for FDCCII	W/L (μm/μm)
M1, M8, M9, M18, M19	2/1
M3, M5, M7, M20, M22	200/2
M2, M4, M6, M21, M23	150/2
M15, M16	100/2
M10, M13, M14, M17	80/1
M11, M12	80/2
Transistor for CDN	W/L (μm/μm)
All transistors	1/0.35

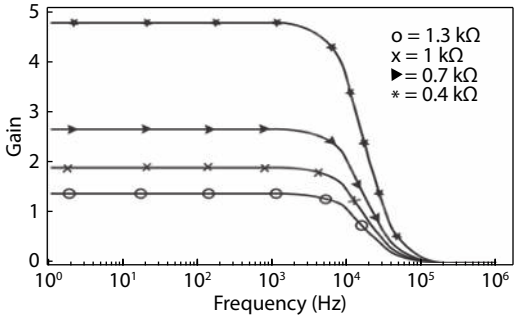

Fig. 5. LPF gain tuning (f_o = 13 kHz) through R_1.

$H_{BP} = -G_1G_2$.

3.1. Sensitivity performance

The voltage gain between differential X and Y terminals, here, is not crucial because unity negative feedback has been employed in the realization. Considering the deviation of current gain involving differential X and Z terminals and taking the non-ideality into account, namely, $I_{zdi} = \alpha_i I_{xdi}$, where i = 1, 2, 3, $\alpha = 1-\varepsilon$ and ε ($|\varepsilon| \ll 1$) is the FDCCII current tracking error, the output LP and BP functions of the proposed filter can be expressed as:

$$\frac{V_{02}}{V_{in}} = -\frac{\dfrac{\alpha_1 G_1 s}{C_1}}{s^2 + s\left(\dfrac{G_2}{C_1}\right) + \dfrac{\alpha_3\alpha_2 G_4 G_3}{C_1 C_2}},$$

$$\frac{V_{01}}{V_{in}} = -\frac{\alpha_1\alpha_2 G_1 G_3/C_1 C_2}{s^2 + s\left(\dfrac{G_2}{C_1}\right) + \dfrac{\alpha_3\alpha_2 G_4 G_3}{C_1 C_2}},$$

$$\omega_o = \sqrt{\alpha_3\alpha_2 G_4 G_3/C_1 C_2},$$

$$\omega_o/Q = \frac{G_2}{C_1},$$

$$Q = \frac{1}{G_2}\sqrt{\alpha_3\alpha_2 C_1 G_4 G_3/C_2}.$$

Table 3. Summarized performance of proposed filter.

Characteristics	Proposed realization
Supply used	± 1.5 V
Technology	0.25 μm
Fully differential	Yes
Active element	FDCCII
No. of active elements	3
Enjoys independent tuning	Yes
Tuning (analog/digital)	Analog
Component values	R_1 = 1.3 kΩ; R_2 = 2.5 kΩ (for LPF) and 10 kΩ (for BPF); R_3 = 3 kΩ; R_4 = 2 kΩ; C_1 = 5 nF; C_2 = 5 nF

The sensitivities of different filter specifications are summarized below.

$$S^{\omega_o}_{\alpha_2,\alpha_3,G_4,G_3} = -S^{\omega_o}_{C_2,C_1} = \frac{1}{2},$$

$$S^{\omega o}_{\alpha_2,\alpha_3,G_4,G_3,C_1} = -S^{Q}C_1 = \frac{1}{2},$$

$$S^{Q}G_2 = -1.$$

The proposed circuit enjoys attractive sensitivity measure. All active and passive sensitivity figures are within reasonable limits. The filter has been realized using three FDCCII blocks, using only four resistors and two capacitors. This component count is less than most of the available Sallen-Key realizations and offers the same number of output functions. It can also independently tune Q and orthogonal control of ω_o & Q.

3.2. Design and verification

SPICE simulations were carried out to verify the potential of proposed second-order filter. When R_1 takes values from 1.3 to 0.4 kΩ decreasing with a step size of 0.3 kΩ, gain of the LP & BP filter is found to be increasing. As R_1 decreases, value of G_1 increases because the two are reciprocal of each other. R_1 takes values equal to {1.3, 1, 0.7, and 0.4 kΩ} for plotting low-pass and band-pass response with variable gain, as given in Figs. 5 and 6. f_o has been fixed at 13 Hz and Q = 1.02 for LPF & Q = 4.08 for BPF. This variation of filter gain with resistor R_1 is in agreement with the transfer functions, V_{01} and V_{02}, as calculated at the beginning of Section 3. Tuning of Q-factor has been achieved by varying R_2 as {8, 12, and 16 kΩ}. Here, the BP filter's gain (see Fig. 7) can be seen to vary with R_2, which again verifies the theoretical calculations. Pole-ωo tuning can be achieved by programming C_1, C_2 using capacitor array[9, 14]. However, the capacitor array requires more chip area but they reserve high linearity of the filter and also allow direct interfacing with digital signal processing section of receiver[9]. The circuit employs floating capacitors which are now standard and implemented with advanced IC design techniques. These new

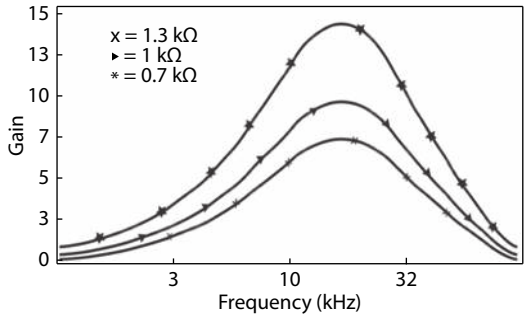

Fig. 6. BPF gain tuning (f_o = 13 kHz & Q = 4.08) through R_1.

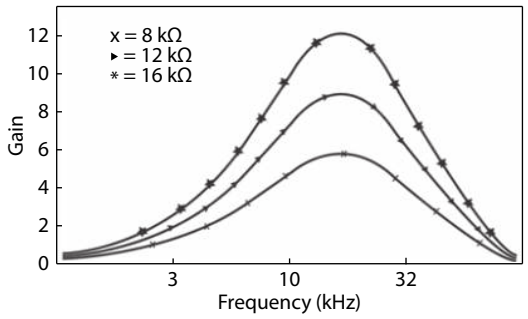

Fig. 7. At constant central frequency of 13 kHz, Q values varying with R_2 are 3.3, 4.9 & 6.5 respectively.

Table 4. Comparative study of previously reported differential second order filters.

Reference	Adway 2000[5]	Alzaher 2003[9]	Chang 2003[6]	Shahrani 2004[13]	Mahmoud 2004[20]	Mahmoud 2005[10]	Mahmoud 2007[14]	Karac 2008[19]	This work
Technology node (μm)	1.2	1.2	1.2	–	0.35	0.5	0.35	0.35	0.25
Active element used	FDCCII	FBCCII	FDCCII	CCII/AD844	FDCFOA	FDCCII	FDCCII	FDCCII	FDCCII
Number of active elements used	3	1	1	6	1	6	1	2	3
Supply rails used (V)	± 1.5	± 2.7	± 5	–	± 1.5	± 1.5	± 1.5	± 1.25	± 1.5
Functions realized	LP BP	BP	LP BP AP BR	LP BP	LP	LP BP AP	BP	LP BP AP	LP BP
Tuning feature	N	Y	N	Y	N	Y	Y	N	Y
Fully differential	Y	Y	Y	Y	Y	Y	Y	Y	Y

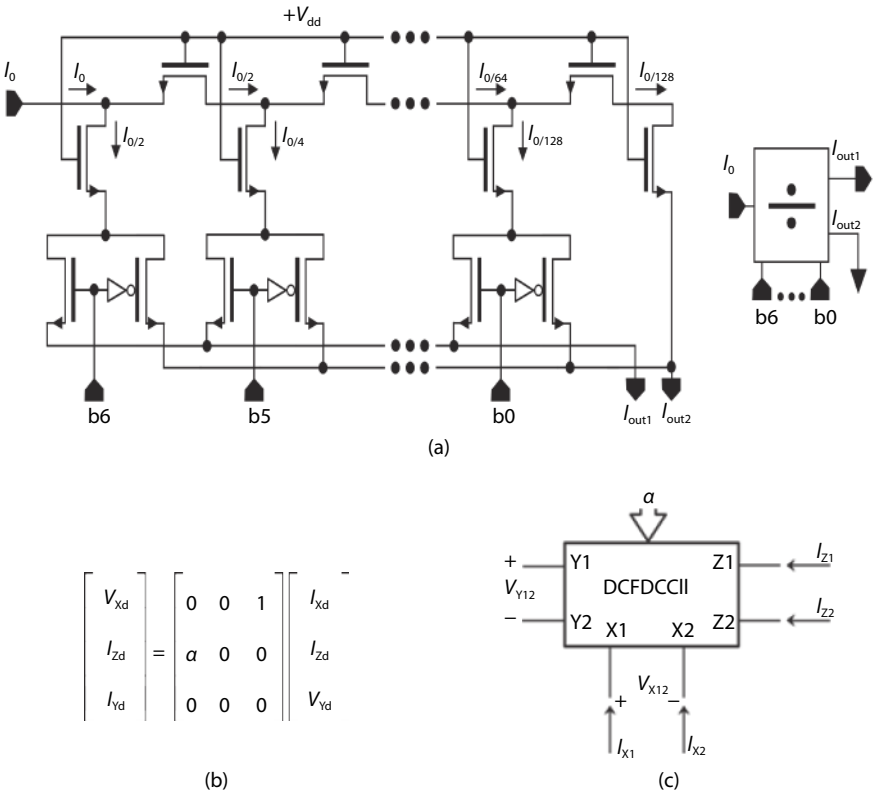

Fig. 8. (a) Current division circuit (CDC). (b) Matrix representation of DCFDCCII. (c) Symbol of DCFDCCII.

IC technologies realize floating capacitors as a double poly (poly1-poly2) capacitor[18]. A basic and a comparative detail of the performance of proposed realization have been summarized in Tables 3 and 4 respectively.

4. Current division circuit

Fig. 8(a) shows a 6-bit M-2M ladder classical circuit which is employed at Z+ and Z- terminals of FDCCCII. Current division circuit divides input current into two branches depending on the value of a set of programmed bits. In our case, I_{out1} is the ladder output that depends on the value of the α and I_{out2} is grounded. N is the digital codeword. The input current is multiplied by a factor alpha, which depends on value of the first 6-bits according to:

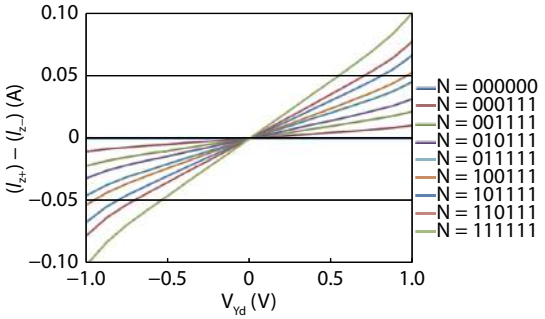

Fig. 9. (Color online) DC response of Z terminals current of DCFDCCII.

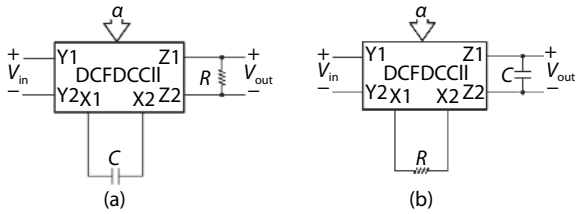

Fig. 10. DCFDCCII based programmable integrator and differentiator.

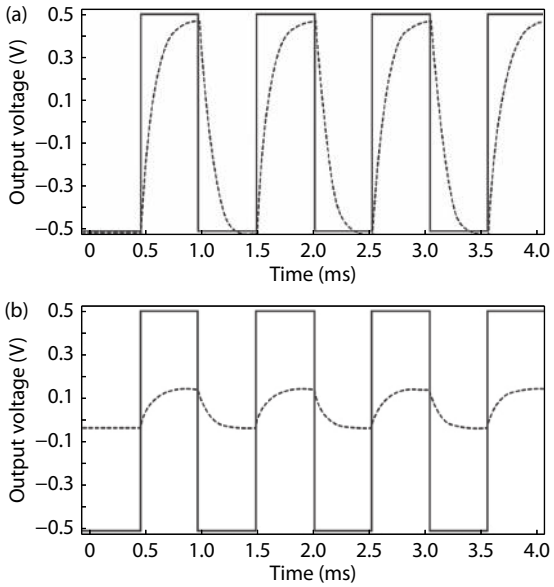

Fig. 11. Observed output for codeword (a) 111111, (b) 010101.

$$I_{\text{out1}} = \boldsymbol{a} I_{\text{in}} \wedge \boldsymbol{a} = \frac{1}{2^n}\left(\sum_{j=0}^{n-1} b_j 2^j\right) \text{ with } n = 6$$

$$\text{where } N = \sum_{j=0}^{n-1} b_j 2^j.$$

Current transfer characteristics of FD-CCII block with digital control is shown in Fig. 9. Both the integrators and differentiators are prominent blocks that find applications in analog-to-digital convertors (ADCs), wave shaping circuits and continuous-time filter structures. They are considered to be very important units in the design of analog integrated and mixed-signal circuits. The output signal in an integrator is nothing but the time integral of the incoming signal. As for the differentiator, its output is directly proportional to the rate of change of the input. Earlier, most of the RC integrator and differentiator circuits were designed using operational amplifier. The major drawback of using these op-amp based circuits is that they don't provide a spacious bandwidth and wider dynamic range. Subsequently, a few circuits have been proposed employing different current voltage-mode devices, such as OTA, CC, CCTA, etc. In this paper digitally programmable VM integrator and differentiator are shown in Fig. 10. These circuits consist of a single DCFDCCII, capacitor and resistor. They not only have the advantages of being differential but they also have versatile programmability. A routine analysis of the circuits yields the following outputs:

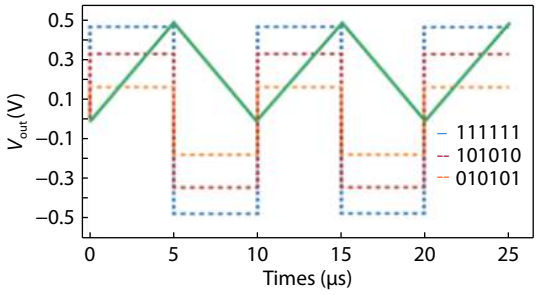

Fig. 12. (Color online) Differentiator input & observed output for code words.

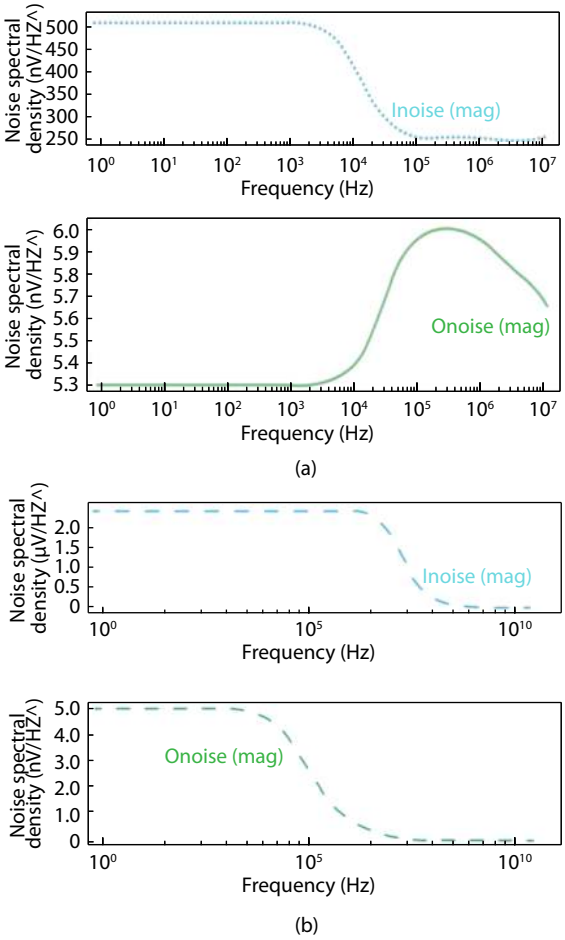

Fig. 13. (Color online) Input (inoise) and output (onoise) referred noise spectral density for (a) integrator, (b) differentiator.

$$V_{\text{out}} = \frac{\alpha V_{\text{in}}}{sCR},$$
$$V_{\text{out}} = \alpha sCRV_{\text{in}}.$$

Table 5. Summarized performance of proposed DCFDCCII applications.

Proposed realization	Integrator	Differentiator
Supply used	± 1.5 V	± 1.5 V
Technology	0.25 μm	0.25 μm
Fully differential	Yes	Yes
Active element	DCFDCCII	DCFDCCII
No. of active elements	1	1
Tuning	Digital	Digital
Component values	R = 2.5 kΩ, C = 400 pF	C = 13 nF, R = 500 kΩ

As evident from these equations, the time constant of the integrator and differentiator are programmable through digital code word alpha. The digital control module (CDC) is implemented for 6-bit. The circuits are simulated with SPICE tool of the TSMC 0.25 μm CMOS process. A pulse input of −0.5 to + 0.5 V and 10 μs time period is applied (high for 5 μs and low for 5 μs). The VM integrator circuit is designed for R = 2.5 kΩ, C = 400 pF. The observed wave shapes for different control word alpha are shown in Fig. 11. The VM differentiator circuit is designed for R = 500 kΩ and C = 13 nF. An input with magnitude 0.5 V is applied and wave shapes observed for different control word alpha are shown in Fig. 12.

The input and output noise spectral densities for CMOS FDCCII based reconfigurable integrator and differentiator are presented in Figs. 13(a) and 13(b). This verifies the essential input to output noise-suppression capability of a differential building block. All of the results that we obtained confirm the theory. The performance of the two realizations is summarized in Table 5.

5. Conclusion

A second order LP/BP filter and reconfigurable integrator and differentiator have been realized using CMOS based FDCCII and its digital variant DCFDCCII respectively. The filter has independent analog tuning of gain, ω_o and Q. The integrator's and differentiator's response are digitally controlled. Our simulation results are based on 0.25 μm technology and 1.5 V supply voltage. This is our dedicated effort to present the facility of analog and digital tuning of FDCCII block.

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