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Pyramid size control and morphology treatment for high-efficiency silicon heterojunction solar cells

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Abstract: This paper investigates the formation process of surface pyramid and etching characteristics during the texturing process of mono-crystalline silicon wafers. It is found that there is an etch rate transition point in alkaline anisotropic etching when {100} plane-dominated etch turns to {111} plane-dominated etch, and the pyramid size has a strong linear correlation with the etch amount at the transition point. Several techniques were developed to control the pyramid size by monitoring and adjusting the etching amount. A wide range of average pyramid sizes were successfully achieved, from 0.5 to 12 μm. The experiments of the pyramid size on the light reflectance, the minority carrier lifetime (MCLT), and the performance of silicon heterojunction (SHJ) solar cells were carried out and analyzed. A desirable range of pyramid sizes was empirically determined by our investigation. In order to reduce the density states on the texturing surface, the wet-chemical smoothing treatment was also investigated. The smoothing treatment improves the passivation quality and the performance of the solar cells. Through pyramid size control and morphology treatment, together with the amorphous silicon (a-Si:H) deposition improvement, and electrode optimization, high performance of SHJ solar cells has been achieved, up to conversion efficiency 23.6%.

Key words: pyramid size; silicon; heterojunction; passivation

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1. Introduction

Silicon heterojunction (SHJ) solar cells are attracting more and more interest from both academia and industrial communities, due to the merits of their high efficiency, low temperature coefficient, and negligible performance degradation. In SHJ solar cells, the crystalline silicon (c-Si) and the amorphous silicon (a-Si:H) layers form the p/n heterojunction, and the substrate surface directly becomes part of the electronic interface[1]. In this case, the surface morphology of the silicon wafer is crucial to the quality of the a-Si:H/c-Si interface and the performance of the SHJ solar cells.

The formation of pyramid structures on the surface of <100>-oriented monocrystalline silicon wafers is an effective approach to reduce light reflection losses of silicon solar cells, including SHJ solar cells[2]. Anisotropic wet chemical etching of silicon wafers using an alkaline solution is a well-known method to generate pyramidal textures on the silicon wafer surface. The pyramid structures form during the etching process because the etching rate in the <100> direction is greater than that in the <111> direction[3]. The textures improve the optical properties at the cost of increased effective surface area and crystallographic imperfections, both of which inherently correspond to a larger number of electrically active defect states in the band gap and thereby result in higher interface recombination losses[4]. Therefore, high-quality passivation of pyramid-textured silicon wafers is quite difficult[5–9]. The control of pyramid size and shape is of vital importance to the passivation quality of silicon surface [characterized by minority carrier lifetime (MCLT)] and the overall performance optimization of SHJ solar cells[2].

In this paper, we study the key factors determining pyramid size and realize effective pyramid size control, and put our emphasis on the effects of pyramid size on the passivation quality of the silicon surface as well as the performance of SHJ solar cells. A desirable pyramid-size range is proposed for SHJ solar cells, different from the small pyramid trend for conventional silicon diffused-junction solar cells.

However, an appropriate pyramid size alone is insufficient to ensure passivation quality and efficiency of SHJ solar cells. Sharp 'peaks', narrow 'valleys', and small imperfect structures embedded among pyramids, as well as micro-roughness on different facets, must be taken into account. Thus, the wet-chemical smoothing treatment is also introduced and investigated to address these issues and make the silicon surface smooth.

Finally, a high efficiency of 23.6% is achieved using the pyramid-size control and the wet-chemical smoothing treatment approaches, coupled with other techniques, including a-Si:H deposition improvement and electrode optimization.

2. Experimental

Phosphor-doped CZ (100) n-type 5-inch silicon wafers with 3.0 Ω·cm resistivity and 200 μm thickness were used in this study. A NaOH solution was initially used to remove saw

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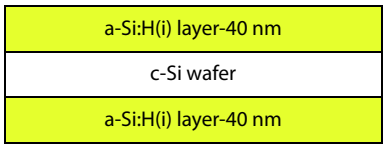

Fig. 1. (Color online) Symmetrical a-Si:H(i)/c-Si/a-Si:H(i) structure for lifetime test structure.

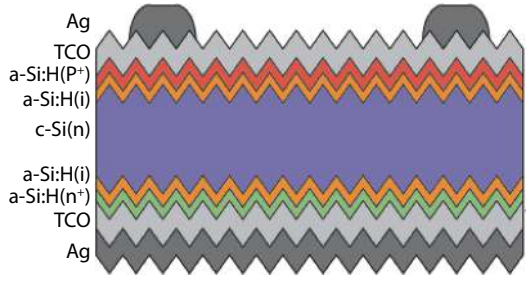

Fig. 2. (Color online) Schematic cross-section of the silicon heterojunction solar cell structure.

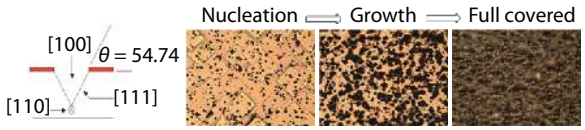

Fig. 3. (Color online) An optical microscopy image of the silicon surface during the texturing progress.

damage. The wafers were textured using an alkaline based wet-chemical etching solution. We then analyzed pyramid morphologies and etching amounts at designated critical points during the texturing processes, using optical microscopy, scanning electron microscopy (SEM), and electronic balance.

Wafer cleaning was performed using RCA cleaning procedures followed by the deposition of an a-Si:H film using a parallel plate RF PECVD reactor operated at radio frequency (13.56 MHz). In order to observe surface passivation, ~40 nm intrinsic a-Si:H [a-Si:H(i)] layers were deposited using SiH_4 and H_2 precusors to form a symmetrical a-Si:H(i)/c-Si/a-Si:H(i) structure for MCLT test. Fig. 1 shows the symmetrical a-Si:H(i)/c-Si/a-Si:H(i) structure. The MCLT was measured using a Sinton Consulting (WTC-120) quasi-steady-state photoconductance (QSSPC) lifetime tester in transient mode[10, 11]. The morphology and the feature of the a-Si:H(i)/c-Si interface was examined using transmission electron microscopy (TEM) technology.

The SHJ solar cells were manufactured using the textured wafers with different pyramid sizes. To further enhance the performance of the SHJ solar cells, a wet-chemical smoothing treatment was investigated. The textured wafers were etched in a HNO_3/HF solution for smoothing treatment. Intrinsic a-Si:H layers were deposited on both sides of the wafers, on which doped p-type and n-type a-Si layers were grown respectively. Finally, a transparent conducting oxide (TCO) film was deposited on the front side using a high vacuum magnetron sputtering system followed by a screen-printed grid electrode with the back side covered by a TCO/Ag stack. Fig. 2 shows the silicon heterojunction solar cell structure.

3. Results and discussions

Fig. 3 illustrates the optical microscopy images of the silic-

Fig. 4. (Color online) A schematic diagram of pyramidal structure forming on wafer surface.

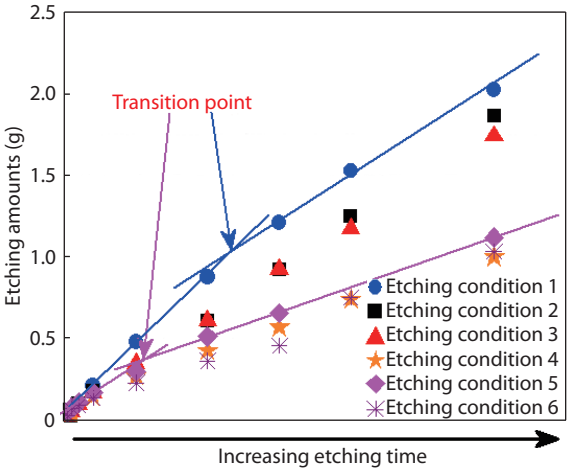

Fig. 5. (Color online) The etching amount increase with etching time.

on wafer surface during the texturing process. In the initial texturing phase, only a few immature pyramids appear and form on the surface. This phase is called the nucleation stage when pyramid size and population density are minimal. As the growth goes on, the pyramids mature in number, size, and shape, followed by a predictable increase in surface density. As the texturing process continues, the pyramids eventually cover the entire wafer surface. After that, the surface morphologies, including the pyramid size and density, almost remain unchanged although etching time increases. Fig. 4 demonstrates a schematic diagram of pyramidal structure formation on a wafer surface during texturing process. As we know, the etching rate in the <100> direction is greater than that in the <111> direction. Therefore, in the initial stages of the etching process, several small pyramids with {111} oriented facets are formed. The wafer surface consists of {100} and {111} facets. The proportion of the {111} facets increases with the pyramid size and density as the texturing process continues. As the pyramids all aggregate, the wafer surface is saturated by pyramids of {111} facets.

Fig. 5 shows the change in etching amounts versus etching time under different texturing conditions. Our research indicates a clear transition point in the relationship curve between etching time and amount. Combining the results obtained from Fig. 3 and Fig. 4, we conclude that the transition point results from the etch rate difference between the <100> and <111> directions. The etching amount at the transition point and the pyramid size under different texturing conditions are shown in Table 1. We find that the pyramid size has almost a linear correlation with the etching amount at the transition point, though additive type, amount, alkali concentration, and solution temperature is different. The relationship is shown in Fig. 6.

High etching amount at the transition point results in large pyramid sizes, while low etching amount yields small pyr-

Table 1. The etching amount at the transition point and the pyramid size under different texturing conditions.

NaOH (wt%)	Temperature (°C)	Additive			Etching amounts at the transition (mg)	Pyramids size (μm)
		IPA (v/v%)	GP (v/v%)	TS41 (v/v%)		
0	85	0	0	0	0	0
5	85	0	0.1	0	1200	10.2
2	85	10	0	0	580	6
5	85	0	0.2	0	300	3.3
6	85	0	0.15	0	400	4
5	85	0	0.33	0	200	2.2
4	80	0	0	1.5	350	3.1

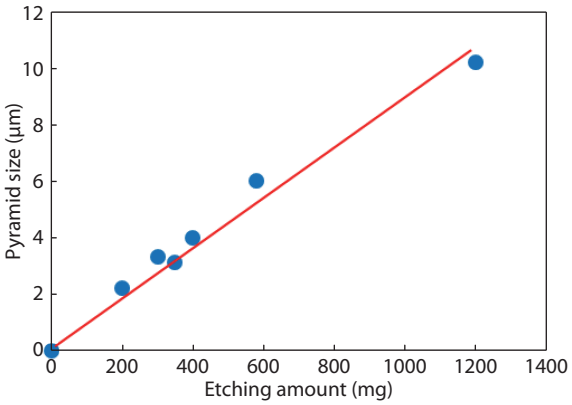

Fig. 6. (Color online) The relationship between pyramid sizes and etching amounts at the transition.

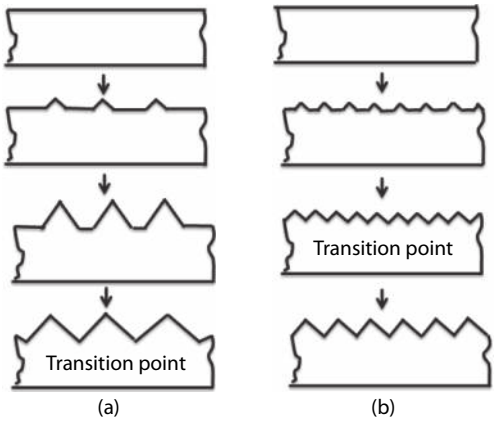

Fig. 7. The formation process of both large and small pyramids.

amid sizes. In our experiments, we observed pyramid growth and convergence before the transition point during the texturing process. At the transition point, we found that pyramids combined, covering the full wafer surface. At this point, the etching progress became isotropic etching in the <111> direction. After the transition point, the change in pyramid size was negligible. Therefore, we conclude that the etching amount at the transition point from {100} to {111} planes determines averaged pyramid size. As explained in Fig. 7, large etching amount at the transition point equates to longer anisotropic etching process shown in Fig. 7(a); low etching amounts at the transition point equates to rapid pyramid formation and surface coverage as illustrated in Fig. 7(b). At the conclusion of the texturing process, the pyramid density of the high etching amount at the transition point is lower compared to that of the low etching amount.

Therefore, the pyramid size can be controlled by monitoring and adjusting the etching amount at the transition point, through modifying additive type or amount, alkali concentration, and solution temperature.

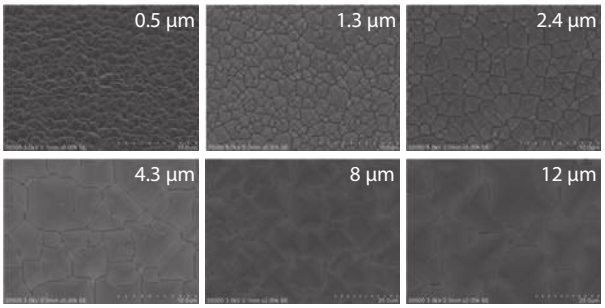

Fig. 8. Scanning electron microscope (SEM) images of samples with various pyramid sizes.

Using this method, the texturing process yielding an average pyramid size of between 0.5 to 12 μm was successfully achieved. Fig. 8 shows SEM images of the samples with different pyramid sizes.

The influence of the pyramid size distribution on MCLT and open circuit voltage (V_{oc}) is summarized in Fig. 9, which illustrates a rise of MCLT as the pyramid size increases at the early stage. This can be explained by considering that larger pyramids result in a lower density of valleys, which are known to be the centers for epitaxial growth and local cracks of the intrinsic a-Si:H layer[2, 12]. Fig. 10(a) is the transmission electron microscopy (TEM) image at the a-Si:H(i)/c-Si interface of small pyramid (< 1 μm), while Fig. 10(b) shows the locally enlarged image. At the a-Si:H(i)/c-Si interface, we find the unintentional local epitaxial growth, which was reported to degrade passivation quality[4, 12, 13]. The local epitaxial growth becomes less obvious with large pyramid sizes (not shown here). This agrees with the literature[14–16]. In addition, we find out that above a specific threshold, further increases in pyramid size do not lead to effective increases in MCLT, suggesting that the recombination processes at defects on the large pyramid facets, instead of those in the valleys, dominated the overall recombination at interfaces[17, 18]. Too large a pyramid size can lead to less uniform and regular morphology thus increasing the density of surface defects. Therefore, MCLT is found to decrease when pyramids become excessively large. Fig. 9(b) shows V_{oc} of cells with different pyramid sizes. Surface recombination directly affected V_{oc}, hence V_{oc} also decreases when pyramid size becomes excessively small or large.

An analysis of pyramid size on light reflection and short circuit current density (J_{sc}) is summarized in Fig. 11. Excessively small pyramids increase the number of valleys and edges. This

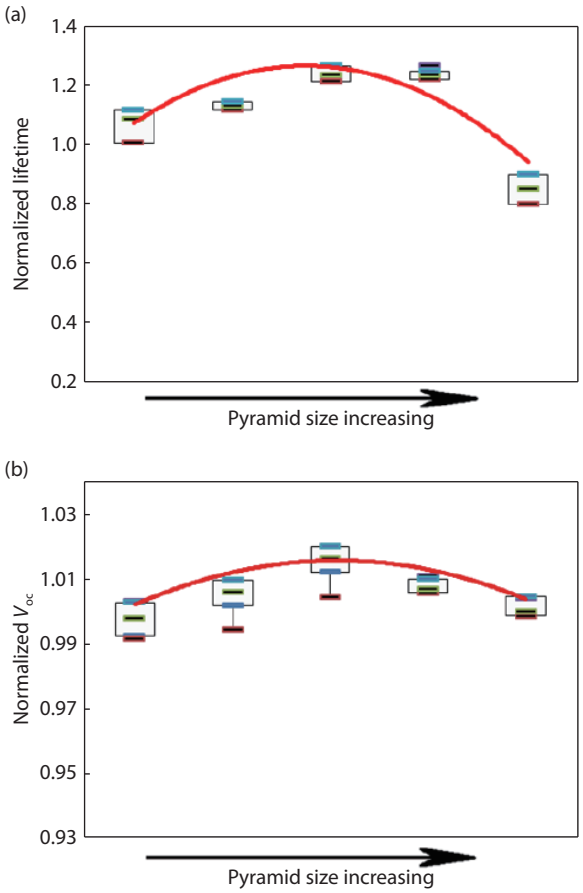

Fig. 9. (Color online) The influence of pyramid size distribution on MCLT and V_{oc}.

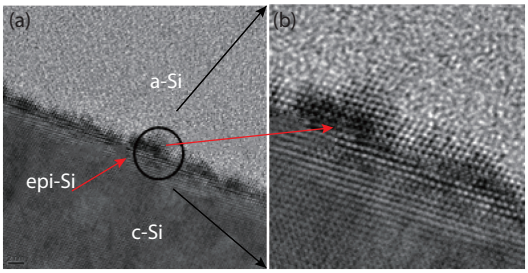

Fig. 10. (Color online) The transmission electron microscopy (TEM) image at the a-Si:H(i)/c-Si interface of excessively small pyramid.

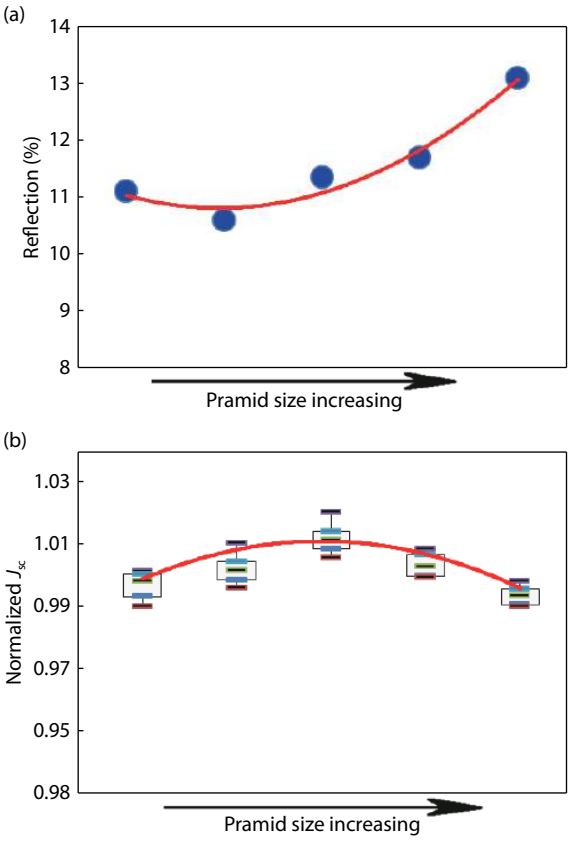

Fig. 11. (Color online) The influences of pyramid size on wafer reflection and J_{sc}.

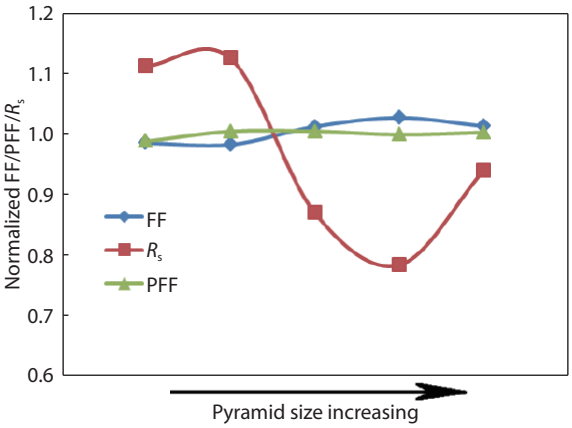

Fig. 12. (Color online) The relationship between FF/PFF/R_s and pyramid size.

can increase reflectivity. Excessively large pyramids can result in decreased coverage and thus increase reflectivity. Therefore, the reflectivity initially decreases followed by a dramatic increase with pyramid size increases. If other factors are not taken into account, the trend of current and reflectivity is reversed, therefore J_{sc} initially increases and decreases drastically with pyramid size increasing.

Fig. 12 shows the relationship between fill factor (FF) and pyramid size. Small pyramids result in low FF and FF increases when initial pyramid size increases. However, further increases in pyramid size dose not lead to any increase in FF.

Then we analyzed the PFF (pseudo fill factor) and R_s (series resistance) of the samples. PFF is the fill factor of the solar cell without the effects of series resistance. The PFF curve in Fig. 12 shows there is no obvious difference among the PFF of the samples with different pyramid sizes, except for those with excessively small sizes. As we analyzed above, the valleys of the excessively small pyramid can be centers for epitaxial growth of the intrinsic a-Si:H layer which can destroy the character and passivation quality of the a-Si:H(i)/c-Si interface. So the PFF of excessively small pyramid is lower than that of samples with larger pyramids. However, the PFF has almost no change with pyramid size increasing above a certain threshold, which shows the passivation quality of the a-Si:H(i)/c-Si interface is similar.

From the R_s curve in Fig. 12, we can find there is a well-corresponding relationship between the change tendency of the R_s and the FF. So, we can conclude that the pyramid size influences the FF through its effect on the R_s which includes the contact resistance, bulk resistance of the TCO and the printing fingers, and also the resistance of the a-Si:H(i)/c-Si interface.

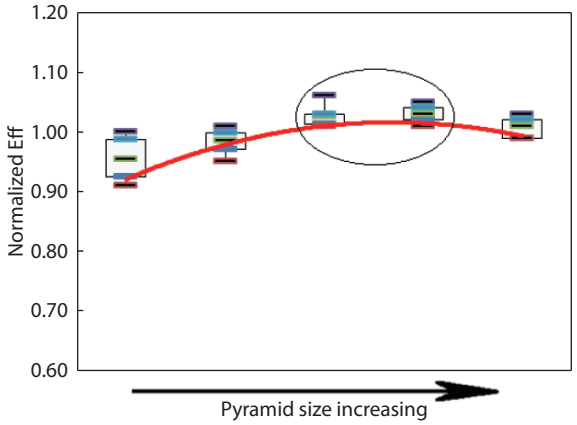

Fig. 13. (Color online) The influence of pyramid size on solar cell efficiency.

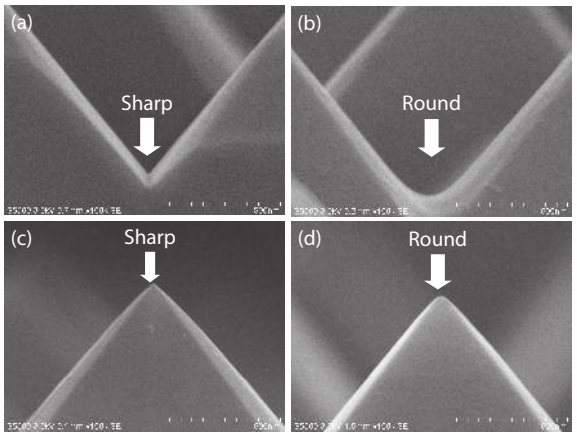

Fig. 14. Typical SEM images of a pyramid as-textured and post-smoothing: (a) and (c) is the valley and the tip of pyramid as-textured; (b) and (d) is the valley and the tip of pyramid post-smoothing.

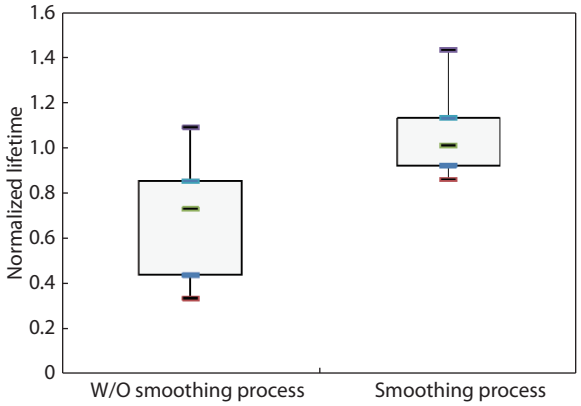

Fig. 15. (Color online) Comparison of minority carrier lifetime with and without smoothing process.

However, further investigations are still required to clarify and explain the mechanisms affecting FF.

In Fig. 13, the influence of pyramid size on solar cell conversion efficiency (Eff) is a combined effect of the influences on V_{oc}, J_{sc}, and FF. Here, a desirable range of pyramid sizes are obtained as indicated by the black circle.

However, an appropriate pyramid size alone is insufficient to achieve high MCLT and V_{oc}. Sharp 'peaks', narrow 'valleys', and small imperfect structures embedded among pyramids, as well as micro-roughness on different facets, could degrade a-Si deposition coverage and passivation quality. So an isotropic etch step using chemical based smoothing was carried out in order to make pyramid surface 'round' and 'smooth', with small imperfect structures mostly removed.

Fig. 14 compares typical SEM images of a pyramid valley as-textured and post-smoothing, which shows the smoothing process makes the pyramid surface 'round' and 'smooth'. The 'round' and 'smooth' surface can enhance the passivation quality of the a-Si:H(i)/c-Si interface. Fig. 15 shows the smoothing process results in a ~25% gain in MCLT.

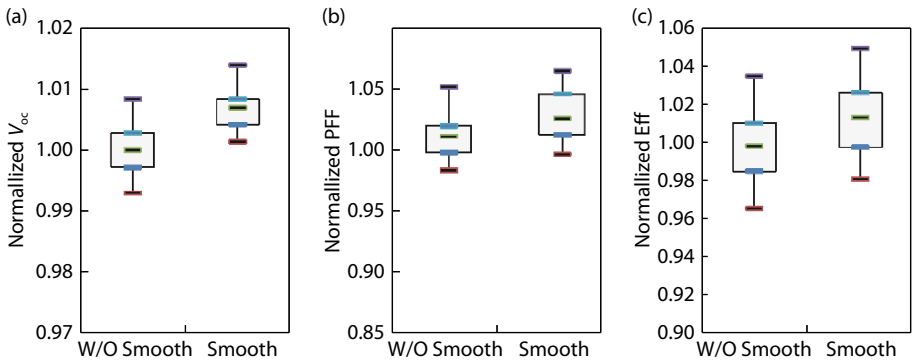

Fig. 16. (Color online) Comparison of (a) V_{oc}, (b) PFF, and (c) Eff between solar cells with and without the smoothing process.

Fig. 16 shows the smoothing process can result in a ~0.7% gain in V_{oc} and 1.3% gain in PFF. The profits of MCLT, V_{oc} and PFF attributed to the enhancement of the passivation quality of the a-Si:H(i)/c-Si interface. Eventually, the smoothing process enhances the Eff by ~0.2%.

Using the pyramid size control and morphology treatment, together with other process optimization in a-Si deposition and electrode formation processes, we have achieved SHJ solar cell efficiency up to 23.6% with V_{oc} 734 mV, J_{sc} 39.9 mA/cm^2 (area 144 cm^2) and FF 80.6% (Fig. 17, in-house testing). The efficiency is already verified by 18th Institute of China Electronic Technology Group Corporation CETC (23.63%).

4. Conclusion

In this paper, we investigated the pyramid size and etching amounts during wafer texturing processes. We find that the pyramid size has a linear correlation with etching amounts at the transition points from planes {100} to {111}. Our research indicates that pyramid size can be controlled by monitoring and varying the etching amounts at the transition point. Av-

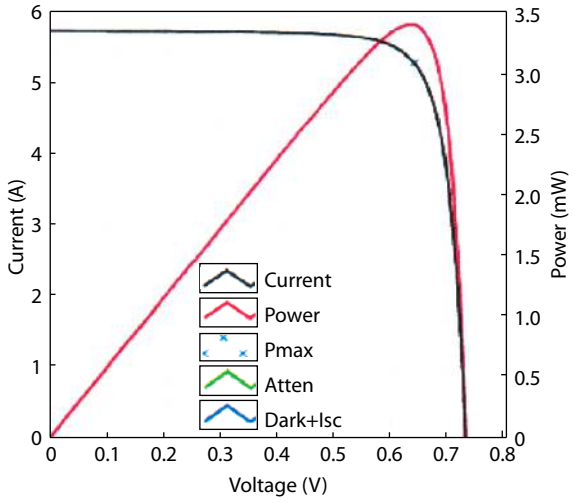

Fig. 17. (Color online) Illuminated *I*–*V* characteristics of SHJ cell of 23.6% efficiency.

erage pyramid sizes of 0.5 to 12 μm were achieved using this method. A desirable range of pyramid sizes were obtained by our investigation for SHJ solar cells. The smoothing treatment can further enhance passivation quality and the performance of the solar cell. Using the pyramid size control and morphology treatment technology together with the other optimized processes, a high efficiency 23.6% of SHJ solar cell is achieved.

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