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ARTICLES

2D study of AlGaN/AlN/GaN/AlGaN HEMTs' response to traps

A. Hezabra[1], N. A. Abdeslam[1], N. Sengouga[1, †], and M. C. E. Yagoub[2]

[1]Laboratory of Metallic and Semiconducting Materials (LMSM), Mohammed Khider University, Biskra, Algeria

[2]School of Electrical Engineering and Computer Science, University of Ottawa, Ottawa, ON, Canada

Abstract: In this work, the effects of GaN channel traps and temperature on the performance of AlGaN/AlN/GaN/AlGaN high electron mobility transistors (HEMTs) on Si (111) substrate, were investigated. 2D simulations carried out using the Silvaco TCAD simulator tool for different drain and gate voltages showed that acceptor-like traps in the channel have a significant influence on the DC and RF characteristics. It was found that deeper acceptors below the conduction band with larger concentration have a more pronounced effect on the transistor performance. Meanwhile, the donor-like traps show no influence. Pulsing the device with different pulse widths and bias conditions, as well as increasing temperature, showed that the traps are more ionized when the pulse is wider or the temperature is higher, which can degrade the drain current and thus the DC characteristics of the transistor. Passivation of the transistor has also a beneficial effect on performance.

Key words: AlGaN HEMT; AlGAN/AlN/GaN structure, silicon substrate; Silvaco; trapping effects; channel traps

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1. Introduction

Nowadays, AlGaN/AlN/GaN high-electron mobility transistor (HEMT) technology is increasingly attracting interest from researchers due to AlGaN's wide band gap, high electron mobility, and high breakdown voltage[1–3]. The important piezoelectric polarization present in GaN and AlN semiconductors induces a large piezoelectric and spontaneous charge at the interface of the AlGaN/AlN/GaN/AlGaN heterojunction structure. This creates a high two-dimensional electron gas (2DEG) density near the interface, which is the effective channel of the structure. The high density of 2DEG, the mobility and the large band gap characteristics lead to a high power output, suitable for a variety of high-frequency high-power applications. But, unfortunately, this also leads to an increase in the lattice temperature. Biased gate and drain contacts induce converse piezoelectric stress that can influence the piezoelectric polarization charge and further influence the 2DEG density and output characteristics[4].

In fact, because of its higher 2DEG density, even using an ultrathin AlN barrier layer of thickness well below 5 nm, a high aspect ratio (gate length on gate-to-channel distance) can mitigate short-channel effects[5, 6]. Several works have demonstrated that the AlGaN/AlN/GaN HEMT technology can reach a 2DEG density of up to 2.1 × 10^{13} cm^{-2}[6] at the hetero-interface and a high drain current of 2 A/mm[2, 7]. Despite substantial progress realized in this technology over the last years[8], its performance is still curtailed by the presence of electronic traps in the device structure.

The traps may be at the surface, on the bulk or at the interface, causing effects such as current collapse, transconductance frequency dispersion, and gate- and drain-lag[2]. To the best of the authors' knowledge, quite a limited number works focus solely on describing the effects of the presence of traps in the device structure.

In order to provide an appropriate understanding of such effects to enable further technological advances, an analysis of trapping effects on the device performance is clearly required. In addition to this, very few analytical models have been developed to handle the high temperature effect on GaN-based devices[9–11] and they are primarily tailored for use in circuit simulations, not for device optimization. Furthermore, they are mainly on experimental data, not simulations[12, 13].

To efficiently address the above issues, different directions were explored, allowing pertinent results, which will be quite useful for researchers, to be obtained. To be specific, we investigated (i) the influence of traps on the DC/RF characteristics of AlGaN/AlN/GaN/AlGaN HEMTs, such as their level within the band gap and their concentration, (ii) the effect of temperature on the device performance, (iii) how the transistor reacts when pulsed with different pulse widths, and finally (iv) the effect of passivation on the device features.

2. Simulation details and device structure

For simplicity, the investigated AlGaN/AlN/GaN/AlGaN HEMT structure has the same dimensions as the one described in Ref. [1]. As shown in Fig. 1, it consists of three thin $Al_xGa_{1-x}N$ layers with aluminum fractions of 0.6, 0.4 and 0.2, respectively, a 2.44 μm thick GaN channel layer as buffer layer, a 1 nm ultrathin AlN barrier layer and an $Al_{0.23}Ga_{0.77}N$ layer[1]. The gate is placed asymmetrically with a length L_g of 3 μm and a width W_g of 1000 μm, fabricated on a Si wafer. The source-gate separation L_{gs} and gate-drain distance L_{gd} are 1 μm and 4 μm, respectively. Two-dimensional physics based numerical simulations have been carried out using the commercially available TCAD-Silvaco[14].

Note that, except for the case where the temperature was

Correspondence to: N Sengouga, n.sengouga@univ-biskra.dz, nourseng2015@gmail.com

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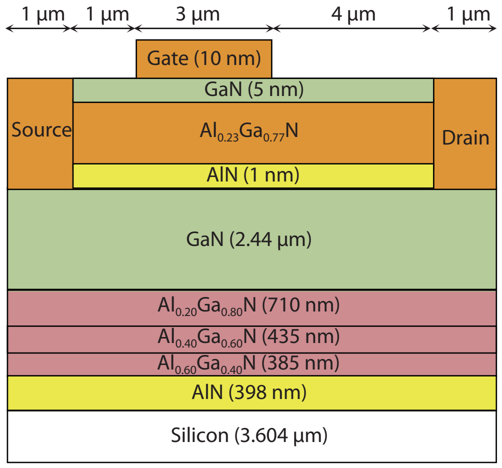

Fig. 1. (Color online) Cross-section of the AlGaN/AlN/GaN/AlGaN HEMT structure simulated in this work.

Table 1. Summary of the material parameters used in the simulations.

Material parameter	GaN	AlGaN	AlN
Band gap (eV)	3.42	3.91	6.12
Effective conduction band density of state (10^{18} cm^{-3})	2.24	2.7	4.42
Relative permittivity	9.5	–	8.5
Electron affinity (eV)	4	–	1.84
Electron saturation			

varied to study its effect on the device performance, the DC simulations carried out in this work were performed at room temperature.

The TCAD-Silvaco simulations solve a system of three equations, i.e, the three fundamental equations governing the semiconductor behavior, namely the Poisson equation and the electron/hole continuity equations. Drift-diffusion (DD) transport model equations are also solved self-consistently. The software produces numerical solutions by calculating the values of the unknown variables at each grid point of the device. An internal discretization process converts the original continuous model into a discrete nonlinear algebraic system, which is then solved using an iterative process until the predefined convergence criteria are satisfied[14].

The processes related to generation-recombination are known to fall into six main categories, but the most frequent and dominant process is that of Shockley–Read–Hall (SRH) recombination[15]. The transitions occur in the presence of a trap (or defect) within the forbidden gap of the semiconductor. Since trap centers influence the space charge density in the semiconductor bulk and the recombination statistics, they have to be included in the space charge term in the Poisson equation, in addition to the ionized donor/acceptor impurities. It has been established from solid physics that they can be summarized as interface-fixed charges, interface-trap states and bulk-trap states. Interface-fixed charges can be modeled as a sheet of charges at the interface and therefore controlled by the interface boundary condition while interface-traps and bulk-traps add space charges directly into the right hand side of the Poisson equation.

The induced electric field due to the polarization phenomenon contributes to the formation of 2DEG density at the AlN/GaN interface, without the need for any intentional doping. The theoretical methods used for estimating the polarization charges are described in Ref. [16]. The polarization charge at the AlN/GaN interface is modeled as a fixed interface charge with + σ_{pol} = 1.7 × 10^{13} cm^{-2}[2, 17]. The AlN layer was used over the Si substrate to help dissipate heat as its thermal conductivity is high, thereby reducing the impact of self-heating in the device[18]. Note that low field mobility for both electrons and holes was taken into account in this work by using the Albrecht mobility model[19]. The parameters used in our simulations are summarized in Table 1.

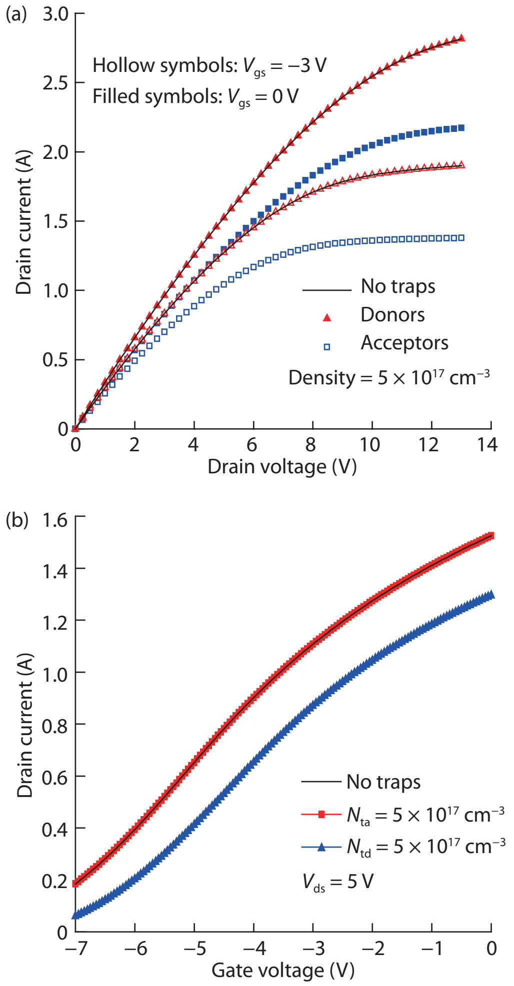

Fig. 2. (Color online) Simulated (a) DC characteristics for different gate-source voltages and (b) transfer characteristics in the presence of acceptor and donor traps in the GaN channel compared to the case with no traps. Trap energy level is 0.3 eV below E_c for the acceptor and 0.3 eV above E_v for the donor.

3. 2D simulation results

3.1. Types of traps

Two-dimensional physical-electrical simulations were performed to first determine which type of traps present in the studied heterostructure device has more influence. Fig. 2 shows the influence of acceptor traps and donors on the DC characteristics of the transistor. They decrease the drain current since they reduce the effective density of electrons in the channel while the donors do not. Knowing that the channel must be undoped in order to mitigate the scattering phenomenon, the excess electrons have enough room to diffuse because the channel is formed, in our case, by a large GaN layer.

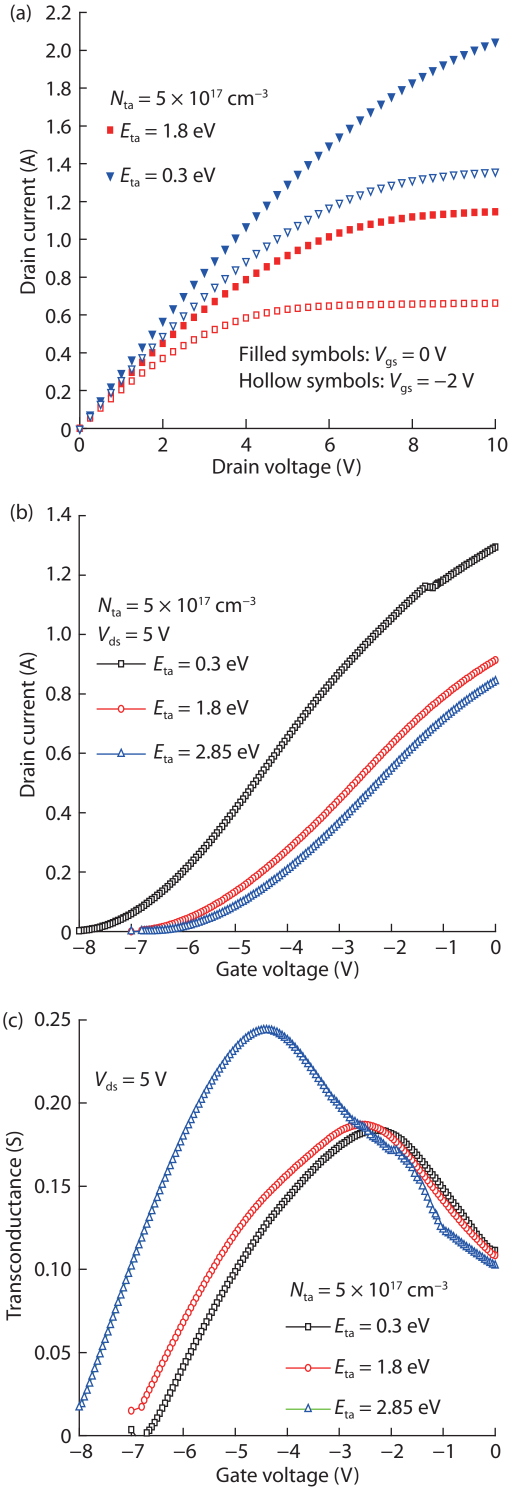

Fig. 3. (Color online) Influence of acceptor traps located below the conductance band on the (a) output characteristics, (b) transfer characteristics, and (c) transconductance of the AlGaN/AlN/GaN/AlGaN HEMT device at $V_{ds} = 5$ V. Acceptor traps in the GaN channel have a density of 5×10^{17} cm^{-3}.

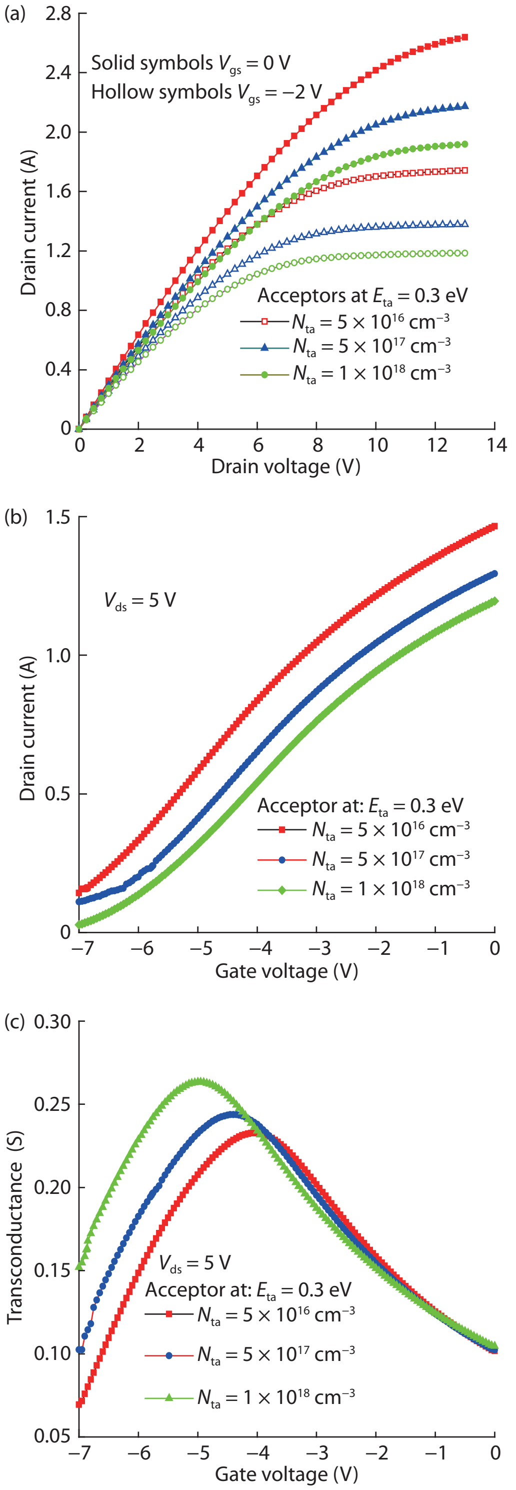

Fig. 4. (Color online) Influence of acceptor trap concentration on the (a) output and (b) transfer characteristics and (c) the transconductance of the device. Acceptor traps in the channel are located at E_{ta} = 0.3 eV. The drain voltage is $V_{ds} = 5$ V.

Note that these conclusions are in agreement with those reported in Ref. [2].

Fig. 3 shows the influence of acceptor traps with different trap energy levels on the DC and transfer characteristics and the transconductance of the device. As can be seen, acceptor traps whose energy levels lie deep inside the band gap cause a significant drain current decrease and also a shift in the pinch-off voltage. This can also be verified by the fact that the maximum transconductance increases for deeper acceptor traps.

Under the biased conditions of a drain-source voltage V_{ds} = 5 V, the trap acceptors are all ionized in the channel and thereby cause an important degradation of the drain current[2]. Fig. 4 shows the influence of the acceptor trap density on the output and transfer characteristics and the transconductance of the HEMT. A significant decrease of the drain current and an increase (absolute value) of the pinch off voltage

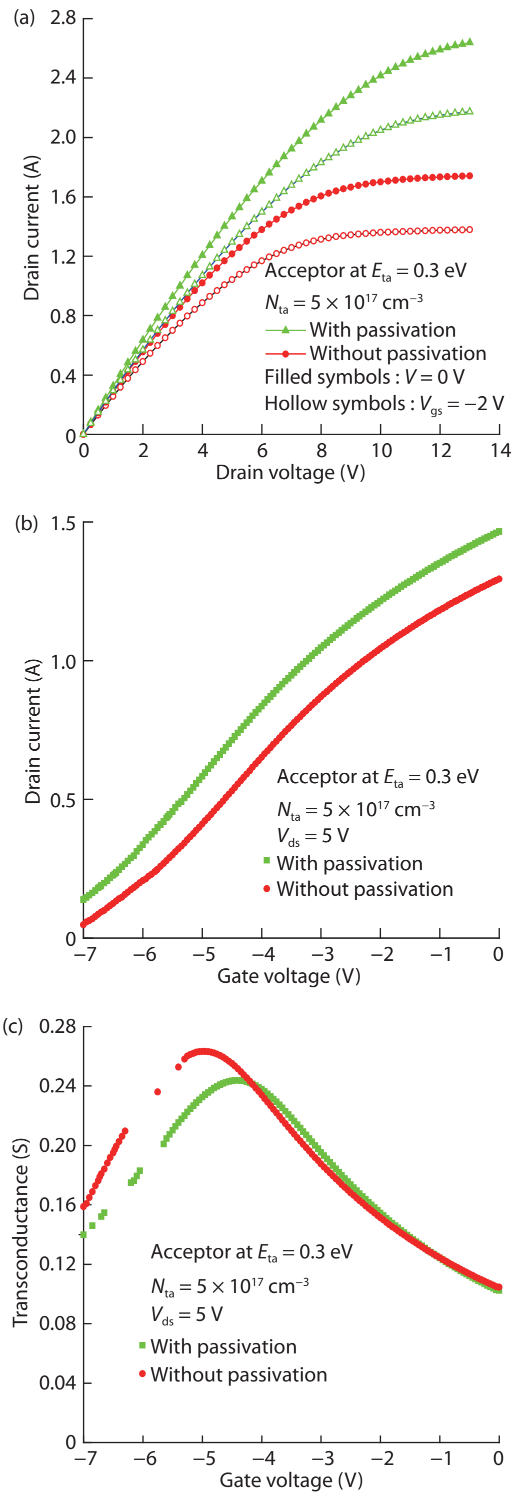

Fig. 5. (Color online) Passivated and unpassivated structures under the same bias conditions. (a) The output and (b) transfer characteristics and (c) the transconductance of the device. Acceptor traps in the channel have a density of N_{ta} = 5 × 10^{17} cm^{-3} and are located at E_{ta} = 0.3 eV below the conduction band.

(where the transfer characteristics cross the V_{gs} axis) can be observed with increasing acceptor trap concentration in the channel. As can be seen, the maximum value of the transconductance g_{mmax} is shifted in the direction of negative gate bias values and increases by 0.10 S.

3.2. Passivated and unpassivated cases

Passivated and unpassivated devices exhibit different increases in power dissipation at high drain bias currents. Low power dissipation is observed in unpassivated devices due to a large reduction in the output power, induced by deeper dispersion effects[20, 21]. In fact, unpassivated structures suffer from lower output power and lower power gain. So, in order to reduce the negative impact of the surface states, such as RF current collapse, a SiO_2 surface passivation was introduced. Fig. 5 shows the impact of the passivation on the device electrical characteristics.

It is well known that the surface of the material contains a large concentration of donor-like and acceptor-like traps which surpasses > 10^{13} cm^{-2}[22] and which degrades the drain current. As can be seen from this figure, the pinch-off voltage is shifted in the direction of negative gate voltage, which indicates more gate control on the device.

3.3. Temperature effect

Since temperature plays a significant role in the device performance, a study was carried out at different temperatures. Acceptor-like traps were introduced in the GaN channel with a concentration of N_{ta} of 5 × 10^{17} cm^{-3} and an energy level E_{ta} of 0.3 eV below the conduction band.

As shown in Fig. 6, the drain current decreases when the temperature increases, due to the fact that the acceptor traps are ionized. In fact, increasing the temperature degrades the drain current and shifts the pinch-off voltage due to the temperature rise of the device.

3.4. Effect of pulse width

The traps-related current collapse phenomenon was also studied in this work by investigating the effect of pulse width. As shown in Fig. 7, V_{gs} was pulsed between 0 and −5 V while V_{ds} was kept at 25 V. The drain current is significantly reduced, demonstrating the current collapse phenomenon. The cause of the current collapse is mainly the change in the charge state of the acceptor doping deep in the channel under the gate. For completeness, the unstressed bias remained on the device until the traps became de-populated by electrons and the drain current returned back to its original value.

Indeed, intentional doping is not necessary for GaN based devices[23] due to the high polarization and the 2DEG density, which is of the order of 10^{13} cm^{-2}. Moreover, doping could reduce the electron mobility via scattering, as highlighted in Fig. 7, where the drain current is reduced during the pulse. In fact, by reducing the pulse duration, the drain current is still decreased, but to a lesser degree since, when the pulse ends, the current can rapidly recover its initial value even if the pulse is repeated as in Fig. 8 (V_{gs} between 0 and −5 V and V_{ds} = 10 V).

4. Conclusion

Investigations of the electrical performance of AlGaN/AlN/GaN HEMTs grown on Si (111) substrate were carried out through 2D TCAD based numerical simulations. The results indicate an important influence of acceptor-like traps located in the channel on the DC and RF characteristics. A deeper position in the band gap under the conduction band and a larger concentration were considered, showing a significant decrease of the drain current. Meanwhile the donor-like traps show no influence. Pulsing the device with different pulse widths and bias conditions, as well as increasing temperature, showed that the traps are more ionized when the pulse is wider or the temperature higher, which can degrade the drain current, and thus the DC characteristics of the transistor.

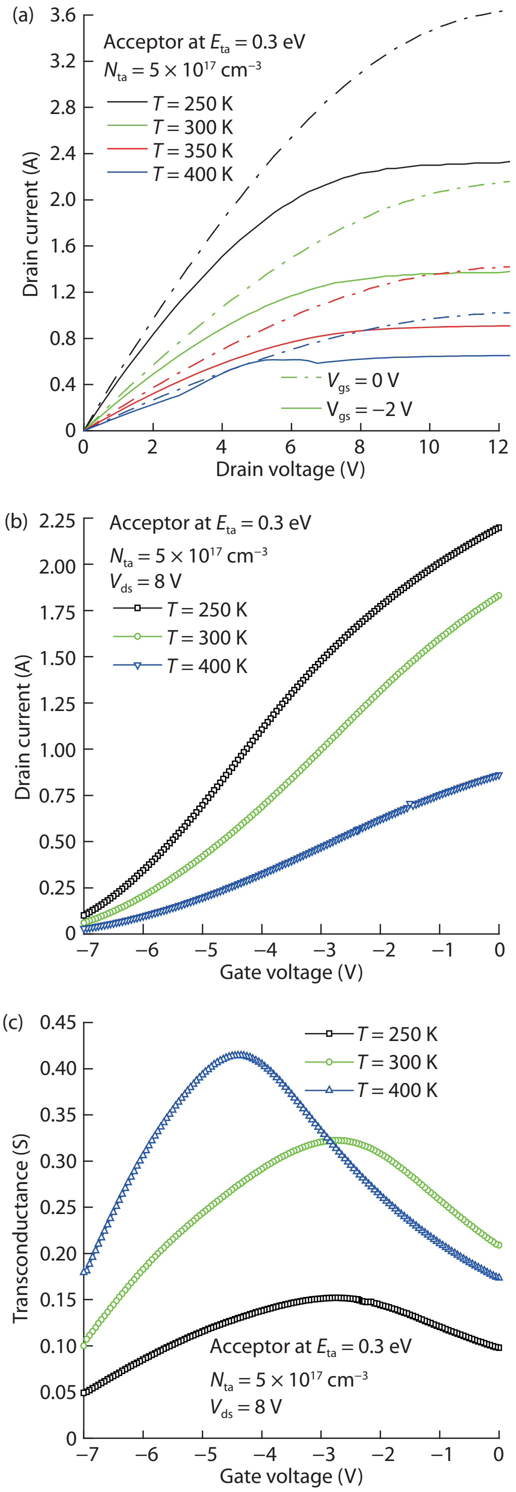

Fig. 6. (Color online) Influence of the temperature variations on (a) DC characteristics, (b) transfer characteristics, and (c) the transconductance of the device in the presence of acceptor traps (N_{ta} = 5 × 10^{17} cm^{-3}, E_{ta} = 0.3 eV).

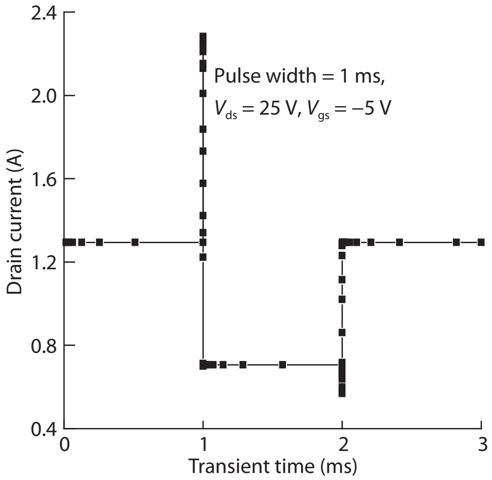

Fig. 7. Drain current recovery curve after bias stressing with a pulse width of 1 ms on the gate (V_{gs} = 0, −5 V and V_{ds} = 25 V) in the presence of acceptor-like traps (N_{ta} = 5 × 10^{17} cm^{-3}, E_{ta} = 0.3 eV).

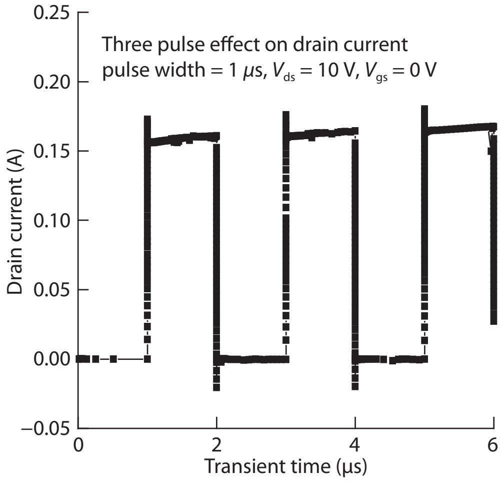

Fig. 8. Drain current recovery curve after bias stressing on the gate (V_{gs} = 0, −5 V and V_{ds} = 10 V) in the presence of acceptor-like traps (N_{ta} = 5 × 10^{17} cm^{-3}, E_{ta} = 0.3 eV).

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