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High-performance RF Switch in 0.13 μm RF SOI process

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Abstract: A high-performance single-pole single-throw (SPST) RF switch for mobile phone RF front-end modules (FEMs) was designed and characterized in a 0.13 μm partially depleted silicon-on-insulator (PD SOI) process. In this paper, the traditional series-shunt configuration design was improved by introducing a suitably large DC bias resistor and leakage-preventing PMOS, together with the floating body technique. The performance of the RF switch is greatly improved. Furthermore, a new $R_{on} \times C_{off}$ testing method is also proposed. The size of this SPST RF switch is 0.2 mm^2. This switch can be widely used for present 4G and forthcoming 5G mobile phone FEMs.

Key words: RF switch; SOI; insertion loss; isolation; linearity

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1. Introduction

RF front-end modules (FEMs) have become increasingly prominent with the increase in 4G and 5G mobile communication which is required for multi-band and multi-mode applications. The RF switch is the largest demand module in the RF FEM product; its performance directly determines the entire RF transceiver system. Insertion loss and isolation are two major parameters that measure the performance of the RF switch in addition to the linearity requirement (harmonics) and power handling capacity. However, achieving a trade-off among these various parameters is often difficult. Most previous studies on RF switch performance, such as those on insertion loss, isolation, and $P_{0.1\ dB}$, harmonics, are insufficient, since they do not consider the $R_{on} \times C_{off}$ metrics. Hence, this paper not only focuses on the optimization of the primary RF switch parameters, such as insertion loss, isolation, $P_{0.1\ dB}$, and linearity, but also measures the product $R_{on} \times C_{off}$. A high-quality SPST RF switch is designed by improving switch structure and parameter optimization[1] in a 0.13 μm PD SOI process.

2. RF SOI process

The wireless communication industry has always been interested in integrating a multi-mode multi-band RF switch in one small and low-cost system. Undoubtedly, the RF SOI process is cost effective for RF switches in comparison to other technologies, such as conventional bulk CMOS, silicon-on-sapphire, and GaAs[2–4].

The low-R_{on} body-contact (BC) transistor is selected for the RF switch design as it can reduce insertion loss in the case of a large voltage swing and also has high voltage handling capability through device stacking, which can greatly increase linearity, while reduced C_{off} for improved isolation can also be achieved in the design. Fig. 1 shows inherently small overlap capacitance C_{ov} and junction capacitance C_j of the transistor while the switch in the off state. R_{on} is measured from a single transistor; usually we measured I_d @ 2.5 V V_g, 0.05 V V_d, then obtained I_{din} by normalizing I_d to transistor width. In addition, we obtain C_{off} from C_{ov} plus C_j, with C_{ov} measured @ 0 V V_g, 45 mV 1 MHz AC condition, while C_j is measured @ 0 V V_b, 45 mV 1 MHz AC condition. Eqs. (1) and (2) give the transistor's R_{on} and C_{off} measurement formulas and the figure of merit (FoM) of the RF switch can be obtained by using Eq. (3).

$$R_{on}\,(\Omega/\mu\mathrm{m}) = \frac{V_d}{I_{din}}\left(I_{din} = \frac{I_d}{W}\right), \tag{1}$$

$$C_{off}\,(\mathrm{fF}/\mu\mathrm{m}) = \frac{1}{2}C_{ov} + C_j, \tag{2}$$

$$\mathrm{FOM}\,(\mathrm{fs}) = R_{on}C_{off}. \tag{3}$$

By ignoring the influence of other capacitances, only the effects of gate-to-source and gate-to-drain on overlap capacitance C_{ov} are considered, because source-to-body, drain-to-body, and gate-to-body are too small for $C_{ov,}$ and junction capa-

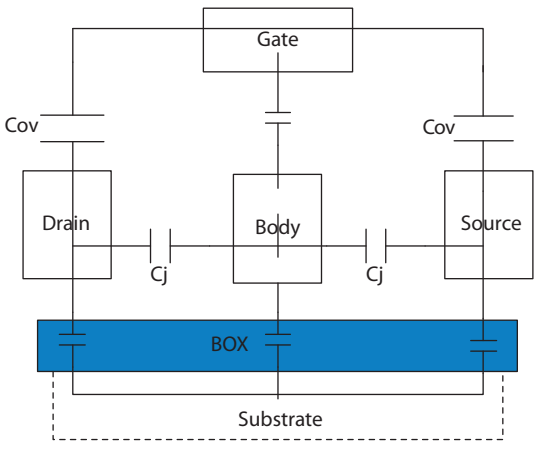

Fig. 1. (Color online) Simplified capacitive models.

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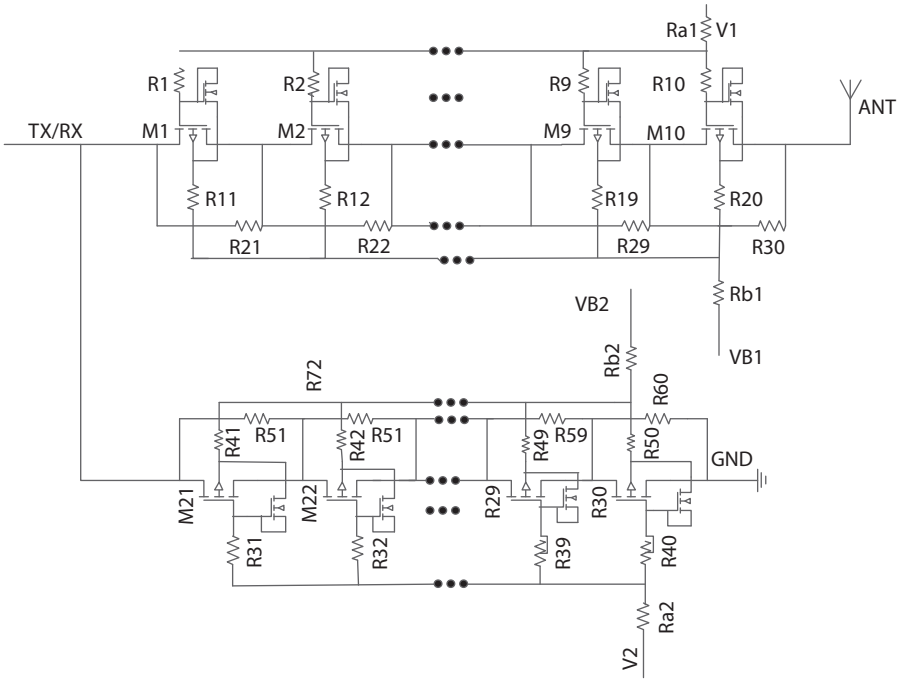

Fig. 2. Proposed RF switch.

citance C_j mainly refers to source-to-body and drain-to-body. As reducing $R_{on} \times C_{off}$ can improve the performance of linearity ($P_{0.1\ dB}$, harmonic), R_{on} reduction will be considered first[5]. R_{on} reduction for intrinsic FETs is fundamentally achieved through channel length shrink. However, this reduction must be carefully balanced with a corresponding decrease in break down voltage of BVD_{ss}[6]. Reducing BVD_{ss} requires a large FET stack number and chip area. Increased high isolation can be achieved by reducing C_{off} through optimization of the RF switch transistor layout.

The RF SOI Platform is much more preferable for the RF Switch module due to the excellent $R_{on} \times C_{off}$ performance; the ideal RF Switch should have much lower R_{on} in the turned-on state to transmit the RF signal with low insertion loss and high linearity. Furthermore, the RF switch should also have lower parasitic capacitance to block or isolate the unwanted RF signal in the turned-off state to maintain high terminal isolation. In most situations, R_{on} should be traded off against C_{off}, it is difficult to improve R_{on} while maintaining C_{off} at the same level and vice versa. Therefore, $R_{on} \times C_{off}$ is a good figure of merit by which to assess the RF SOI Platform performance.

3. Design optimization of RF switch

The most important parameters of the RF switch are insertion loss (IL), isolation (ISO), and power handling capacity measured by $P_{0.1\ dB}$. Isolation and insertion loss are limited primarily by off-state parasitic capacitance and on-state current leakage. The IL and ISO can be expressed by Eqs. (4) and (5).

$$\mathrm{IL} = -20\log\frac{R_o}{2R_0 + R_{on}}, \tag{4}$$

$$\mathrm{ISO} = -10\log\frac{2R_0}{2R_0 + \frac{2}{\omega C_{off}}}. \tag{5}$$

In commercial mobile phones, the GSM band transmit mode requires a power level at the antenna port as high as 35 dBm at 0.9 GHz and 33 dBm at 1.9 GHz and their maximum output power and maximum peak to peak voltage can be calculated as follows:

$$P_{watt} = 10^{\frac{35}{10}} \times 0.001 = 3.16\ \mathrm{W}, \tag{6}$$

$$V_{peak} = \sqrt{2P_{watt}Z_0} = 17.8\ \mathrm{V}, \tag{7}$$

$$V_{max} = V_{peak}\left(1 + \frac{\mathrm{VSWR} - 1}{\mathrm{VSWR} + 1}\right) = 28.5\ \mathrm{V}. \tag{8}$$

From Eqs. (6)–(8), 35 dBm power can be translated into 28.5 V peak voltage for a 4 : 1 VSWR, which requires stacked NFETs with breakdown voltage of 3.3 V in the GSM transmit paths to prevent transistors in the off-state from turning on, which greatly degrades signal linearity.

As shown in Fig. 2, we provide an improved series-shunt configuration by adding a big DC bias resistor and leakage preventing PFET in the schematic to optimize the overall performance of the RF switch. These stacked FETs are used to handle the GSM transmit mode high voltage swing and increase the power handling capability. The gate resistors ($R1$–$R10$) are used to improve the linearity of the RF switch while the body resistors are used to improve insertion loss by blocking the current leakage to the ground[7, 8]. The resistors between the source and drain for each stacking transistor are used for voltage division, evenly distributing the transmit above calculated high voltage. The PFET across the gate and body of each NFET is for self-bias to simplify bias design. If the NFET is turned on, then PFET will be turned off and the NFET body will be connected to ground through VB1/VB2; the floating body can offer super-high impedance to minimize IL. If the NFET is turned off and under a negative gate voltage (–2 V), the PFET will be turned on to ensure that the body is close to the negative gate, preventing the RF signal from leaking. Therefore,

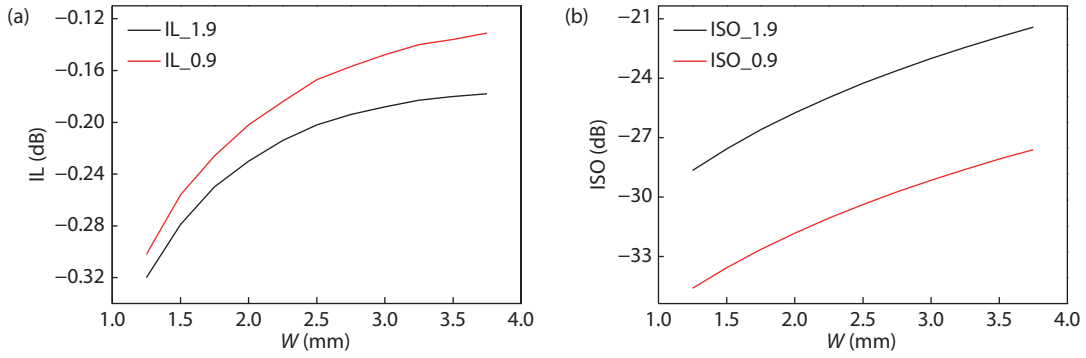

Fig. 3. (Color online) (a) Simulated IL for varying widths of NFETs at 0.9 and 1.9 GHz. (b) Simulated ISO for varying widths of NFETs at 0.9 and 1.9 GHz.

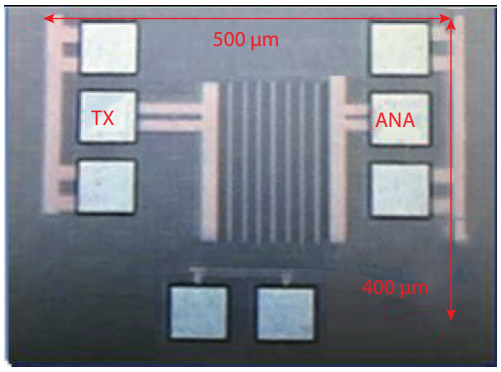

Fig. 4. (Color online) Photomicrograph of RF switch chip.

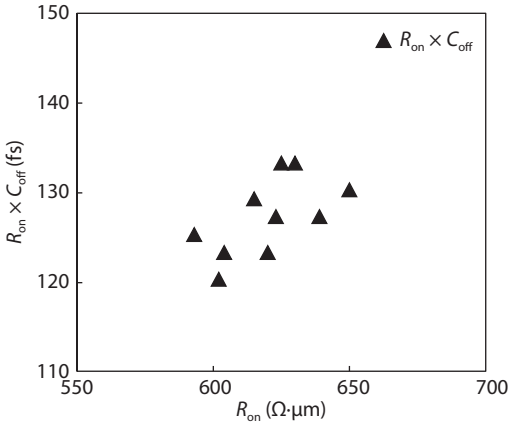

Fig. 5. Measured $R_{on} \times C_{off}$ for RF switch.

when an RF signal goes through the switch, the series NFETs (M1–M10) are turned on, which means that the switch is in the closed state and the RF signal can be transmitted or received with low insertion loss. Meanwhile, the shunt NFETs (M21–M30) are turned on in order to increase isolation and ensure the RF switch is totally open without any current leakage ensuring high isolation.

The optimized insertion loss and isolation of the RF switch should be balanced by selecting the best NFET transistor width. In Figs. 3(a) and 3(b), simulation results are given as the NFET width increases from 1.25 to 3.75 mm. Considering that large transistor width will increase parasitic capacitance and the reduction in insertion loss tends to be less, a 2.5 mm transistor width is selected. A typical value for the gate bias resistance is 50 kΩ. Fig. 4 shows a photomicrograph of the chip with a size of 0.4 × 0.5 mm^2, including testing RF GSG pads.

4. Measurement and discussion

The designed RF switch chip is tested by using a network analyzer through the *S*-parameter for both insertion loss and isolation. The product of R_{on} and C_{off} is actually one of the key merits of the RF switch and a low FoM (120 fs) is given in Fig. 5.

Insertion loss and isolation are measured using an Agilent N9020A Network Analyzer, while $P_{0.1\,dB}$ and harmonics are measured using an Agilent E4440A PSA Series Spectrum Analyzer. For insertion loss of this RF switch, the measurement bias voltages VB1 and V1 are 0, 2.5 V while VB2 and V2 are −2 V. As shown in Fig. 6, the RF switch exhibits low insertion loss of 0.24/0.34 dB and isolation (Fig. 7) takes on higher values of 28.8/22.4 dB at frequency bands of 0.9/1.9 GHz, respectively. The linearity of the RF switch is analyzed by $P_{0.1\,dB}$ and harmonic measurements. The $P_{0.1\,dB}$ (Fig. 8) is well beyond 36 dBm, meeting the GSM 900 standard, which dictates that the maximum available power at the antenna should be at least 33 dBm. The 2nd and 3rd harmonics were measured when a body is biased at 0 V and the gate is biased at 2.5 V. Fig. 9 shows another metric of linearity, the 2nd and 3rd order harmonics are lower than −41 at 34 dBm input power.

Table 1 compares several key parameters with the relevant state-of-the-art RF switches reported. The performance of this SPST RF switch is comparable to that of the RF switch designed in HR SOI[9], which has more expensive substrate and SiGe BiCMOS[11], CMOS technology[12]. Compared with SP10T designed in 0.18 μm SOI[7] and SP6T with 0.13 μm SOI[10], this switch has a lower IL in the case of equal $P_{0.1\,dB}$. All of linearity, $R_{on} \times C_{off}$, insertion loss, and isolation are considered to achieve good overall performance in the SPST switch. These performances can fully meet the requirements of the present mobile phone RF FEM system for multi-mode and multi-frequency applications.

5. Conclusions

A high-performance RF switch with ultra-low insertion loss, high isolation, and linearity is achieved through 0.13 μm RF SOI. The inherent advantages of the SOI process combined with the optimization of the circuit structure significantly improve the performance of the RF switch. Results show a good performance for the SPST RF switch which is used in 4G and 5G mobile phone FEMs and can be used widely in forthcoming 5G technology.

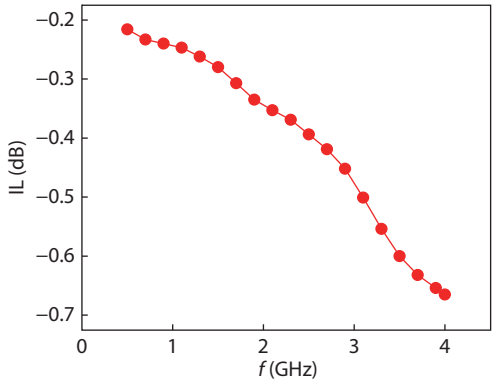

Fig. 6. (Color online) Measured IL for RF switch.

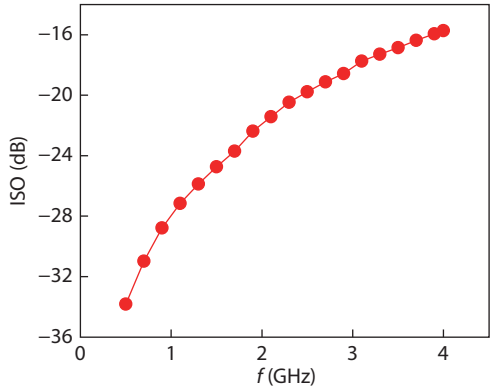

Fig. 7. (Color online) Measured ISO for RF switch.

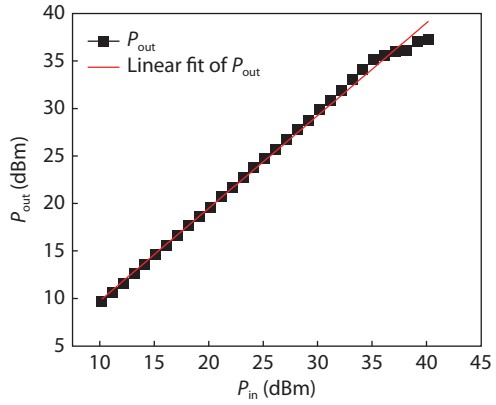

Fig. 8. (Color online) Measured $P_{0.1\,dB}$ for RF switch.

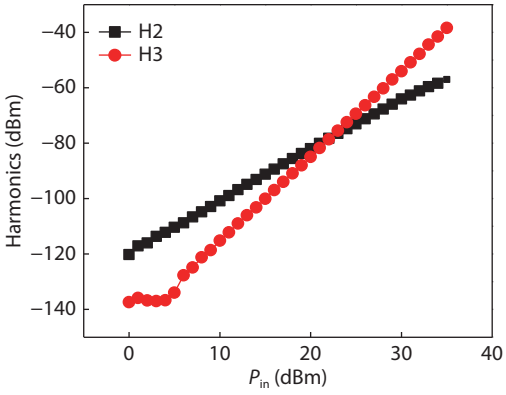

Fig. 9. (Color online) Measured harmonics for RF switch.

Table 1. Comparison of RF switch performance.

Reference	[7]	[9]	[10]	[11]	[12]	This work
RF switch	SP10T	SPDT	SP6T	PNP SPST	SPST	SPST
Freq (GHz)	0.9/1.9	1	0.9/1.9	1	2.55	0.9/1.9
IL (dB)	0.48/0.81	0.4	0.7/0.7	1.6	1.8	0.24/0.34
ISO (dB)	43.1/40	40	40/30	36	41	28.8/22.4
$P_{0.1\,dB}$ (dB)	36	—	36	—	23.2($P_{1\,dB}$)	36
Technology	0.18 μm SOI	HR SOI	0.13 μm SOI	0.25 μm SiGe BiCMOS	65 nm CMOS	0.13 μm SOI

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