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EXCITON-POLARITONS

Perovskite exciton-polaritons

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Microcavity exciton-polariton is a Bosonic quasi-particle of half-matter and half-light formed by strong coupling between semiconductor exciton and microcavity photon. With effective mass 10^4 times lower than electrons, the exciton-polariton provide opportunities for realizing all-solid-state Bose-Einstein condensation (BEC) and superfluities at room temperature and generating a variety of novel excitonic and quantum devices, such as ultra-low threshold polariton lasing, entangling light sources and slowing light devices, *etc.* However, till now owing to the low intrinsic oscillation strength, the exciton-polaritons of inorganic semiconductor are mainly either operated under low temperature, or in ultraviolet regime. On the other hand, the exciton-polariton condensation of organic semiconductor is still challenging because of weak nonlinearity. These extensively hinder the development of exciton-polariton devices.

Qing Zhang and her co-workers demonstrated surface plasmon enhanced strong exciton-polariton effect in hybrid inorganic–organic perovskite nanowire Fabry-Pérot microcavities operated under room temperature. Their spectroscopic study shows that the local oscillation density is effectively redistributed and enhanced in semiconductor–insulator–metal (MIS, $CH_3NH_3PbBr_3$ nanowire–SiO_2–Ag) structure. The Rabi splitting energy reaches up to 564 meV at ~520 nm. The coupling strength is almost twice as much as reported in the other semiconductor nanowires of the same emission color. Their study shows that the perovskite would open new avenues to enrich the fundaments and applications of exciton-polaritons.

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PEROVSKITE LIGHTING

Warm white light emission

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Materials with efficient and stable white light emission are indispensable for solid-state lighting and display applications. It is still a great challenge to achieve broadband emission covering the entire visible wavelength range by using a single material up to date. To this end, it is urgent to explore new environment-friendly single materials with high efficient and stable white light emission for commercial lighting applications to reduce the cost and complexity of devices.

Recently, researchers from Huazhong University of Science and Technology and The University of Toledo demonstrated the high efficient and stable warm white light emission in lead-free all-inorganic double perovskite Cs_2AgInC_{l6}. The white light emission is believed to be from the self-trapped excitons due to the Jahn–Teller distortion of the $AgCl_6$ octahedron in the excited states induced by the strong electron–phonon coupling. Impressively, by intentionally incorporating the Na element to form alloyed $Cs_2(Ag_{0.60}Na_{0.40})InCl_6$ with the trace amount of Bi doping, the photoluminescence quantum efficiency can achieve as high as 86 ± 5% with an excellent stability over 1000 hours in air under continuous heating at 150 °C. Those studies would shed light on exploring new lead-free perovskite materials for high efficiency white light devices and stimulate more research on single-emitter-based white-light-emitting phosphors and diodes.

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SEMICONDUCTOR LASERS

High performance terahertz laser

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For any laser, high power, good beam quality, and broad electrical frequency tuning range are deemed as the key assets to possess for various applications. Terahertz (THz) quantum cascade laser is no exception. Since its invention in 2001, extensive effort has been devoted to optimizing the laser performance, yet with little success in improving these major aspects on a laser chip simultaneously.

Recently, A group led by Qing Hu in MIT has made a major leap with a phase locking approach and achieved these three key performance goals at once. Inspired by the chemistry of hybridization, they can phase lock multiple THz wire lasers by π coupling design. By properly adjusting spacing of adjacent laser element, the laser array can be designed to operate in a coherent symmetric supermode—all collectively radiating in a phase-locked scheme. The demonstrated device exhibits a good level of output power up to 90 mW at continuous-wave operation, and a tight beam pattern of 10° divergence, and a continuous electrical tuning of ~10 GHz at ~3.8 THz. Achieving all three performance metrics means less noise and higher resolution, for more reliable and cost-effective gas sensing, chemical detection, and medical imaging.

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LOW POWER CIRCUIT

Subthreshold analog techniques

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Low power is a fundamental requirement in state-of-the-art IC designs, where lower and scalable supply voltages

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are demanded due to the power benefits of digital circuits under near- and sub-threshold supply voltages. The ultra-low voltage design is also driven by technology scaling as well as leakage and reliability considerations. While analog circuits with weak-inversion transistors benefit from high g_m/I_D due to the exponential characteristics of the V_{GS} versus I_D curve in weak inversion, the shrunk voltage headroom and signal swing limit signal-to-noise ratio fundamentally, and the linearity of transconductance becomes worse. In addition, the decreased intrinsic gain of downscaled planar transistors makes it difficult to build high gain analog blocks. It is thus very challenging to design high-linearity and high-precision analog circuits under near- and sub-threshold supply voltages, where operational transconductance amplifiers are fundamental. Though several approaches have been proposed to replace OTAs in particular analog systems by, e.g., time-domain circuits, dynamic amplifiers, ring amplifiers, zero-crossing based circuits, etc., OTAs remain indispensable due to their linear operation in closed-loop systems.

The team of researchers from University of Electronic Science and Technology of China presented an evolution process of implementing conventional structures with inverters, allowing ultra-low voltage operation with increased flexibility in adopting traditional circuit techniques. Based on the proposed inverter-based elementary structure and CMFB, both the Miller-compensated (MC) OTA and the feedforward-compensated (FFC) OTA achieved significantly improved performance as compared to previous works. The proposed amplifier techniques were verified in ΔΣ modulator (DSM) design, with MC-OTA for a DT-DSM and FFC-OTA for a CT-DSM, both fabricated in a 0.13 μm CMOS. The 0.3 V DT-DSM achieved 74.1 dB SNDR, 83.4 dB SFDR and 20 kHz bandwidth with 79.3 μW power, resulting in a Schreier FoM of 158 dB. The 0.3 V CT-DSM achieved 68.5 dB SNDR, 82.6 dB SFDR and 50 kHz bandwidth with 26.3 μW power, leading to a Schreier FoM of 161 dB. Both DSMs exhibit highly competitive performance among sub-0.5 V designs, validating the proposed subthreshold amplifier techniques.

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HIGH POWER-EFFICIENT SoC CHIP

A 130-nm ferroelectric nonvolatile system-on-chip for internet of things

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Nonvolatile processor (NVP) is promising for energy-harvesting-powered internet-of-things (IoT) devices, owing to its unique capability to sustain computation progress over power outages. Recently, NVPs with different nonvolatile memory technologies have been reported, and significant efforts have been made to improve the on/off switching speed and to minimize the power consumption caused by data backup and restore operations. However, a little attention has been devoted to improve the system-level performance when the NVP works in a real-world transient computing system. As a result, the widespread application of NVP faces challenges such as low level of integration and large peripheral restore overheads.

The nonvolatile system-on-chip (NVSoC) presented by Yongpan Liu (Corresponding author, Department of Electronic Engineering, Tsinghua University, Beijing, China), *et al.* opens the possibility to make transiently-powered IoT devices fast, power-efficient and compact. An on-chip power management subsystem is proposed to minimize the requirement of off-chip components while supporting versatile power policies. And a direct peripheral restore architecture is designed, enabling fast and parallel re-configuration of peripheral devices. A test chip is fabricated in 130-nm ferroelectric-CMOS process, showing more than 6x higher data throughput than previous NVPs.

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BEYOND-CMOS DEVICES

Magnetoelectric spin–orbit logic

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In the last decade, transistor scaling has been enabled by direct improvements to the carrier transport and superior electrostatic control. Despite the successful scaling in the size of transistors, voltage and frequency scaling have slowed. In response, a considerable effort to invent, demonstrate and benchmark beyond-CMOS devices got underway.

Now, a scalable beyond-CMOS spintronic logic device is proposed by Sasikanth Manipatruni and co-workers from Intel Corporation, University of California, Berkeley and Lawrence Berkeley National Laboratory. The beyond-CMOS logic device, also called magnetoelectric spin–orbit (MESO) device, comprises two technologically scalable transduction mechanisms: ferroelectric/magnetoelectric switching and topological conversion of spin to charge. The device interfaces with electrical interconnects and is therefore charge-/voltage-driven and produces a charge/voltage output. It comprises a magnetoelectric switching capacitor, a ferromagnet and a spin-to-charge conversion module. When the input interconnect carries a current, an electric field is set up in the magnetoelectric capacitor. The resulting magnetoelectricity switches the ferromagnet in the determined direction. When a supply current is injected into the device, causing a flow of spin-polarized electrons from the ferromagnet into the spin–orbit-coupling (SOC) mater-

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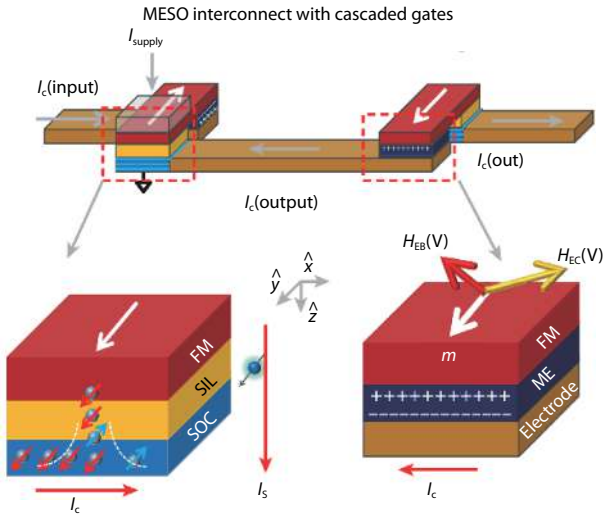

Fig. 1. MESO interconnect with cascaded gates.

ials. Owing to SOC spin-to-charge transduction, a charge current is generated at the output. Hence, the input charge state is inverted by the MESO logic gate at the output. Magnetoelectric/ferroelectric switching is regarded as the most energy-efficient mechanism at room temperature that scales to lateral dimensions of 10 nm and retains a stable collective order parameter. The intrinsic switching energy for ferroelectric/magnetoelectric switching can approach 1 aJ/bit, which is around 30 times lower than the switching energy of advanced CMOS devices. For spin-to-charge conversion using inverse SOC, the efficiency improves with reducing the width of the magnet, which is a highly desirable scaling feature. In view of distinct advantages of superior switching energy, low switching voltage, and enhanced logic density, MESO logic may enable entirely new computer architectures that may avoid the trade-offs of the Turing and von Neumann architectures and of Amdahl's law.

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