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A compact two-dimensional analytical model of the electrical characteristics of a triple-material double-gate tunneling FET structure

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Abstract: This paper presents a compact two-dimensional analytical device model of surface potential, in addition to electric field of triple-material double-gate (TMDG) tunnel FET. The TMDG TFET device model is developed using a parabolic approximation method in the channel depletion space and a boundary state of affairs across the drain and source. The TMDG TFET device is used to analyze the electrical performance of the TMDG structure in terms of changes in potential voltage, lateral and vertical electric field. Because the TMDG TFET has a simple compact structure, the surface potential is computationally efficient and, therefore, may be utilized to analyze and characterize the gate-controlled devices. Furthermore, using Kane's model, the current across the drain can be modeled. The graph results achieved from this device model are close to the data collected from the technology computer aided design (TCAD) simulation.

Key words: triple-material double-gate TFET; surface potential; lateral and vertical electric field; drain current; TCAD simulation

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1. Introduction

Over the past few decades, the performance of metal–oxide–semiconductor field-effect transistors (MOSFETs) has greatly improved thanks to their incessant and aggressive scaling. CMOS transistors scaling exhibits several short channel effects (SCEs). The short channel effects in MOSFETs are drain induced barrier lowering (DIBL), high leakage currents during OFF-state, high subthreshold slope (SS) and others. These effects lead to greater static power consumption and evil switching characteristics. Hence, substitute, innovative devices are introduced, among which tunneling field-effect transistor (TFET) is a promising candidate[1–4]. TFET operates based on BT-BT process where electrons tunnel from valance band states to the conduction band state of the channel. Therefore, carriers with high energy are filtered out through the semiconductor bandgap, so its subthreshold slope TFET is < 60 mV/decade, though semiconductor bandgap carriers with higher energy levels are filtered out[5]. The output characteristic of TFET shows a delayed saturation. Therefore, TFETs should be designed carefully. The utility of TFET device is severely limited by the strong drain induced barrier lowering (DIBL)[6].

Numerous analytical models are carried out in the literature[7–15]. Many one-dimensional analytical models assume a constant electric field over the source channel junction to derive the current[7–10]. Many two-dimensional analytical models are based on TFET to calculate the tunneling generation rate using a two-dimensional Poisson's equation, while the tunneling current has been computed by using surface potential equations[11–13]. A number of analytical models were proposed for SMGTFET[7–19]. Many TFET with DM gates have been proposed, in which the OFF-state current is reduced due to minimum surface potential and adverse lateral electric field across the channel[20–28]. A TFET with triple material was proposed in which TFET will tunnel carriers from source side to drain side in two directions due to shift of the tunneling junction. Analytical modeling of TMGTFET is very complex to analyze[26]. However, precise analytical models for TMGTFET are required. Thus, the main objective of this paper is to develop an analytical model for TMDGTFET by using a parabolic approximation approach. Using two-dimensional Poisson's equations, we model surface potential, lateral and vertical electric field and drain current in simpler equations. The analytical model developed in this paper is useful for prognostic compact modeling of TMDGTFET, which includes analysis of the device physics. Section 2 explains the device parameters and structure, with three metal work function. The two-dimensional analytical model for TMDGTFET is derived using a two-dimensional Poisson's equation for the various parameters in Section 3. Meanwhile, Section 4 includes the result and discussion with simulation graphs. Finally, the model is concluded in Section 5.

2. Device parameters and structure

The schematic of a triple-material double-gate tunneling FET shown in Fig. 1, where M1, M2 and M3 are three different metals having different work function: Cobalt(ϕ_{m1} = 5 eV), Iron(ϕ_{m2} = 4.7 eV) and Chromium(ϕ_{m3} = 4.5 eV) in the channel region. Both the back and front gates consists of three metals, with each channel length having L_1, L_2 and L_3. The drain is n-type doped, the source is p-type doped, and the channel section is lightly doped with n-type. The effect of oxide charges is neglected because the channel is uniformly doped. t_{si} and t_{ox} are the thickness of channel and the oxide.

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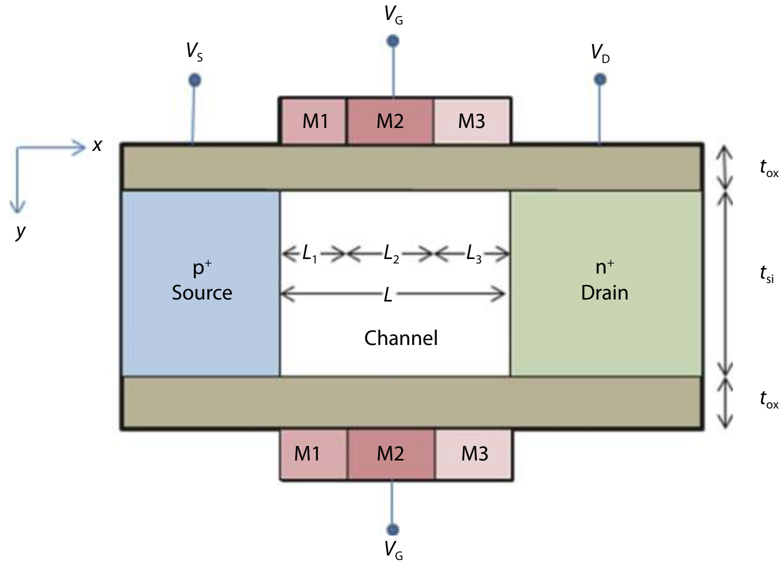

Fig. 1. (Color online) Schematic diagram of triple metal double-gate TFET (n-type).

The OFF-state current is quite low due to reduced work function ϕ_m and on source side there is no band overlap. The probability of tunneling of carriers on the source side increases because the band overlap increases as the tunneling width decreases. Hence, electrons tunnel from valence band to the conduction band of source in the intrinsic body and they then drift to drain by a process of drift diffusion. If there is an increase in ϕ_m, then the band diagram in ON-state does not change.

3. Analytical model

3.1. Surface potential

The potential distribution in the oxide region of the gate is distinguished by using a two-dimensional Poisson's equation:

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = 0. \quad (1)$$

The parabolic approximation approach is employed to resolve the two-dimensional Poisson's equation for TMDG TFET. The parabolic method is used to calculate the potential distribution over the two-dimensional space (along device depth and device length) and an equation for the potential is given as follows

$$\phi(x,y) = C_0(x) + C_1(x)y + C_2(x)y^2. \quad (2)$$

$C_0(x)$, $C_1(x)$ and $C_2(x)$ are arbitrary constants, each constant is functions of x. Since the gate consists of three materials, the potential under each material M1, M2 and M3 are given in Eqs. (3)–(5), respectively

$$\phi_1(x,y) = C_{10}(x) + C_{11}(x)y + C_{12}(x)y^2, \quad 0 \leqslant x \leqslant L_1, \quad (3)$$

$$\phi_2(x,y) = C_{20}(x) + C_{21}(x)y + C_{22}(x)y^2, \quad L_1 \leqslant x \leqslant L_1 + L_2, \quad (4)$$

$$\phi_3(x,y) = C_{30}(x) + C_{31}(x)y + C_{32}(x)y^2, \quad L_1 + L_2 \leqslant x \leqslant L_1 + L_2 + L_3. \quad (5)$$

The boundary conditions required for the solution of Poisson's equation are as follows.

3.1.1. At the front-oxide gate interface, the electric flux is continuous in TMDG TFET, as given in Eqs. (6)–(8)

$$\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}x} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s1}(x) - \psi_{g1}}{t_{ox}}, \text{under material M1 at } y = 0, \quad (6)$$

$$\frac{\mathrm{d}\phi_2(x,y)}{\mathrm{d}x} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s2}(x) - \psi_{g2}}{t_{ox}}, \text{under material M2 at } y = 0, \quad (7)$$

$$\frac{\mathrm{d}\phi_3(x,y)}{\mathrm{d}x} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s3}(x) - \psi_{g_3}}{t_{ox}}, \text{unde material M3 at } y = 0. \quad (8)$$

3.1.2. At the back gate-oxide and the back channel interface the electric flux is continuous in three materials and it is given in Eqs. (9)–(11) as follows

$$\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}x} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_{g1} - \phi_{s1}(x)}{t_{ox}}, \text{under material M1 at } y = t_{si}, \quad (9)$$

$$\frac{\mathrm{d}\phi_2(x,y)}{\mathrm{d}x} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_{g2} - \phi_{s2}(x)}{t_{ox}}, \text{under material M2 at } y = t_{si}, \quad (10)$$

$$\frac{\mathrm{d}\phi_3(x,y)}{\mathrm{d}x} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_{g3} - \phi_{s3}(x)}{t_{ox}}, \text{under material M3 at } y = t_{si}. \quad (11)$$

By applying the above boundary condition from Eq. (6) to Eq. (11) we obtain

$$C_{10} = \phi_{s1}(x), \quad (12)$$

$$C_{11} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left[\frac{\phi_{si} - \psi_{g1}}{t_{ox}}\right], \tag{13}$$

$$C_{12} = -\frac{1}{t_{si}}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left[\frac{\phi_{si} - \psi_{g1}}{t_{ox}}\right], \tag{14}$$

$$C_{20} = \phi_{s2}(x), \tag{15}$$

$$C_{21} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left[\frac{\phi_{si} - \psi_{g2}}{t_{ox}}\right], \tag{16}$$

$$C_{22} = -\frac{1}{t_{si}}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left[\frac{\phi_{si} - \psi_{g2}}{t_{ox}}\right], \tag{17}$$

$$C_{30} = \phi_{s3}(x), \tag{18}$$

$$C_{31} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left[\frac{\phi_{si} - \psi_{g3}}{t_{ox}}\right], \tag{19}$$

$$C_{32} = -\frac{1}{t_{si}}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left[\frac{\phi_{si} - \psi_{g3}}{t_{ox}}\right]. \tag{20}$$

3.1.3. The potential equations across source end and drain end are as follows

$$\phi_{s1}(0, 0) = V_{bi}, \tag{21}$$

$$\phi_{s1}(L_1, 0) = \phi_{s2}(L_1, 0), \tag{22}$$

$$\frac{\partial\phi_{s1}}{\partial x} = \frac{\partial\phi_{s2}}{\partial x}, \quad \text{when } x = L_1, \tag{23}$$

$$\phi_{s2}(L_1 + L_2, 0) = \phi_{s3}(L_1 + L_2, 0), \tag{24}$$

$$\frac{\partial\phi_{s2}}{\partial x} = \frac{\partial\phi_{s3}}{\partial x}, \quad \text{when } x = L_1 + L_2, \tag{25}$$

$$\phi_{s3}(L_1 + L_2 + L_3, 0) = V_{bi} + V_{DS}. \tag{26}$$

By applying these boundary conditions, the calculated surface potential $\phi_{s1}(x)$, $\phi_{s2}(x)$ and $\phi_{s3}(x)$ is given in Eqs. (21)–(26)

$$\phi_{s1}(x) = Ae^{\lambda x} + Be^{-\lambda x} + \psi_{g1}, \ 0 \leqslant x \leqslant L_1, \tag{27}$$

$$\phi_{s2}(x) = Ce^{\lambda(x-L_1)} + De^{-\lambda(x-L_1)} + \psi_{g2}, \quad L_1 \leqslant x \leqslant L_1 + L_2, \tag{28}$$

$$\phi_{s3}(x) = Ee^{\lambda(x-L_1-L_2)} + Fe^{-\lambda(x-L_1-L_2)} + \psi_{g3}, \\ L_1 + L_2 \leqslant x \leqslant L_1 + L_2 + L_3, \tag{29}$$

where

$$\lambda = \sqrt{\frac{2\varepsilon_{ox}}{\varepsilon_{si}t_{ox}t_{si}}}$$

$$\psi_{g1} = V_{gs} - \phi_{m1} + \chi + E_g/2$$

$$\psi_{g2} = V_{gs} - \phi_{m2} + \chi + E_g/2$$

$$\psi_{g3} = V_{gs} - \phi_{m3} + \chi + E_g/2$$

E_g is the energy bandgap, V_{gs} is the gate voltage, q is elementary charge, V_{DS} is the drain to source voltage, V_{bi} is the built in potential, ε_{si} and ε_{ox} is the relative permittivity of silicon and silicon dioxide, L is channel length, χ is electron affinity and ϕ_m is work function of metal. Solving the Eqs. (27)–(29) we obtain A, B, C, D, E and F.

$$A = \frac{(V_{bi} - \psi_{g1})e^{-\lambda(L_1+L_2+L_3)} - (V_{bi} + V_{DS} - \psi_{g3}) + (\psi_{g1} - \psi_{g2})\cosh\lambda(L_2 + L_3) + (\psi_{g2} - \psi_{g3})\cosh\lambda L_3}{e^{-\lambda(L_1+L_2+L_3)} - e^{\lambda(L_1+L_2+L_3)}} \tag{30}$$

$$B = \frac{(V_{bi} + V_{DS} - \psi_{g3}) - (V_{bi} - \psi_{g1})e^{\lambda(L_1+L_2+L_3)} - (\psi_{g1} - \psi_{g2})\cosh\lambda(L_2 + L_3) - (\psi_{g2} - \psi_{g3})\cosh\lambda L_3}{e^{-\lambda(L_1+L_2+L_3)} - e^{\lambda(L_1+L_2+L_3)}} \tag{31}$$

$$C = Ae^{\lambda L_1} + \frac{\psi_{g1} - \psi_{g2}}{2}, \tag{32}$$

$$D = Be^{-\lambda L_1} + \frac{\psi_{g1} - \psi_{g2}}{2}, \tag{33}$$

$$E = Ce^{\lambda L_{21}} + \frac{\psi_{g2} - \psi_{g3}}{2}, \tag{34}$$

$$F = De^{\lambda L_2} + \frac{\psi_{g2} - \psi_{g3}}{2}, \tag{35}$$

3.2. Electric field

The lateral electric field E_x and vertical electric field E_y are found by deriving potential with respect to x and y, respectively. The lateral electric field is given in Eqs. (36)–(38) as

$$E_{1x}(x) = -\frac{d\phi_{s1}(x)}{dx} = -A\lambda e^{\lambda x} + B\lambda e^{-\lambda x}, \quad 0 \leqslant x \leqslant L_1 \tag{36}$$

$$E_{2x}(x) = -\frac{d\phi_{s2}(x)}{dx} = -C\lambda e^{\lambda(x-L_1)} + D\lambda e^{-\lambda(x-L_1)}, \\ L_1 \leqslant x \leqslant L_1 + L_2, \tag{37}$$

$$E_{3x}(x) = -\frac{d\phi_{s3}(x)}{dx} = -E\lambda e^{\lambda(x-L_1-L_2)} + F\lambda e^{-\lambda(x-L_1-L_2)}, \\ L_1 + L_2 \leqslant x \leqslant L_1 + L_2 + L_3. \tag{38}$$

The vertical electric field is given in Eqs. (39)–(41) as

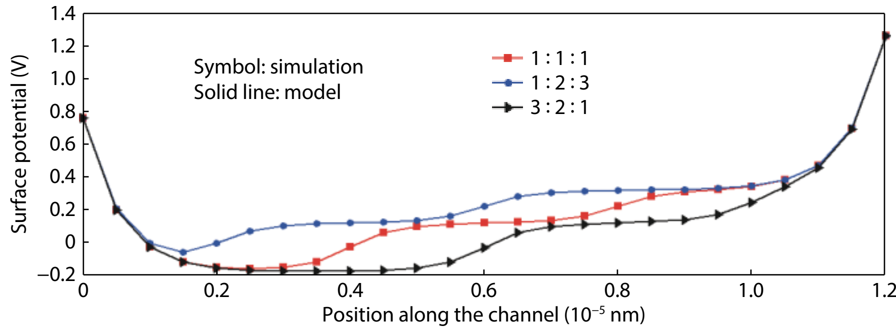

Fig. 2. (Color online) Surface potential variation along the position of channel from the p-type doped source to n-type doped drain with different $L_1 : L_2 : L_3$ ratio for $V_{GS} = 0.25$ V, $V_{DS} = 0.5$ V, and $t_{ox} = 2$ nm.

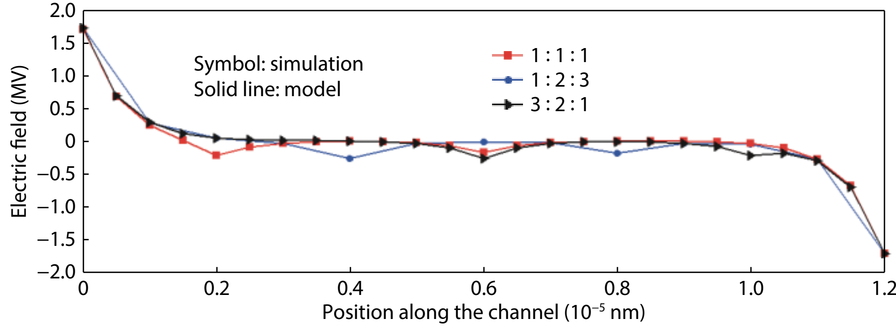

Fig. 3. (Color online) Lateral electric field along the position of channel from the p- type doped source to the n- type doped drain with different $L_1 : L_2 : L_3$ ratio for $V_{GS} = 0.25$ V, $V_{DS} = 0.5$ V, and $t_{ox} = 2$ nm.

$$E_{1y}(x) = -\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}y} = -C_{11}(x) - 2yC_{12}, \quad 0 \leqslant x \leqslant L_1, \tag{39}$$

$$E_{2y}(x) = -\frac{\mathrm{d}\phi_2(x,y)}{\mathrm{d}y} = -C_{21}(x) - 2yC_{22}, \quad L_1 \leqslant x \leqslant L_1 + L_2, \tag{40}$$

$$E_{3y}(x) = -\frac{\mathrm{d}\phi_3(x,y)}{\mathrm{d}y} = -C_{31}(x) - 2yC_{32}, \quad L_1 + L_2 \leqslant x \leqslant L_1 + L_2 + L_3. \tag{41}$$

3.3. Drain current

The current in TMDG TFET depends on the BTBT of electrons from source valance band to conduction band of channel region, which is given as

$$I_{DS} = q \iint G\mathrm{d}x\mathrm{d}y, \tag{42}$$

where generation rate (G) can be calculated using Kane's model which is given as

$$G(E) = A_1 E^{D_1} \exp\left(-\frac{B_1}{E}\right), \tag{43}$$

where $A_1 = 4 \times 10^{14}$ cm$^{-1/2}$V$^{-5/2}$s^{-1} and $B_1 = 1.9 \times 10^7$ V/cm are the Kane's parameters, E the magnitude of the electric field which is defined as

$$E = \sqrt{E_x + E_y}.$$

4. Results and discussion

Our proposed models are verified using two-dimensional numerical simulation. Fig. 1 gives a cross-sectional view of the proposed model TM-DG TFET, in which both front and back gates are composed of three materials with three various work functions. Fig. 2 provides the plot of surface potential versus position along the channel, for TM-DG TFET with different combinations channel length ratios, such as 1 : 1 : 1, 3 : 2 : 1 and 1 : 2 : 3 for a total channel length; i.e., L = 120 nm, V_{GS} = 0.25, V_{DS} = 0.5 and t_{ox} = 2 nm, respectively. The TM-DG TFET potential graph provides enhanced screening of channel space with respect to the first metal to be depleted from potential variation. The 3 : 2 : 1 device model needs high vitality to provide higher potential boundary as compared with other structures, with an increase in power supply to a substantial threshold voltage. In addition, the movement of carriers is decreased due to substantial potential barrier at the source side. The 1 : 2 : 3 device model outshines because of its enhanced carrier transport effectiveness.

Fig. 3 demonstrates the correlations of lateral electric field across the channel for TM-DG TFET structures for V_{gs} = 0.25, V_{ds} = 0.5 and t_{ox} = 2 nm. The two peaks obtained in the electric field profile of TMDG structure indicate appropriate carrier transport efficiency and an appropriate average electric field along the channel. The extra peak in electric field increases the speed of the carriers in the channel, along these lines guaranteeing a vertical extent gate transport effectiveness to provide more quantities of carriers to drain. In addition, at the drain side a reduced peak of electric field appeared to offer an extra advantage of giving higher resistance to HCEs. Among the different TM-DG structures, TM-DG TFET (1 : 2 : 3) lateral electric field has a peak that is closest to the region of source, consequently guaranteeing a peak in its carrier's speed closest to the source. This brings about the ex-

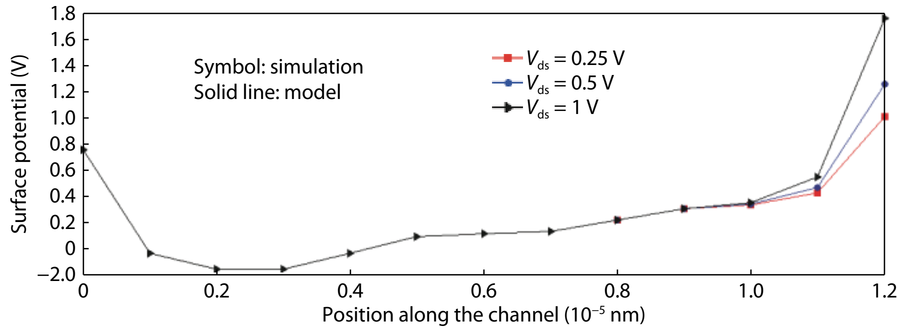

Fig. 4. (Color online) Surface potential across channel length $L = 120$ nm and $V_{GS} = 0.25$ V with different $V_{DS} = 0.25$, 0.5, and 1 V.

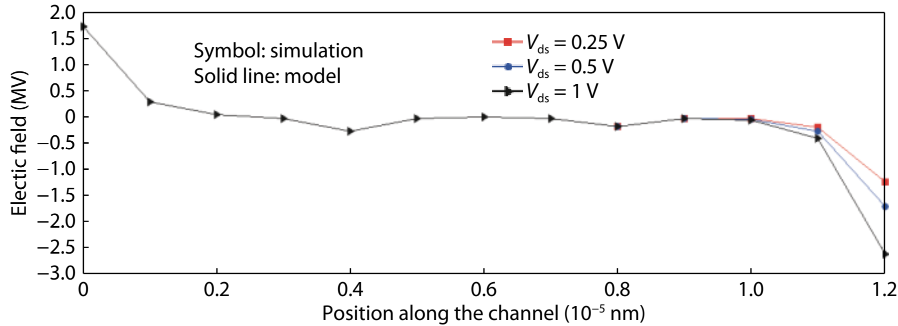

Fig. 5. (Color online) Lateral electric field across the channel length $L = 120$ nm, $V_{GS} = 0.25$ V for different $V_{DS} = 0.25$, 0.5 and 1 V.

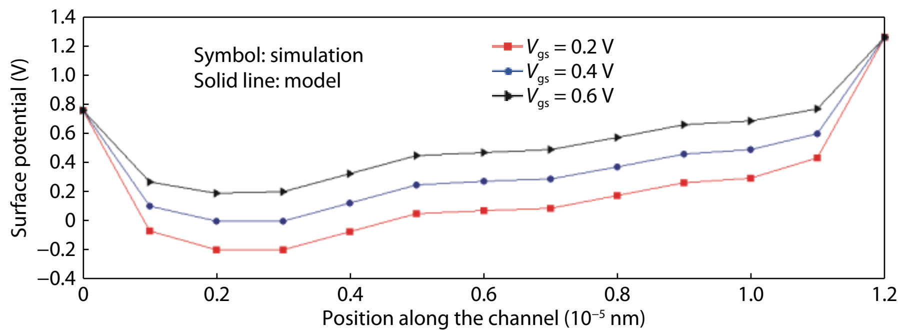

Fig. 6. (Color online) Surface potential along the channel with length $L = 120$ nm and $V_{DS} = 0.5$ V for different $V_{GS} = 0.2$, 0.4, and 0.6 V.

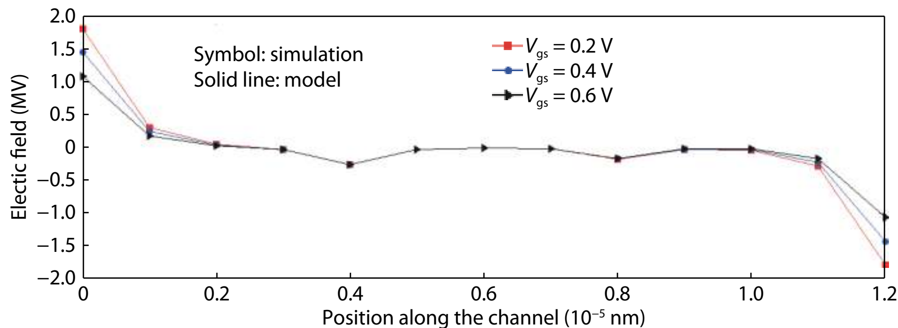

Fig. 7. (Color online) Lateral electric field profile for channel length $L = 120$ nm and $V_{DS} = 0.5$ V for different gate voltages.

treme refinement in the carrier transport effectiveness, influential transconductance, and higher drain current.

Fig. 4 shows surface potential variation versus position across the channel with V_{gs} constant, for different drain to source voltages (V_{ds}). The potential increases only under third metal (M3) and no change under metal M1 and M2, as V_{ds} increases. The lateral electric field variation for different V_{ds} with constant V_{gs} shows a change in the drain side, which is shown in Fig.5. Fig. 6 shows the surface potential variation for different gate to source voltages (V_{gs}), while the V_{ds} constant changes the surface potential throughout the channel. A variation of the lateral electric field along the channel length for different gate to source (V_{gs}) with constant V_{ds} shows that there is a change in both source and drain side, as displayed in Fig. 7. The region under Metal 1 is reduced because the electric field is high at the source channel junction,

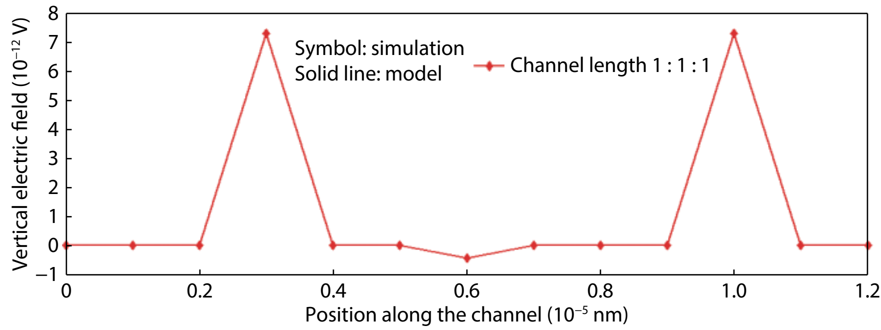

Fig. 8. (Color online) Vertical electric field along the channel for V_{GS} = 0.25 V, V_{DS} = 0.5 V, and t_{ox} = 2 nm.

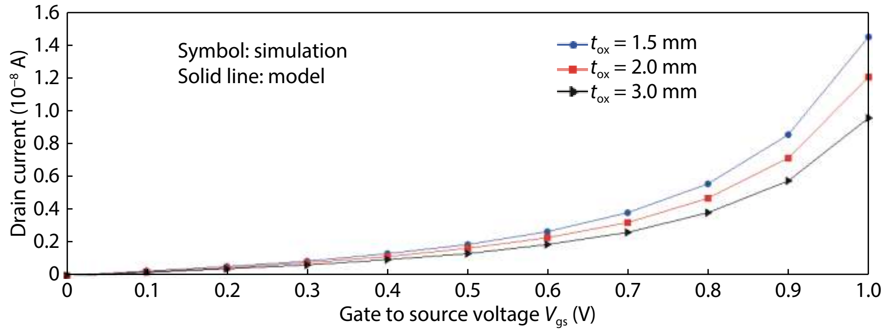

Fig. 9. (Color online) I_d–V_{GS} characteristics on a linear scale for V_{DS} = 0.5 V and t_{si} = 5 nm for different oxide thickness.

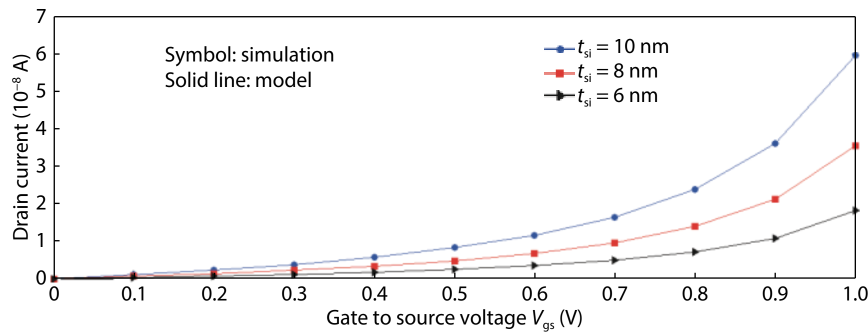

Fig. 10. (Color online) I_d–V_{GS} characteristics on a linear scale for V_{DS} = 0.5 V and t_{ox} = 2 nm for different channel thickness.

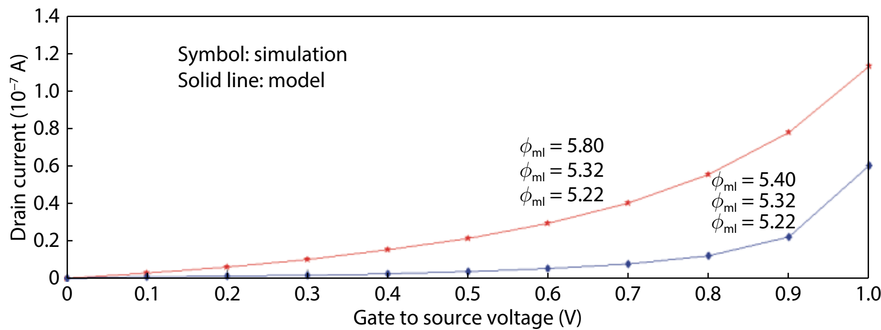

Fig. 11. (Color online) I_d–V_{GS} characteristics on a linear scale for V_{DS} = 0.5 V and for a three different metal work function.

which reduces the tunneling path. Fig. 8 shows the vertical electric field along the channel with V_{GS} = 0.25 V, V_{DS} = 0.5 V, and t_{ox} = 2 nm. The vertical electric field has ae peak when the work function of the metal varies. The first peak is obtained when carriers transfer from M1 to M2 and second peak is obtained from M2 to M3.

The I_d–V_{GS} characteristic for different oxide thickness is shown in Fig. 9. To obtain a high ON–OFF current ratio, Fig. 10 shows variation of I_d–V_{GS} characteristic for different body thicknesses. A reduction in the body thickness helps to increase the current of the TFET, due to which the tunneling path is reduced with an exponential increase in tunneling probability. The I_d–V_{GS} characteristics for different work function combination are shown in Fig. 11. The tunneling current

increases when the work function of M1 increases.

5. Conclusion

This paper proposes analytical modeling of a triple-material double-gate TFET. The tunneling path is modulated by the carriers over the channel due to the different work functions of the metals. The TM-DG TFET provides the better carrier transport efficiency, has higher resistance to HCEs, and obtains a high ON-OFF current ratio. Hence, TFET is strong promising behavior device that can be used in low-power applications.

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