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# Column readout circuit with improved offset mismatch and charge sharing for CMOS image sensor

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**Abstract:** High linearity and low noise column readout chain are two key factors in CMOS image sensor. However, offset mismatch and charge sharing always exist in the conventional column wise readout implementation, even adopting the technology of correlated double sample. A simple column readout circuit with improved offset mismatch and charge sharing for CMOS image sensor is proposed in this paper. Based on the bottom plate sampling and fixed common level method, this novel design can avoid the offset nonuniformity between the two buffers. Also, the single buffer and switched capacitor technique can effectively suppress the charge sharing caused by the varied operating point. The proposed approach is experimentally verified in a 1024 × 1024 prototype chip designed and fabricated in 55 nm low power CMOS process. The measurement results show that the linear range is extended by 20%, the readout noise of bright and dark fields is reduced by 40% and 30% respectively, and the improved photo response nonuniformity is up to 1.16%. Finally, a raw sample image taken by the prototype sensor shows the excellent practical performance.

**Key words:** CMOS image sensor; column readout; buffer; offset mismatch; charge sharing

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## 1. Introduction

Although the charge coupled device (CCD) image sensors have been widely used during the past several decades, complementary metal oxide semiconductor (CMOS) image sensor (CIS) have brought a huge popularity to various imaging applications due to the advantages over CCD image sensor such as system on chip (SOC), low power consumption, and lower cost. The dynamic range and signal-to-noise ratio are two key parameters which determine the performance of an image sensor. In these characteristics, it is obvious to one that the noise parameter is the key technology because the dynamic range is the result of full swing range over the readout noise and the signal-to-noise ratio is the results of signal power over the noise power[1].

To reduce the temporal noise, high gain column amplifier is adopted in the first stage of the column readout chain[2], which is helpful to the low light level, but it will restrict the input light range for the high light level. So, the entire range of light level is not considered in the high gain technology at the same time. An effective approach is to optimize the individual noise of all modules. Offset FPN, low frequency noise and reset noise of pixel can be suppressed through the correlation of reset voltage and integrated signal voltage, which is called correlated double sampling (CDS)[3]. In recent years, high column level gain and correlated multiple sampling (CMS) were implemented to further reduce the input referred temporal noise[4, 5]. Both fixed pattern noise (FPN) and temporal noises are suppressed by the proposed digital correlated multiple sampling (DCMS) technology in Ref. [6]. From the previous reported work, we can see that the temporal noise and the spatial noise are considered and researched through the system. It is realized by sacrificing the swing range and dynamic range. The thoroughgoing approach should be the practical circuit level solution which optimizing the components parameters and the non-ideal effect[7]. So, we are devoted to give the module level solution to reduce the practical level circuit noise. Offset mismatch and charge sharing between the column amplifier and the column buffer are two outstanding problems existed in the column readout circuit. Unfortunately, because the charge sharing is inseparably linked with the charge injection, the image signal is nonlinear. In this paper, simple column readout circuits with improved offset mismatch and charge sharing for CMOS image sensor is proposed. The linear range and the readout noise are improved in a 1024 × 1024 CMOS image sensor chip designed and fabricated in the 55 nm low power CMOS process. The detail description and discussion are organized as following sections.

## 2. Traditional column readout designs

Several CMOS image sensor architectures have been reported according to the types of the signal readout schemes and the position of the analog to digital processing. A typical readout circuit of CMOS image sensor with a noise canceller for fixed pattern noise and reset noise of pixels is shown in Fig. 1. By controlling the timing sequence of switches $S_1$ and $S_2$, the reset level and signal level of the amplified pixel output are sampled on the capacitor $C_1$ and $C_2$ respectively[8]. The equivalent input parasitic capacitor of column buffer 1 and column buffer 2 are $C_{par1}$ and $C_{par2}$. Be-

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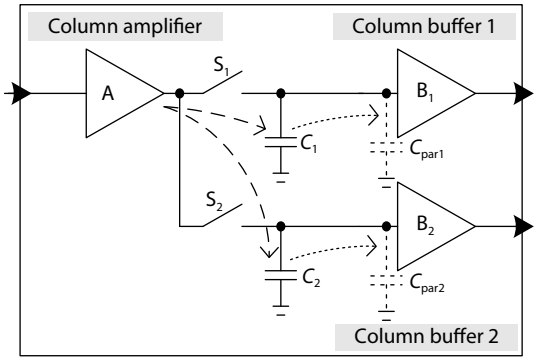


Fig. 1. Column readout with two buffers.

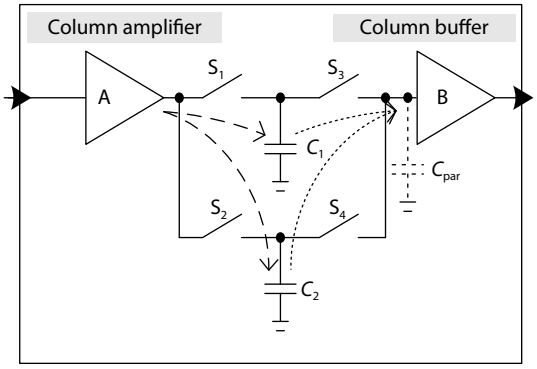


Fig. 2. Column readout with single buffer.

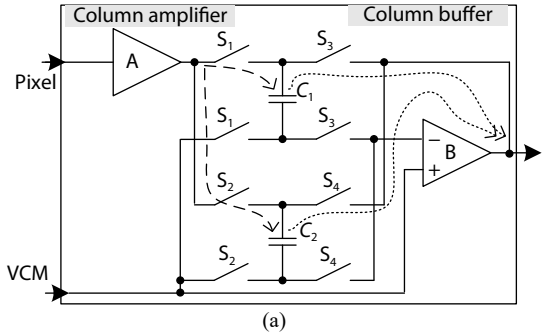


Fig. 3. (a) Proposed column readout. (b) Control timing of the proposed circuit.

cause this parasitic capacitor and storage capacitor are parallel to the column amplifier, it can't induce the nonlinearity of the signal level, except for increasing driving current and settling time. The intrinsic offset due to the mismatch between the column buffer 1 and column buffer 2 is a critical problem. Even though both column buffers use the same circuit, the offset also can't be eliminated by CDS, because the actual signal output can be expressed by Eq. (1), where $V_R$ is the reset level from pixel output, $V_S$ is the image level from pixel output, $V_{OS1}$ is the offset voltage of the buffer 1, and $V_{OS2}$ is the offset voltage of the buffer 2.

$$V_{OUT} = (V_R + V_{OS1}) - (V_S + V_{OS2}) = (V_R - V_S) + (V_{OS1} - V_{OS2}). \quad (1)$$

Therefore, a serial output through single column buffer was designed to overcome the offset, as shown in Fig. 2[9]. Its sample phase is the same as shown in Fig. 1, but the output phase is different because the reset level on capacitor $C_1$ is transmitted through the switch $S_3$ and column buffer, the image level on capacitor $C_2$ is transmitted through the switch $S_4$ and column buffer. However, due to the parasitic capacitor $C_{par}$ in column buffer input, the respective charge sharing during the reset level and image level output phase will produce high noise and nonuniformity. Furthermore, the final balance level is decided not only by the ratio of the storage capacitor and the parasitic capacitor, but also by the initial or the final state. It can be expressed by the following equations:

$$C_1 V_R + C_{par} V_{(L1)} = (C_1 + C_{par}) V_{R(F)}, \quad (2)$$

$$C_2 V_S + C_{par} V_{(L2)} = (C_2 + C_{par}) V_{S(F)}, \quad (3)$$

where $V_{(L1)}$ is the last stage level on the column buffer input $C_{par}$ before switch $S_3$ turns on, $V_{(L2)}$ is the last stage level on the column buffer input $C_{par}$ before switch $S_4$ turns on. So, $V_{(L1)}$ has an approximate storage value of reset level, $V_{(L2)}$ has an approximate storage value of image level during the last row readout. Although there is a correlation between each adjacent row, but for the low noise demanding, the difference will induce enough performance deteriorating owing to the discharge and fixed pattern noise.

## 3. Proposed column readout structures

Based on the analysis of traditional column solution, a low noise column readout circuit with improved charge sharing for CMOS image sensor is proposed in this paper, as shown in Fig. 3(a), and the control timing is shown in Fig. 3(b). The presented approach is composed by the column amplifier, reset level storage capacitor $C_1$, image level storage capacitor $C_2$, a single column buffer and eight switches. In the sample phase, firstly the switch $S_1$ which connect the column amplifier and both plates of capacitor $C_1$ is on, the reset level from pixel column line can be sampled on the capacitor $C_1$, as shown in Fig. 4(a). Then the switch $S_2$ which connect the column amplifier and both plates of capacitor $C_2$ is on, the image level from pixel column line can be sampled on the capacitor $C_2$, as shown in Fig. 4(b). In the buffer phase, firstly the switch $S_3$ which connect both plates of capacitor $C_1$ and the column buffer is on, the reset level sampled on the capacitor $C_1$ can be buffered out to the next stage, as shown in Fig. 4(c). Secondly the switch $S_4$ which connect both plates of capacitor $C_2$ and the column buffer is on, the image level sampled on the capacitor $C_2$ can be buffered out to the next stage, as shown in Fig. 4(d). Since the input operating point is unchanged, it can be seen that this method not only adopts a single column buffer to eliminate the offset, but also improves the charge sharing by the bottom plate sampling.

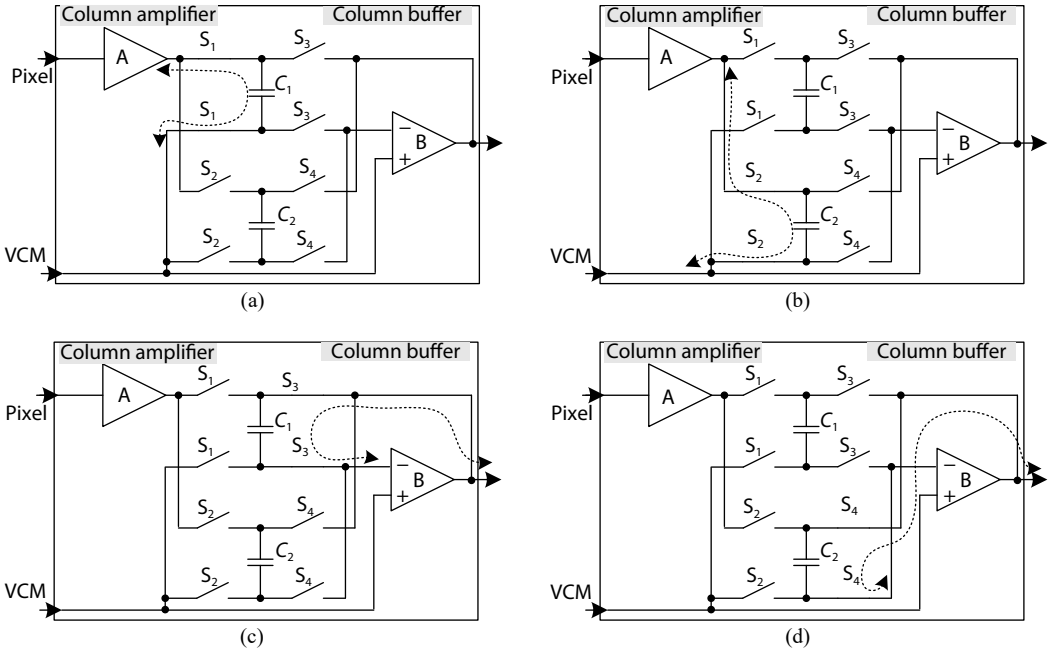


Fig. 4. (a) Reset level sample phase. (b) Image level sample phase. (c) Reset level buffer phase. (d) Image level buffer phase.

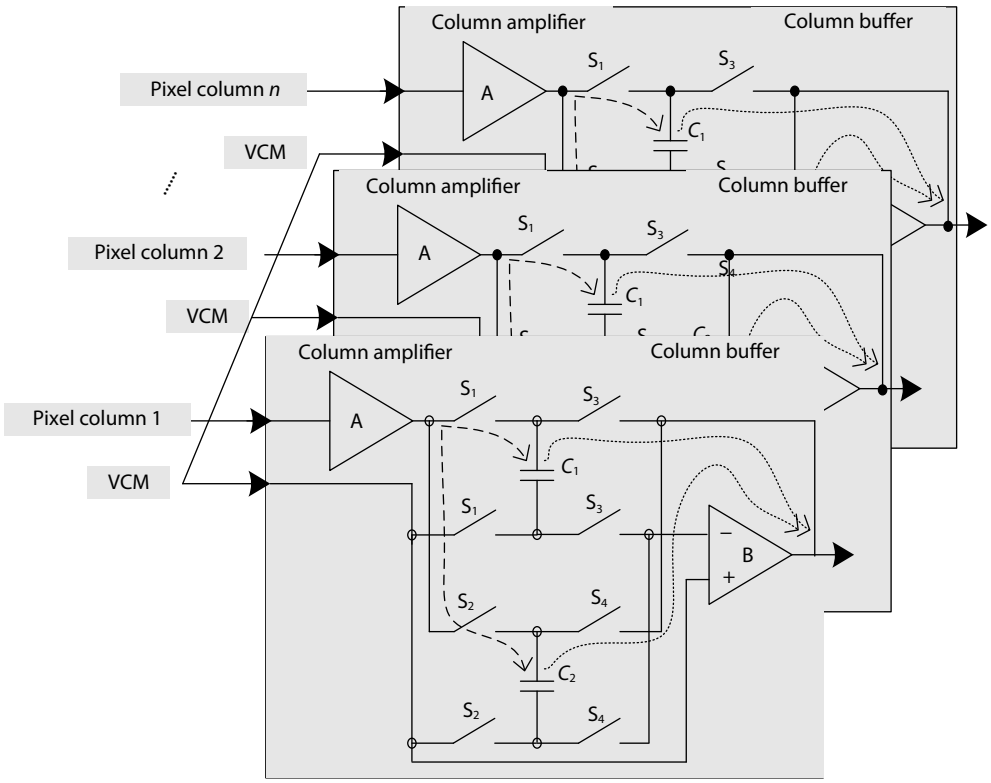


Fig. 5. *n* columns readout schematic.

A large array CMOS image sensor is composed by a great number of column readout circuits. Generally, the sample phase is parallel at same time in a row pixel, and the buffer phase is consecutive to transmit from column 1 to column *n*. *n* column readout circuit adopted proposed approach is designed in Fig. 5, where each column readout has two input ports, one is the pixel output, and another is the common voltage VCM, which is shared to all columns, but with enough driving capability, where the maximum load capacity we designed is 10 mA. The detail control timing is shown in Fig. 6.

## 4. Measurement results

The low noise column readout circuit with improved offset mismatch and charge sharing for CMOS image sensor is implemented in 55 nm CMOS image sensor technology. The die micrograph of the fabricated sensor is shown in Fig. 7, which consists of a 1024 × 1024 pixel array and peripheral circuitry. The column parallel readout circuit is located on a single side below the pixel array. In order to measure the performance of the proposed approach how it improve the off-

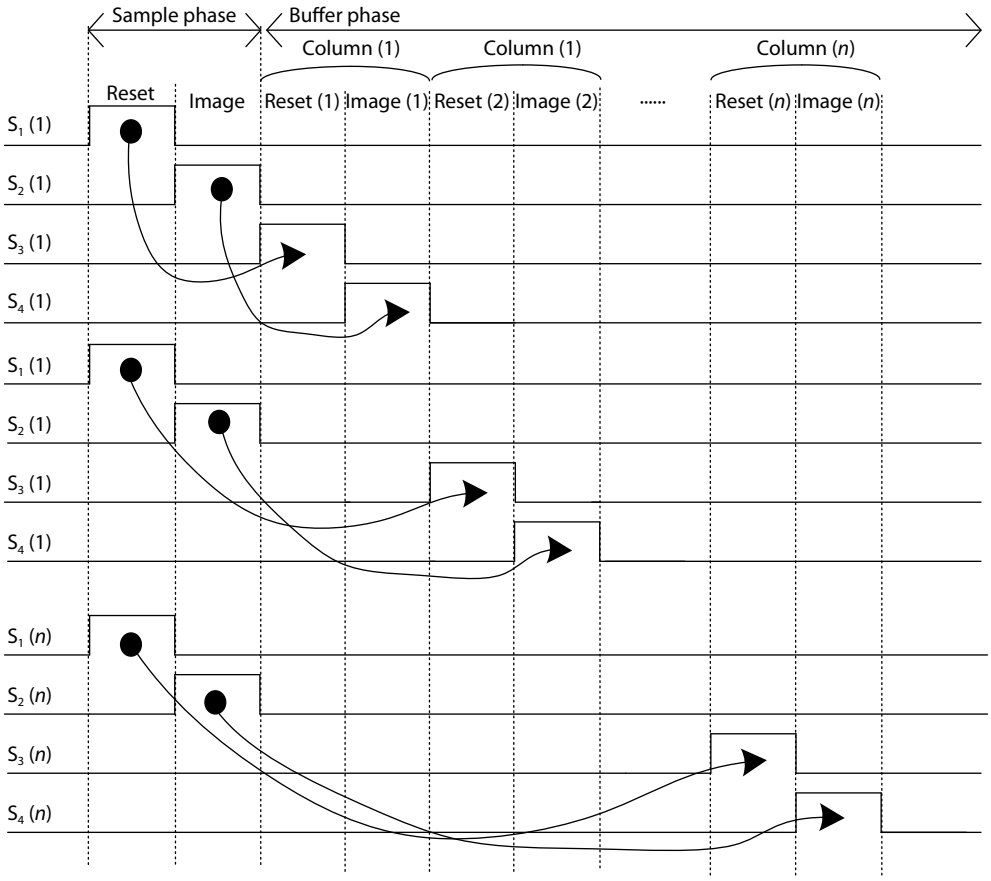


Fig. 6. Control timing of *n* columns readout.

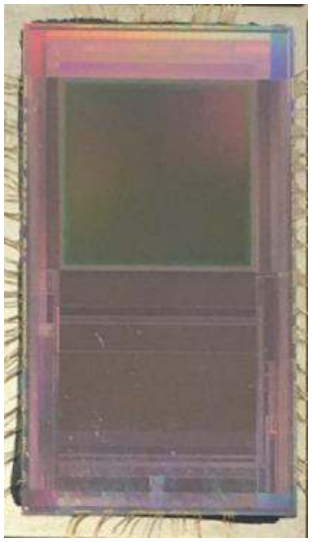

Fig. 7. (Color online) Die micrograph.

set mismatch and charge sharing, the output gray code variances with exposure time and rms value is measured for all pixels by using a 14 bit ADC. Based on EMVA 1288 presented by European Machine Vision Association, a full set of parameters measurement procedures were done on the test image sensor.

Fig. 8 shows a comparative curve with and without the proposed technique applied to the readout circuit under bright and dark conditions. In contrast to conventional architectures, the proposed architecture achieves an excellent linearity output code versus exposure time, which can be increased by 20%. As we can see that the traditional solution dramatically decreased the linearity under bright field and the nonuniformity under dark field, which will deteriorate the image quality during low light to high light application. Furthermore, Fig. 8 shows the measurement results of the nonuniformity with conventional and proposed approach under bright and dark conditions. The proposed architecture can get optimization uniformity lower than ten digital codes, but the conventional method shows a worse noise and growth rate. As is shown, the photo response nonuniformity is reduced by 40% and 30% in bright and dark field. Because the parasitic capacitor can't be matched in the readout chain, the proposed approach without parasitic influence will provide an excellent uniformity. It is verified significantly by the prototype sensor chip, and the statistics results show a better PRNU less than 1.16%. Finally, the comparison of actual image before and after the optimization is shown in Fig. 9. In order to improve the recognition, we extracted part of the image, where the resolution of the pixels shown in the picture is about 10 × 10, and performance summary and comparison with the state of the art are given in Table 1.

## 5. Conclusions

With the pixel array resolution increasing, the column parallel readout topology is facing the challenges in high speed, high accuracy and low noise application. The reset level and the image level of the storage capacitor are sampled by the correlated double sampling technology in the traditional method. However, the offset mismatch which is introduced in the two buffers is not certain related to the

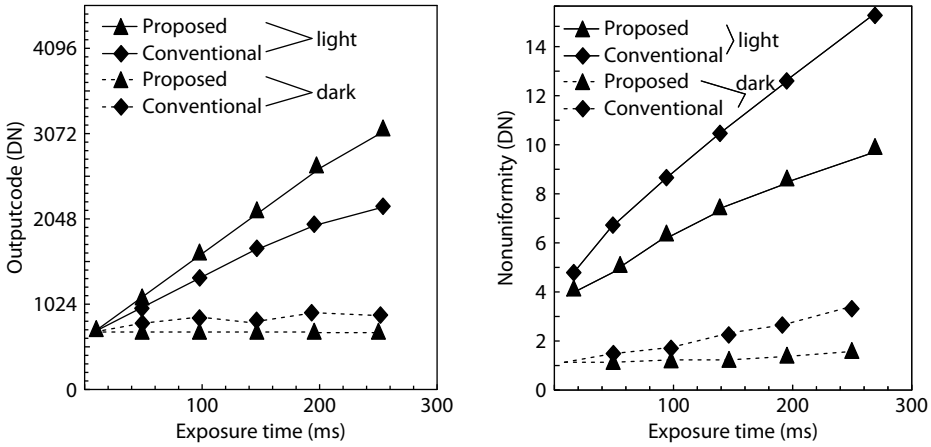


Fig. 8. Output code and nonuniformity versus exposure time.

(a) (b)

Fig. 9. Comparison of actual images before and after optimization. (a) Image with traditional technique. (b) Image with proposed technique.

Table 1. Performance summary and comparison with the state of the art.

| Parameter | This work | Ref. [7] | Ref. [10] |
|---|---|---|---|
| Process | 55 nm CMOS | 40 nm CMOS | 180 nm CMOS |
| Pixel size ($\mu$m) | 5.4 | 5.4 | 2.8 |
| Supply (V) | 3.3/1.2 | 2.5/2/1.1 | 3.3/1.8 |
| Horizontal time ($\mu$s) | 5 | 6.02 | 1.92 |
| Column FPN (%) | 0.0075 | 0.028 | 0.31 |
| Read noise ($\mu$Vrms) | 190 | 261.5 | 320 |
| Dynamic range (intrinsic) (dB) | 75 | 71.8 | 62.9 |
| Photo response nonuniformity | 1.16% | N/A | N/A |

luminance of light, and it can't be cancelled by the CDS because of the intrinsic unbalanced structure and the electrical properties. Due to the difference between the sequential rows, the charge sharing exists in the image level point evidently, and it also exists in the reset level point which is induced by fixed pattern noise. However, the charge sharing which exists in the single buffer structure can result in the charge exchange between the reset level and image level which is critical to the readout noise. Therefore, column readout circuit with improved offset mismatch and charge sharing using a single buffer with eight switches is proposed in this paper. The key technology presented in our design not only avoids the charge sharing through the extra switches, but also keeps the constant operating point, which is favorable to the low noise design. A 1024 × 1024 pixels CMOS image sensor including 1024 columns readout has been fabricated in a 55 nm 1P4M CMOS with pinned photodiode process. The measurement results show that the linear range is extended by 20%, the readout noise is reduced by 40% and 30% in bright and dark field, and the photo response nonuniformity is up to 1.16%. Finally, a raw sample image taken by the prototype sensor shows the excellent practical performance.

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## References

[1] Boukhayma A, Peizerat A, Enz C. Temporal readout noise analysis and reduction techniques for low-light CMOS image sensors. IEEE Trans Electron Devices, 2016, 63(1), 72

[2] Kawai N, Kawahito S. Noise analysis of high-gain, low-noise column readout circuits for CMOS image sensors. IEEE Trans Electron Devices, 2004, 51(2), 185

[3] Yeh S F, Chou K Y, Tu H Y, et al. A 0.66$e_{rms}$- temporal-readout-noise 3-D-stacked CMOS image sensor with conditional correlated multiple sampling technique. IEEE J Solid-State Circuits, 2018, 53(2), 527

[4] Lim Y, Koh K, Kim K, et al. A 1.1e- temporal noise 1/3.2-inch 8 Mpixel CMOS image sensor using pseudo-multiple sampling. IEEE Int Solid-State Circuits Conf Dig Tech Papers (ISSCC), 2010, 396

[5] Seo M W, Suh S, Lida T, et al. An 80 μV rms-temporal-noise 82 dB-dynamic-range CMOS image sensor with a 13-to-19 b variable-resolution column-parallel folding-integration/cyclic ADC. IEEE Int Solid-State Circuits Conf Dig Tech Papers (ISSCC), 2011, 400

[6] Chen N, Zhong S Y, Zou M, et al. A low-noise CMOS image sensor with digital correlated multiple sampling. IEEE Trans Circuits Syst I, 2018, 65(1), 84

[7] Liu Q Y, Edward A, Kinyua M, et al. A low-power digitizer for back-illuminated 3-D-stacked CMOS image sensor readout with passing window and double auto-zeroing techniques. IEEE J Solid-State Circuits, 2017, 52(6), 1591

[8] Kawahito K. Signal processing architectures for low-noise high-resolution CMOS image sensors. IEEE Custom Intergrated Circuits Conference (CICC), 2007

[9] Okura S, Nishikido O, Sadanaga Y, et al. A 3.7 M-pixel 1300-fps CMOS image sensor with 5.0 G-pixel/s high-speed readout circuit. IEEE J Solid-State Circuits, 2015, 50(4), 1016

[10] Watabe T, Kitamura K, Sawamoto T, et al. A 33M pixel 120fps CMOS image sensor using 12b column-parallel pipelined cyclic ADCs. IEEE Int Solid-State Circuits Conf (ISSCC) Dig Tech Papers, 2012, 388