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Contact etch process optimization for RF process wafer edge yield improvement

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Abstract: Radio-frequency (RF) process products suffer from a wafer edge low yield issue, which is induced by contact opening. A failure mechanism has been proposed that is based on the characteristics of a wafer edge film stack. The large step height at the wafer's edge leads to worse planarization for the sparse poly-pattern region during the inter-layer dielectric (ILD) chemical mechanical polishing (CMP) process. A thicker bottom anti-reflect coating (BARC) layer was introduced for a sparse poly-pattern at the wafer edge region. The contact open issue was solved by increasing the break through (BT) time to get a large enough window. Well profile and resistance uniformity were obtained by contact etch recipe optimization.

Key words: bottom anti-reflect coating; break through; wafer edge; planarization

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1. Introduction

CMOS technology has emerged as the leading solution due to its cost advantage, performance improvement, and ease of integration for high-performance digital circuits and high-speed analog/RF circuits. Recently, the CMOS compatible RF process has become the mainstream solution for RF front end modules, especially for switch applications[1–3]. This technology offers a cost effective, high performance alternative to the traditional technology, such as GaAs. The silicon foundry RF process can realize highly integrated RF and analog products, including wireless transceivers, power amplifiers and emerging mm-wave ICs. This platform is now in mass production. However, many abnormal phenomena can take place several millimeters from the wafer's edge, such as yield loss at the wafer edge induced by the process interactions and non-uniformity at edge of the wafer[4–6]. Meanwhile, a failure mechanism and a method to improve the wafer edge yield loss need to be discussed in further detail.

2. Experiment result and discussion

As shown in Fig. 1, some RF process products suffer from wafer edge yield loss. The yield loss is observed at 3 o'clock and 7 o'clock at the wafer's edge. The notch is located on the bottom of the wafer. According to the definition of a failure bin, the yield loss is induced by circuit OPEN. As shown in Fig. 2, contact (CT) open is observed for a poly-sparse pattern at the wafer's edge by scanning electron microscope (SEM). However, no abnormality is observed for the poly-dense pattern and active region. For the RF process platform, an active region (ACT) is generally used for active devices, such as MOSFETs and diodes. The poly-major is located at the top of shallow trench isolation (STI) region, such as the high resistivity resistance, which is used for DC bias control terminal. To reduce the coupling and parasitic effect, ACT and poly-dummy patterns are forbidden. Consequently, an obvious distinction is observed for different poly-pattern regions.

In the device manufacturing process, edge bead removal (EBR) is carried out during the PH loop by directing a controlled stream of developer solvent at the edge of the wafer. Wafer edge exposure (WEE) is often used together with EBR. A clean ring is created at the wafer's edge[7]. Consequently, there is big step height from the wafer's edge to the inside of the wafer. The edge characteristics of the wafer will have a negative impact on the full loop process. For the inter-layer dielectric (ILD) chemical mechanical polishing (CMP) process loop, even for a deposition of a thick layer oxide, the planarization is not good for the wafer's edge, especially for different ACT/poly-pattern regions.

ILD can be introduced by plasma-enhanced chemical vapor deposition (PECVD) SiN, boro-phospho-silicate-glass (BPSG) deposition and densify post the front-end-of-line (FEOL) CMOS process[8]. The CMP process is then applied for planarization. The ILD CMP process loop will be impacted by the ACT and poly-pattern. For the ACT block and poly-dense

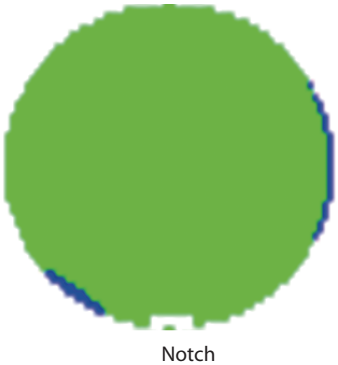

Fig. 1. (Color online) Yield loss map induced by the CT open issue.

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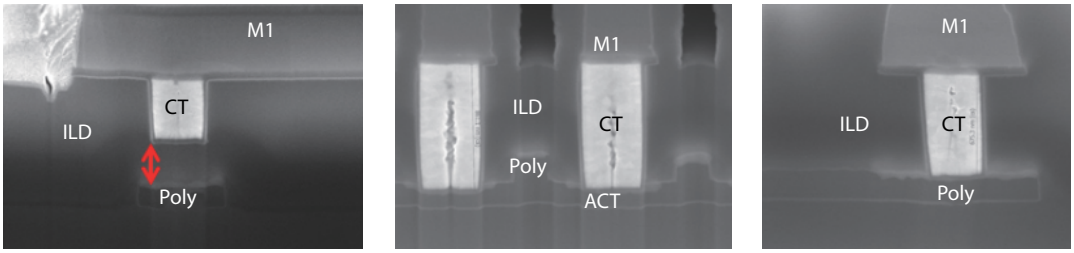


Fig. 2. FA SEM result for a CP fail sample at different pattern regions: (a) CT on poly-sparse pattern; (b) CT on an active region; and (c) CT on a poly-dense pattern. M1 is metal 1 for electrical connection, ILD is inter-layer-dielectric, ACT is active region for device, poly is for MOSFET or resistance, salicide is formed between CT and ACT/poly.

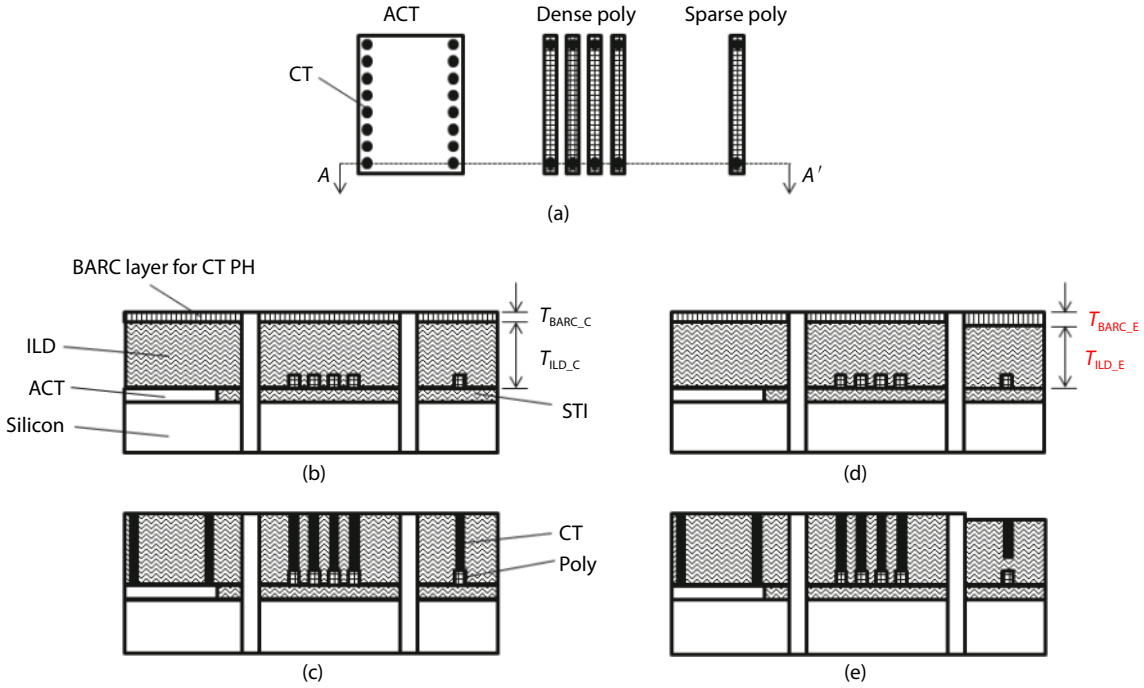


Fig. 3. Failure mechanism for CT open for sparse poly-pattern at most of the wafer's edge. (a) CT pattern top view. (b) BARC layer wafer center. (c) CT formed at wafer center. (d) BARC layer wafer edge. (e) CT formed at wafer edge.

Table 1. Etch rate for BARC and ILD oxide.

CT etch step		BARC	ILD oxide
1st step	BT (CF4 base)	1	2.938
2nd step	ME (C5F8 base)	0.102	1

region, the post-CMP thickness is relatively high. However, for the poly-sparse pattern, the post-CMP thickness is relatively lower. This is generally induced by the micro-loading effect[9]. Therefore, the pre-ILD CMP thickness is thinner at the wafer's edge. In general, the CMP remove rate is higher at the wafer's edge. We have experimented for ILD CMP optimization to improve the thickness uniformity[10, 11], although the CT open issue is still unsolved. The result is not shown here for the sake of clarity. Fig. 3 shows the proposed failure mechanism for CT open for a sparse poly-pattern at most of the wafer's edge. As shown in Fig. 3(a), the following three typical patterns are analyzed: ACT block pattern, dense poly-pattern, and sparse poly-pattern. As shown in Figs. 3(b) and 3(d), the bottom anti-reflect coating (BARC) layer is thicker at the sparse poly-pattern at most of the wafer's edge (T_{BARC_E} > T_{BARC_C}), which is mostly due to the thinner ILD oxide (T_{ILD_C} >

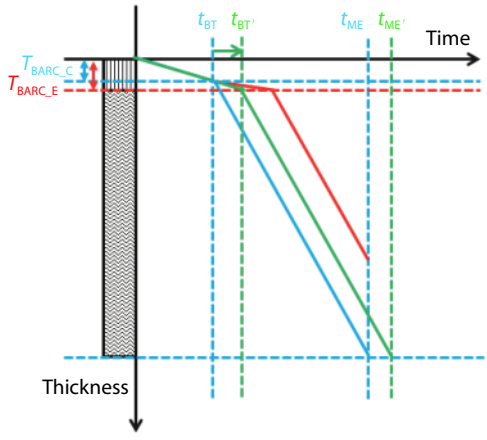
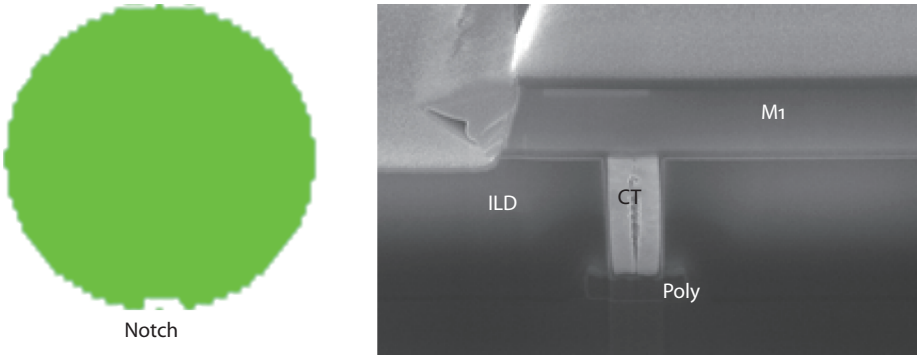


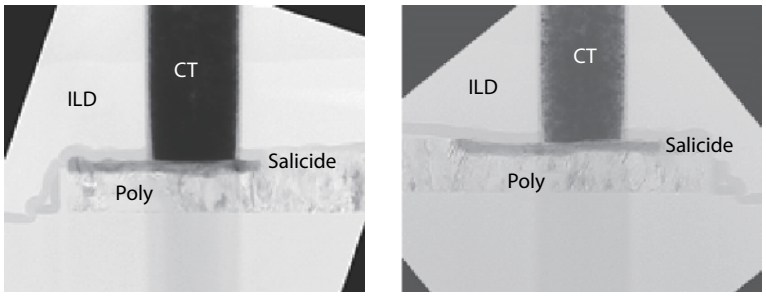
Fig. 4. (Color online) Instruction for CT etch BT and ME steps pre- and post-optimization. The blue line is normal CT etch process for wafer center; the red line is pre-optimization CT etch process at wafer edge; the green line is post-optimization CT etch process at wafer edge.

T_{ILD_E}). A BARC layer is used to avoid the standing wave effect during the PH process[12]. The CT pattern is obtained by a



(a) (b)

Fig. 5. (Color online) (a) Yield map and (b) SEM result at CT on sparse poly-pattern at wafer edge with CT etch optimization recipe.



(a) (b)

Fig. 6. TEM result for CT etch process with (a) POR and (b) post-optimization recipe.

PH loop with a mask.

The aim is to optimize the CT etch process. The etch process has previously been studied[13, 14], although the process steps were not discussed in detail. The CT etch process split has two steps: the first is the break through (BT) step for the BARC layer etch; and the second is the main etch (ME) step for the ILD oxide etch. The CT etching is stopped at the salicide layer on active and poly. Fig. 3(c) shows the CT touch salicide well for the wafer center pattern. The etch rate of BT and ME for BARC and oxide is checked step-by-step. Table 1 shows the etch rate for BARC and ILD oxide by BT and ME base, which defines the unit etch rate for BT etch BACR, and ME etch oxide, respectively. The CT etch rate is also a little lower at the wafer's edge. The ILD oxide etch rate is relatively low with the first BT step CF4 base. The ratio of the oxide etch rate to the BACR etch rate is 0.102 to 1. Consequently, the thicker BARC at the wafer edge sparse poly-pattern region will consume most of the ME C5F8 to remove the BARC. Then, the etch time of the ILD oxide remove is lost. The CT cannot touch the salicide of poly. As shown in Fig. 3(e), CT open is observed for a wafer edge poly-sparse pattern.

Based on the FA SEM result, the ILD thickness is thinner for the poly-sparse pattern at the wafer's edge. During the BARC layer process loop, a thicker BARC layer is formed at the poly-sparse pattern at most of the wafer's edge region. The thickness of BARC and ILD under the etching process is shown in Fig. 4. The blue marked line is the instruction for CT etch process with normal BARC thickness. The CT etch first step is BT with CF4 base, this step etch oxide is also relatively high. However, the second ME step with C5F8 base, the etch rate for BARC layer is relatively lower. Suppose that the BARC layer is thicker at the sparse poly-pattern at most of the wafer's edge ($T_{BARC\_E} > T_{BARC\_C}$). When the BT step is not enough for the BARC layer etch, the ME step will consume most of the time to open the BARC due to the low etch rate. As shown in Fig. 4, the red line marked ILD oxide is not fully etched. Consequently, the height post CT etch is relatively lower, and cannot even touch the top salicide of the sparse poly-pattern. CT open is observed, which leads to circuit OPEN and yield loss. By increasing the t_{BT} to $t_{BT'}$, there is no BARC residue post-BT etch, the ME can then etch the ILD oxide smoothly. In other words, by increasing the BT time to make sure that there is enough BARC layer etch, we can avoid the CT open issue.

Based on the proposed failure mechanism and etch rate, an experiment that increases the BT time is applied. By increasing 50% BT time, CT open is avoided at the poly-sparse pattern at most of the wafer's edge. The optimization result is shown in Fig. 5. The CP yield map is normal for the optimization CT etch recipe. During the recipe optimization, we keep the ME time because the etch rate of C5F8 on BARC is too low. Based on the SEM result for CT on sparse poly-pattern and CP data, increasing the BT time is efficient. The SEM result for CT on ACT and dense poly is not shown for the sake of clarity.

As shown in the Fig. 6 (TEM picture), the CT tungsten touched the poly-salicide well. The salicide thickness is comparable with the baseline center one. During the CT etch process, the etch loop will stop on the salicide layer. The increased BT time may induce salicide damage. The CT profile is checked by TEM for sparse poly-pattern located at the wafer's center. As shown in Fig. 6, no abnormality is observed for the CT/salicide/poly profile with the optimization etch recipe. The thickness of the salicide is comparable for POR and for the post-optimization recipe. N plus (RcN+) and

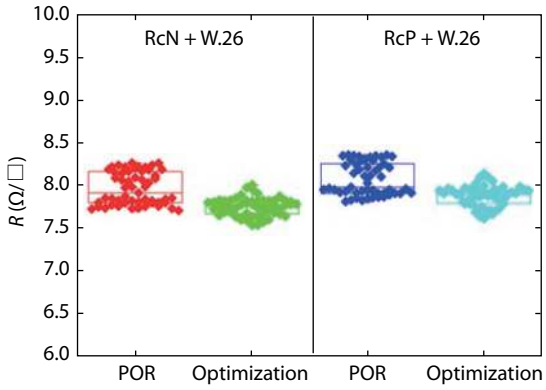


Fig. 7. (Color online) RcN+ and RcP+ WAT mapping data BOX chart. W.26 mean the CT size is 0.26×0.26 μm^2.

P Plus (RcP+) type contact resistance is monitored after the full process loop. As shown in Fig. 7, the resistance mapping test result for RcN+ and RcP+ is comparable for POR and the optimization CT etch recipe. The 54 testkey sites on the wafer are summarized in a BOX chart. The uniformity is a little better for the post-optimization version.

3. Conclusion

In summary, RF process wafer edge yield improvement is obtained by CT etch recipe optimization. A failure mechanism is proposed based on the wafer edge film stack characteristics. The large step height at wafer's edge leads to worse planarization for the sparse poly-pattern region during the ILD CMP process. A thicker BARC layer is introduced for sparse poly-pattern at the wafer's edge region. The contact open issue is solved by increasing the BT time to get enough window. A good SEM result for CT on sparse poly-pattern and improved CP data are obtained with an optimized etch recipe. A good profile for CT/salicide/poly at the wafer's center is obtained by TEM. Finally, good uniformity is observed for the RcN+ and RcP+ resistance by the mapping test.

Acknowledgments

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