

III–V compound materials and lasers on silicon

Wenyu Yang^{1, 2, 3}, Yajie Li^{1, 2, 3}, Fangyuan Meng^{1, 2, 3}, Hongyan Yu^{1, 2, 3}, Mengqi Wang^{1, 2, 3}, Pengfei Wang^{1, 2, 3}, Guangzhen Luo^{1, 2, 3}, Xuliang Zhou^{1, 2, 3, †}, and Jiaoqing Pan^{1, 2, 3, †}

¹Key Laboratory of Semiconductor Materials Science, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China

²Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences, Beijing 100049, China

³Beijing Key Laboratory of Low Dimensional Semiconductor Materials and Devices, Beijing 100083, China

Abstract: Silicon-based photonic integration has attracted the interest of semiconductor scientists because it has high luminous efficiency and electron mobility. Breakthroughs have been made in silicon-based integrated lasers over the past few decades. Here we review three main methods of integration of III–V materials on Si, namely direct growth, bonding, and selective-area hetero-epitaxy. The III–V materials we introduced mainly include materials such as GaAs and InP. The lasers are mainly lasers of related communication bands. We also introduced the advantages and challenges of the three methods.

Key words: integrated photonics; hybrid laser; silicon

Citation: W Y Yang, Y J Li, F Y Meng, H Y Yu, M Q Wang, P F Wang, G Z Luo, X L Zhou, and J Q Pan, III–V compound materials and lasers on silicon[J]. *J. Semicond.*, 2019, 40(10), 101305. <http://doi.org/10.1088/1674-4926/40/10/101305>

1. Introduction

Over the past half century, technological innovation and industrial revolution represented by microelectronics technology and integrated circuits have led the world into a highly informational, networked and intelligent era. Microelectronic devices have laid the foundation for the rapid development of society. At the same time, higher requirements for the performance of microelectronic devices and integrated circuits have been proposed to meet the needs for a larger amount of information acquisition and processing. However, conventional silicon integrated circuits have become increasingly unable to meet increasing demands in terms of data processing speed and bandwidth performance. For decades, people have been working to improve the integration of microelectronics chips to solve related problems, but the average cost per chip is still high on each wafer. Several physical effects^[1, 2] caused by CMOS technology during the scaling down process will severely degrade the performance of MOS-FET devices. III–V compound materials have an extremely high electron mobility and are the most likely alternative to Si-based nMOS channels^[3, 4]. The high cost of microelectronic devices also indicates that it has become more and more difficult to achieve high-speed, low-cost and low-energy communication and information processing by reducing the size. The development of traditional silicon-based microelectronic devices has encountered bottlenecks.

In order to solve the above problems, people have turned their attention to photonics, and use photons as a carrier for information processing and transmission^[5]. The propagation speed of optical signals in optical fibers or optical waveguides is much greater than that of electrical signals in metal

wires. High speed means greater bandwidth and system capacity in the communication system, and the realization of optical wavelength division multiplexing, time division multiplexing, space division multiplexing, and mode multiplexing technology further increases the bandwidth of optical communication. The energy loss of photons is much lower than that of electrons and is not easily interfered by external electromagnetic fields. Therefore, a breakthrough in silicon-based photonic integration technology is required to provide highly integrated low-power optical modules. And the development of low-cost silicon-based photonic integrated devices is one of the best solutions for the above difficulties. Combining electronics and photonics to achieve photonic integration is a reliable way to solve the lack of speed and bandwidth of electronic devices^[6–11].

Considering the compatibility with CMOS processes, it is a general trend to manufacture and integrate various photonic devices on silicon. Here we review three main methods of integration of III–V materials on Si, namely direct growth, bonding, and selective-area hetero-epitaxy. The III–V materials we introduce mainly include materials such as GaAs and InP. The lasers are mainly lasers of related communication bands. We also introduced the advantages and challenges of the three growth methods.

2. Methods of integration of III–V materials on Si

2.1. Direct growth of III–V materials on Si

The direct growth of III–V compound semiconductors on silicon is the first attempt^[12–19]. But there are many challenges like antiphase boundaries (APBs), thermal mismatch and lattice mismatch for direct growth of GaAs, InP, and other III–V compound semiconductors on Si. Thus, solving these major problems is the initial step to fabricate GaAs or InP based devices on Si. APBs usually happen when III–V materials are grown on elemental semiconductors. Fig. 1 shows APBs on the surface of a GaAs layer on Ge. These could lead

Correspondence to: X L Zhou, zhouxl@semi.ac.cn; J Q Pan, jppan@semi.ac.cn

Received 28 MAY 2019; Revised 26 AUGUST 2019.

©2019 Chinese Institute of Electronics

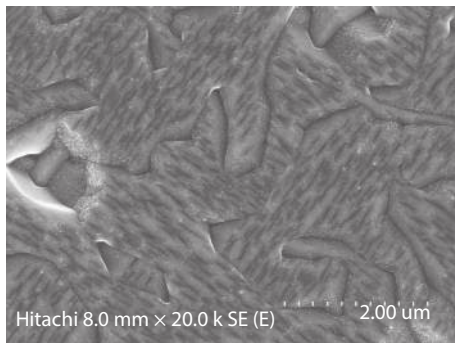


Fig. 1. Plane view SEM image of GaAs on Ge etched by melt KOH.

to a rough surface, carrier or photo scattering at the boundaries and so on. To solve this, miscut substrates and high temperature treatment of substrate surface before growth are normal methods, which are widely applied^[20, 21]. By the above-mentioned methods, bi-atomic steps at the Si or Ge surface are obtained, through which single-domain GaAs is grown with an As-atom prelayer.

The GaAs-based material system is the most studied III–V compound on Si because of its wide usage and relatively smaller lattice mismatch compared with InP-based materials. To solve the mismatch problem such as InGaAs interlayer^[20], post-annealing^[21, 22], two-step growth, and so on for GaAs on Si have been used. Also, a nuclear layer like AlGaAs or GaP is also applied^[23, 24]. Due to the similar lattice constant of the Ge and GaAs crystals, a Ge interlayer is often used as a buffer layer between the GaAs layer and the Si substrate^[25]. Fig. 2 shows an example of a GaAs layer on Si by a Ge buffer layer which is grown by ultra-high vacuum chemical vapor deposition (UHV-CVD). High density of dislocations appears at the interface of Ge and Si and self-annihilation phenomenon^[25, 26] could be observed at the GaAs and Ge interface.

Although much effort has been made, there are no practical devices that have been fabricated on the GaAs/Si platform, because the lowest defect density for the GaAs top layer could reach only 10^5 – 10^6 cm⁻²^[25, 27]. And, it is impossible to obtain devices on InP/Si system for even higher defect density of 10^7 cm⁻²^[23].

Although it is difficult to achieve high performance devices on III–V/Si material system, research has not been suspended, especially lasers on Si. Due to proper band structure, III–V materials are grown on Si for light source emitting at fiber-optic communication wavelength. From the 1980s, GaAs/AlGaAs^[28] and InGaAs/InGaAsP^[29] quantum well lasers on Si were achieved, emitting at 810 and 1540 nm, respectively. As mentioned above, these devices could not be widely used because of their high defect density.

InAs quantum dot (QD) lasers operating at 1.3 μm have recently been grown on miscut Ge^[29] or Si^[30, 31] using solid-source MBE technology. It is found that QDs and strained-layer superlattices could be grown in the buffer as dislocation filters. Also, nucleation layers like AlGaAs^[31] or AlAs^[30] could be applied for APB reduction. The high QD density provides reduced sensitivity to crystalline defects allowing for long device lifetimes^[32]. The 3D carrier confinement confines the carriers inside quantum dots that reduces sensitivity to defects. By the above methods, reliable, efficient electrically pumped silicon-based InAs/GaAs quantum dot lasers are achieved with a low threshold current density of 62.5 A/cm²,

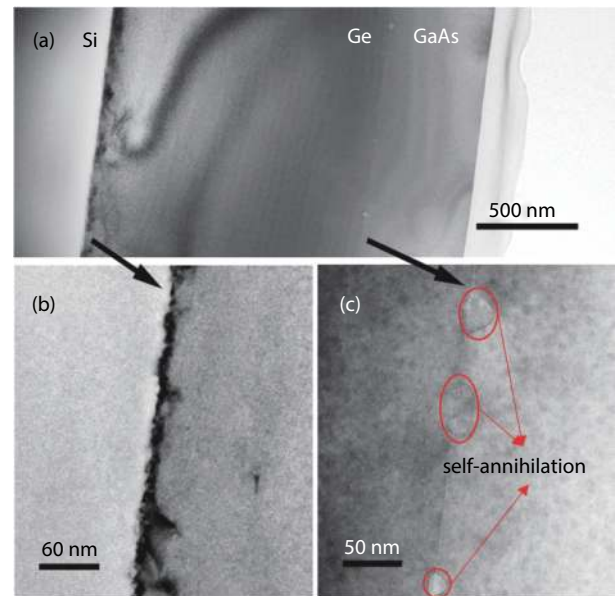


Fig. 2. (Color online) (a) TEM images of GaAs on Si with a Ge buffer. (b) and (c) show the Ge/Si interface and the GaAs/Ge interface, respectively^[26].

a room-temperature output power exceeding 105 mW and operating up to 120 °C, as shown in Fig. 3. The extrapolated mean time to failure is estimated at over 100 000 h^[30]. Other researchers found that reducing the dislocation density has improved the InAs quantum dot laser lifetime from a few thousand hours to more than 10×10^6 h. Lowering the dislocation density also helped in maintaining the slope efficiencies of the lasers during the aging test^[33]. The researchers grew 1.3 μm InAs quantum dot lasers on silicon by molecular beam epitaxy. The room temperature continuous wave threshold is as low as 16 mA, with output power exceeding 176 mW, and lasing up to 119 °C^[34]. Recently researchers have reported the realization of 1.5 μm room-temperature electrically pumped epitaxially grown on standard (001) Si substrates without offcut. A threshold current density of 1.6 kA/cm², a total output power exceeding 110 mW, and operation up to 80 °C under pulsed current injection have been achieved^[35]. Also, quantum well lasers and micro-disk InAs QD lasers fabricated on patterned, miscut substrates are not compatible with CMOS processing and the patterned, on-axis (001) Si would be a solution for integration application^[36, 37]. Based on light source research on Si by large area growth in recent years, InAs QD lasers might be a solution to the light source on Si for opto-electronic integration.

In short, the research on silicon-based large-area epitaxial III–V semiconductors has been carried out very early, and material defects have not been completely solved. In addition, the laser fabricated by this method still needs to grow a thick buffer layer between the III–V semiconductor and the silicon substrate, and the defect density in the buffer layer is relatively large, which greatly reduces the coupling efficiency and device lifetime at elevated temperature, respectively. Silicon-based quantum dot lasers have made great progress, but the gain is still relatively low. Therefore, there is a limitation in the large-scale integration of light sources on silicon by the conventional buffer layer epitaxial III–V semiconductor material method.

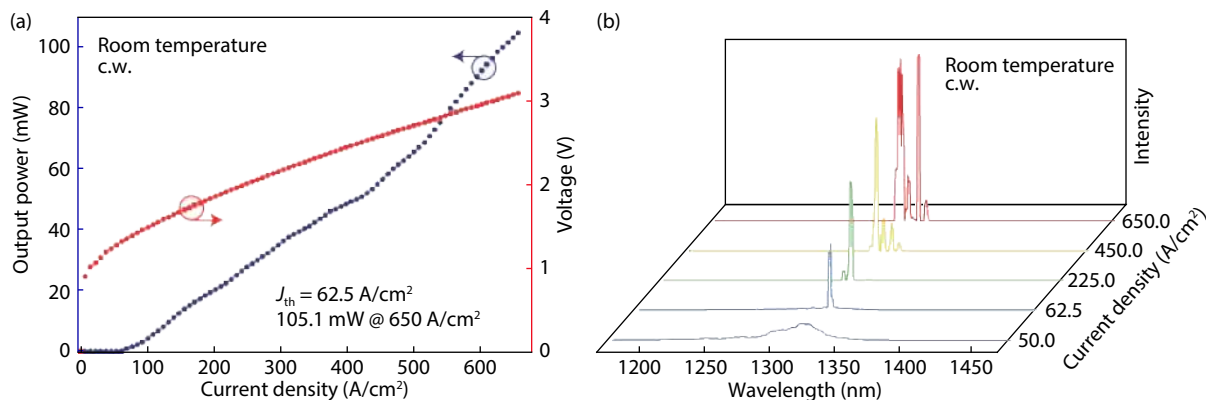


Fig. 3. (Color online) (a) CW PIV characteristics for an InAs QD laser on Si at 18 °C. (b) Emission spectrum for this device at various inject current density^[31].

2.2. Silicon-based bonded lasers

In the current situation, bonding is a very practical method^[38]. As the name suggests, bonding is the combination of two wafers or devices by heating or pressing directly or through the intermediate layer, which avoids direct contact of semiconductor atoms, thus effectively solving the growth of III–V materials on silicon. Direct bonding, adhesive bonding and metal bonding are currently the three most important bonding methods.

Direct bonding does not require any medium, and directly bonds two substrates with atomic level flat surfaces together using heat and pressure^[39–46]. But due to different thermal expansion coefficients of different materials, high temperature processing will introduce thermal stress. If the thermal stress is too large, defects and dislocations will be formed. Researchers proposed a method of activating the bonding surface with oxygen plasma before bonding that successfully reduced the bonding temperature to below 300 °C^[46]. UCSB and Intel researchers obtained the first electrically pumped hybrid integrated AlGaInAs/Si FP cavity laser by using the oxygen plasma-assisted direct bonding scheme^[41]. The laser has a threshold current of 65 mA, a maximum output power of 1.8 mW with a differential quantum efficiency of 12.7% and a maximum operating temperature of 40 °C. Another group demonstrated the first electrically pumped DFB silicon evanescent laser^[40], with the maximum output power of 5.4 mW and a threshold current of 25 mA at 10 °C. The maximum operating temperature and minimum line width of the laser are 50 °C and 3.6 MHz, respectively.

Adhesive bonding mainly uses some high molecular organic materials as a bonding material to bond the chip and the wafer. Commonly used bonding materials are mainly benzocyclobutene (BCB), photoresist and polyimide. The adhesive bonding process is simple, the bonding temperature is low, the requirement for surface flatness is relatively low, and the bonding strength is high. However, the main problem is that the organic material used for bonding has poor electrical and thermal conductivity. Ghent University, in conjunction with several organizations, produced a hybrid integrated silicon-based DFB laser using an ultra-thin BCB bonding layer^[47]. Both III–V and Si use the taper structure to achieve adiabatic mode conversion, and etch the gratings directly onto the Si waveguide. The hybrid integrated silicon-based DFB laser has a lasing wavelength of around 1550 nm, a single-facet maximum

output power of 14 mW, a side mode suppression ratio (SMSR) of 50 dB and a maximum operating temperature of 60 °C. The research team of the Institute of Semiconductors of the Chinese Academy of Sciences used BCB bonding to realize 16-channel silicon-based microdisk laser arrays^[48], with 16 channels outputting light from a silicon waveguide. The laser is a room temperature pulse lasing with a lasing wavelength around 1550 nm and a wavelength interval of 3 nm.

Metal bonding refers to the bonding of two wafers or devices by means of a pure metal or alloy, by metal bonding, metal melting or diffusion between metal and wafer. Its main advantages are superior electrical performance, high reliability, good thermal conductivity, and effective release of stress. Andrijasevic *et al.* used Au–Au hot pressing to bond a GaAs-based quantum cascade laser to a silicon substrate at a bonding temperature of 330 °C^[49], operating at a wavelength of 12 μm and a maximum output power of 550 mW. Metal absorbs light at long wavelengths very weakly, but for light in the communication band, the metal absorbs strongly. Researchers proposed a scheme for selective area metal bonding (SAMB) method^[50–52], which effectively avoided the metal absorption of the light by laterally separating the optical coupling region from the metal bonding region. We demonstrated an evanescently coupled InGaAsP/Si hybrid DFB laser with a buried ridge stripe (BRS) structure based on the SAMB method^[53], as shown in Fig. 4(a). The hybrid DFB laser has a threshold current as low as 5 mA at room temperature in CW operation as shown in Fig. 4(b), and it emits at a wavelength of 1536 nm with a SMSR of ~40 dB as shown in Fig. 4(c).

In short, bonding is a very practical method so far. At the same time, bonding is a relatively mature method, and there are already some applications in the business such as Intel and Juniper Network. It can be used to effectively solve the excessive defect density caused by growing III–V materials on silicon and to integrate light sources on silicon for large scale commercialization.

2.3. Selective-area hetero-epitaxy

Selective-area hetero-epitaxy, which is an epitaxial method that restricts epitaxial materials in the pre-defined regions^[54–57]. Aspect ratio trapping (ART) is a kind of selective-area hetero-epitaxy method. In recent years, the use of ART to epitaxially grow III–V material in the trench of Si has been proposed and quickly attracted widespread attention. The epitaxial technique uses high aspect ratio to limit de-

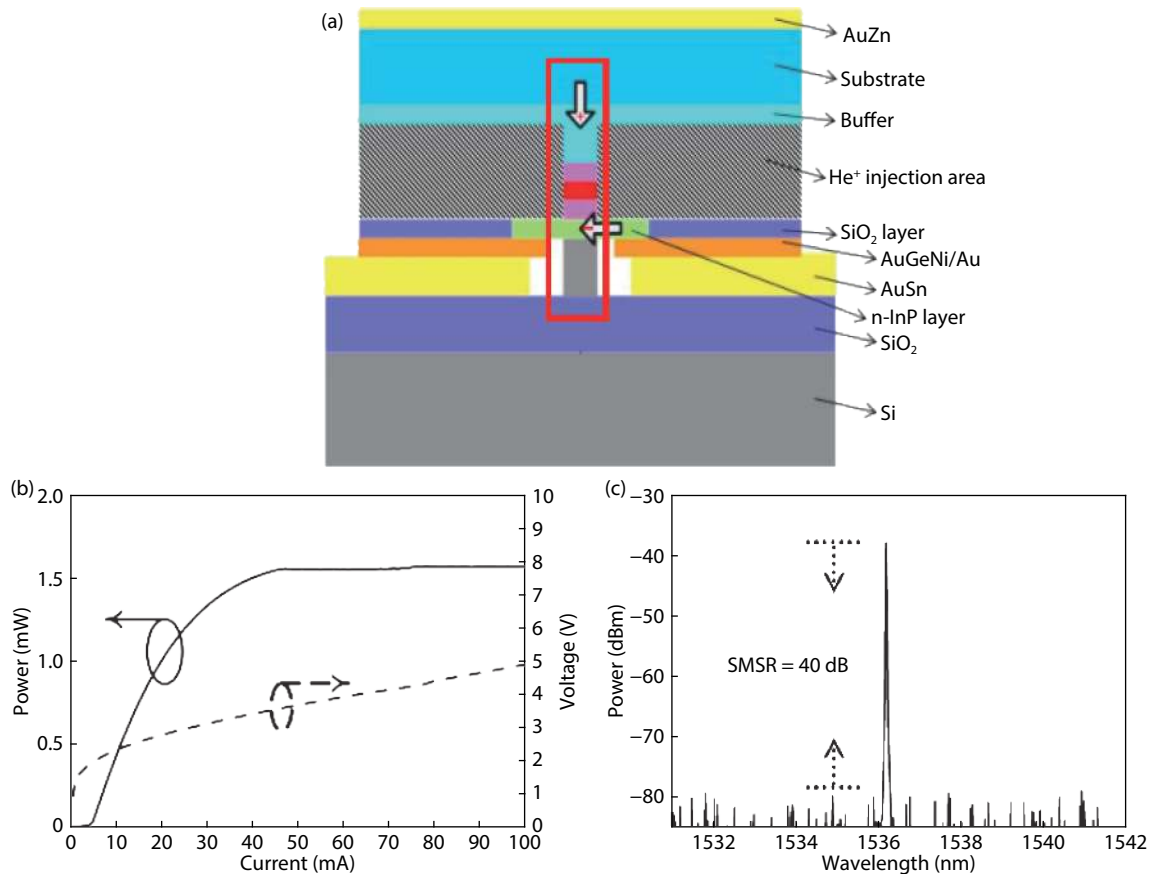


Fig. 4. (Color online) (a) The cross-sectional schematic diagram of the hybrid laser. The arrows marked with “+” and “-” show hole and electron flows, respectively. (b) Single-sided L - I - V characteristics of the hybrid BRS laser under continuous wave (CW) condition at room temperature. (c) The optical spectrum at 30 mA injection current with a 40 dB SMSR.

fects from the Si surface to the bottom of the trench by using SiO_2 sidewalls, thereby obtaining high-quality, dislocation-free III-V material at the top. By depositing a SiO_2 or SiN_x dielectric layer on the surface of the substrate, photolithography is used to etch the desired pattern as a growth window. Relative to the nucleation of the semiconductor surface, the III-V material requires greater nucleation energy when nucleating on the surface of the SiO_2 or SiN_x , so the III-V material preferentially grows in the selected window region. During the epitaxy process, the precursor diffuses laterally from the mask region to the window region, so that the growth rate of the material increases, and the solid solution composition of the material also changes accordingly.

The selective-area hetero-epitaxy technique was used in the heteroepitaxial epitaxy of silicon-based III-V materials^[56]. The results show that this technology can effectively reduce the stress effect between silicon and III-V, which significantly improves the surface warpage and microcracks caused by compressive strain. In 1993, researchers at the University of London further implemented heteroepitaxial growth of GaAs/AlGaAs quantum well structures on silicon substrates by selective-area hetero-epitaxy^[57]. After this, a unique growth method derived from selective-area hetero-epitaxy was discovered that can better limit defects, called ART. The ART method was firstly used to grow Ge on Si. MIT researchers used this principle to grow Ge on a silicon substrate with a circular pattern and to obtain a defect-free layer on top^[54]. Park and Bai of AmberWave company reported high-quality Ge ma-

terials through trenches with SiO_2 sidewalls with an aspect ratio bigger than 2 on Si substrates^[58] in 2006. In order to grow high mobility materials, GaAs materials were grown. The following year, the company reported high-quality GaAs through ART method^[59], as shown in Fig. 5. The researchers used photolithography and reactive ion etching (RIE) to etch trenches through 500 nm thick thermally grown SiO_2 films on Si substrates, using a MOCVD to grow GaAs in the trenches. Through this method, GaAs approximately 300 nm wide and free of near-surface defects, as shown in Figs. 5(a) and 5(b), was grown. This article shows great promise for the integration of other III-V materials on Si substrates.

To better limit defects, researchers have applied V-grooves to grow materials. Researchers have successfully used MOCVD to epitaxially produce high-quality GaAs materials on Si (001) substrates^[60, 61], as shown in Figs. 6(b) and 6(c). During the epitaxy, the III-source and V-source sources continuously migrate into the v-groove of silicon and nucleate on both facets constituting the V-groove (the silicon (001) plane is covered by SiO_2 , so the atoms participating in the reaction will not nucleate). The V-groove of silicon is composed of two $\langle 111 \rangle$ facets, the III-V material forms a diatomic step when nucleating on these two facets, and the APBs between III-V and silicon can be suppressed. At the same time, dislocations between III-V and silicon can be limited by the sidewalls of the trench. Therefore, the method of performing selective growth on a pre-fabricated silicon substrate can effectively eliminate various defects caused by the growth of the

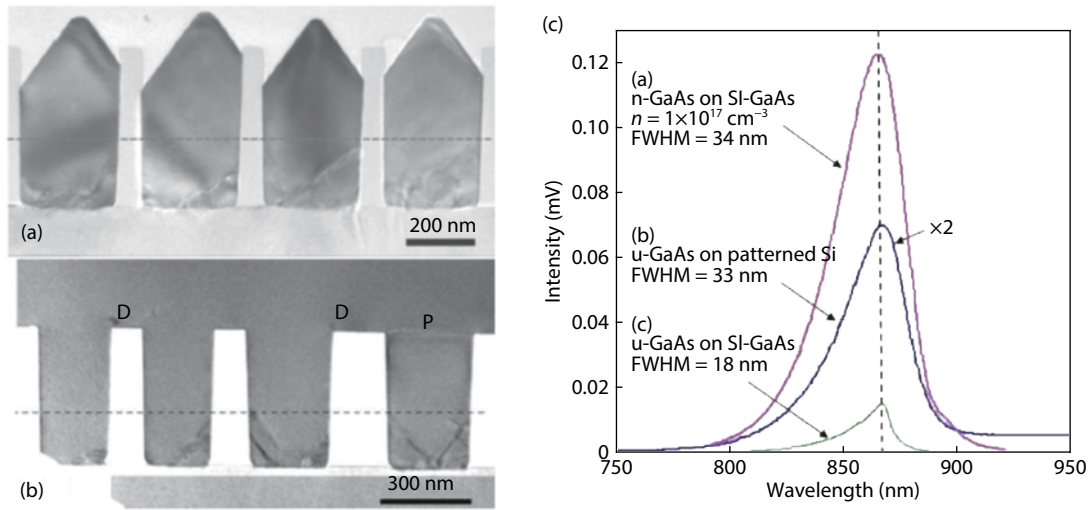


Fig. 5. (Color online) (a) ART technology silicon-based GaAs heteroepitaxial TEM image. (b) Lateral coverage epitaxial results. (c) Room temperature photoluminescence of GaAs grown on Si-GaAs substrate.

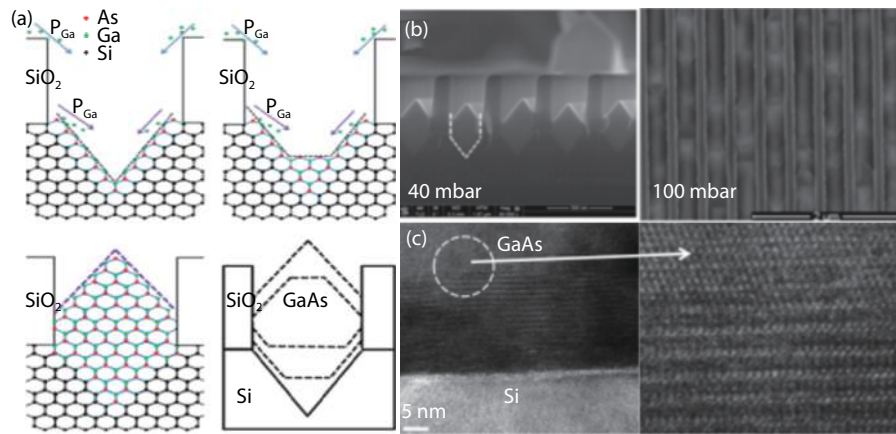


Fig. 6. (Color online) (a) Schematic diagram of growing GaAs. (b) SEM image of GaAs. (c) TEM image of GaAs.

III-V compound semiconductor material on planar silicon. The structural scheme can effectively suppress the generation of APBs and greatly improve the quality of the epitaxial material, as shown in Fig. 6(a).

In order to expand the range of applications of the materials, researchers have also developed InP-based materials, a material that can be used to emit light in the telecom wavelengths. In 2010, researchers at IMEC successfully grew InP materials on Si substrates by growing a thin layer of Ge buffer layer and SiO₂ trench isolation to suppress dislocations^[62], as shown in Figs. 7(a) and 7(b). In 2012, they used V-grooves to restrict the antiphase boundaries (APBs) by depositing a III-V material in shallow trench isolation (STI) patterned Si wafers^[63], as shown in Fig. 7.

To achieve the communication band, researchers have grown some quantum well materials like InGaAs/InP multiple quantum wells. The researchers epitaxially grew high-quality InP materials on this basis. To realize silicon-based high gain laser materials the InGaAs/InP multiple quantum well structure was successfully epitaxially grown on InP materials^[64, 65], as shown in Figs. 8(a) and 8(b). The quantum well has a well-barrier interface with a fluorescence spectrum of 1.5 μm , which is a potential good gain material for the laser, as shown in Fig. 8.

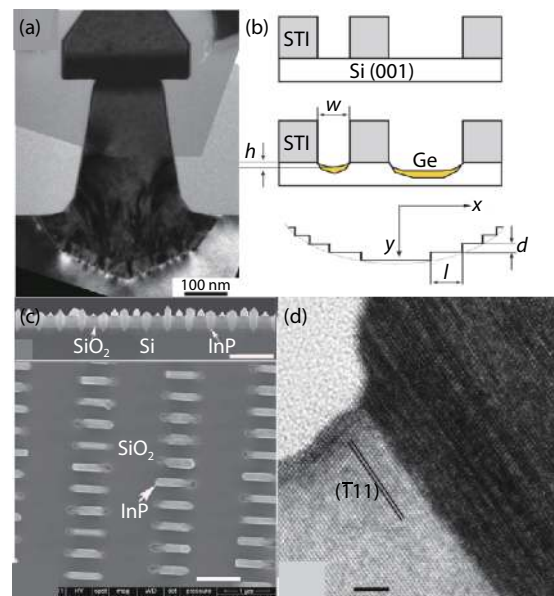


Fig. 7. (Color online) (a) ART technology silicon-based InP growth SEM image in 2010. (b) Schematic diagram of the atomic step creation mechanism. (c) ART technology silicon-based V-groove InP growth SEM image in 2012. (d) High-resolution TEM image at Si and InP (111) interface.

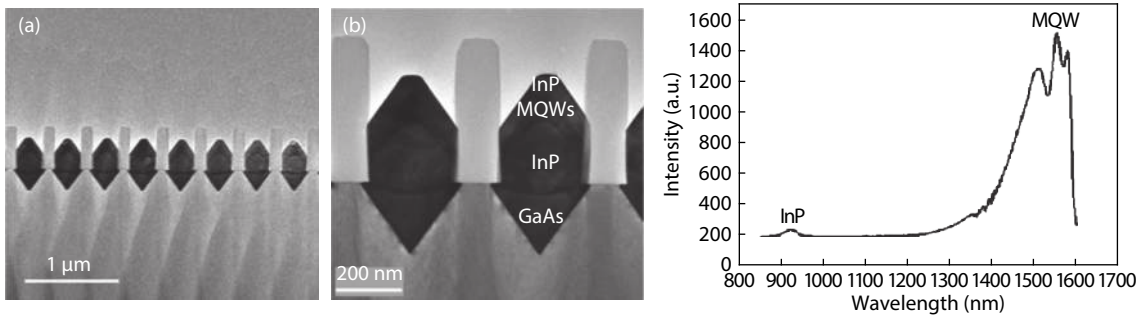


Fig. 8. Silicon-based InGaAs/InP multiple quantum well structure and its photoluminescence spectrum at room temperature.

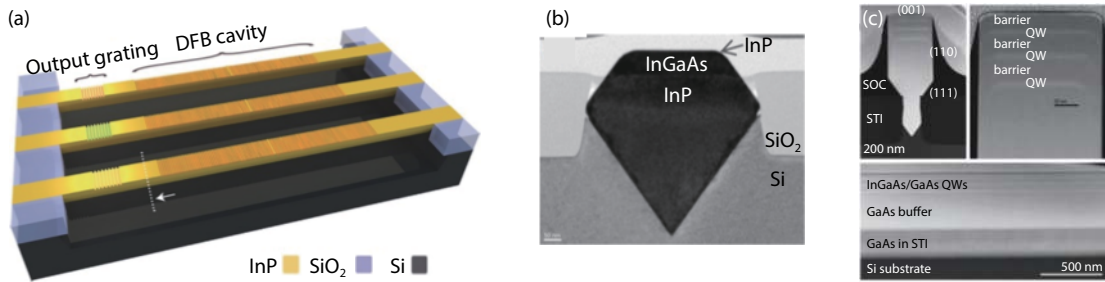


Fig. 9. (Color online) (a) Schematic diagram of a silicon-based InP DFB optical pump laser. (b) Cross-section electron micrograph of a silicon-based InP/InGaAs optical pump laser. (c) Cross-section electron micrograph of a silicon-based GaAs/InGaAs nanowire.

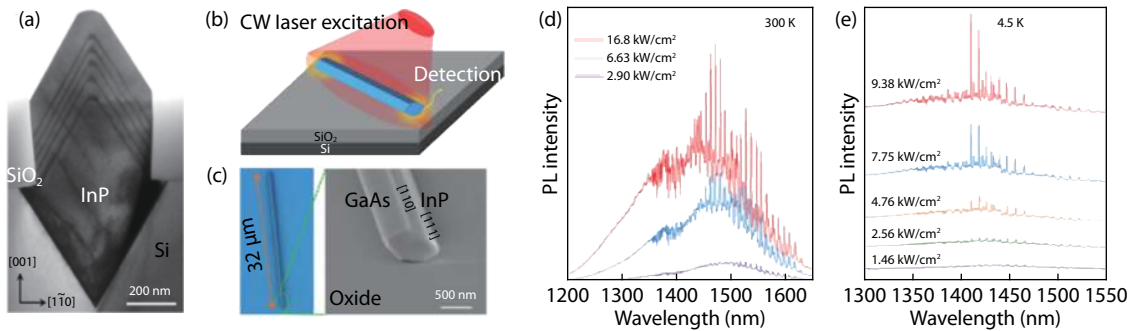


Fig. 10. (Color online) (a) Cross-sectional TEM image of one representative InP/InGaAs nanoridge on (001) Si. (b) Schematic of the transferred InP/InGaAs nanoridge on a SiO₂/Si substrate. (c) Microscopic image and SEM of the transferred InP/InGaAs nanoridge. (d) PL spectra of the transferred InP/InGaAs nanoridge under different excitation levels. (e) Emission spectra of the InP/InGaAs nanoridge at increasing excitation levels at 4.5 K.

Researchers have carried out many experiments and used many methods in order to achieve light pump illumination. The research team at Gent University and IMEC in Belgium has done a lot of research in this area. They used the ART method to directly grow high-quality InP nanowires outside the Si substrate with periodic V-grooves and SiO₂ sidewalls and fabricated DFB laser arrays in 2015. They achieved light pump lasing at room temperature. Since the gain material is only InP, its lasing wavelength is about 920 nm^[66], as shown in Fig. 9(a). In the following year, the team further epitaxially grew a layer of InGaAs and a very thin InP cap layer on the top of the InP, and fabricated the DFB laser of the optical pump using the same process to make the lasing wavelength reach approximately 1.3 μm^[67], as shown in Fig. 9(b). In the same year, the team attempted to grow GaAs outside a silicon V-groove using a similar epitaxial method. Due to the different growth rates of different crystal planes, when there is no sidewall limitation, the (100) plane is gradually formed on the

top of the GaAs. The team continued to grow the multi-quantum well structure of InGaAs/GaAs and measured fluorescence around 1.1 μm at room temperature^[68], as shown in Fig. 9(c).

Researchers at the Hong Kong University of Science and Technology used another way to achieve the light pump. They grew InP/InGaAs nanoridges on Si substrates, transferring InP/InGaAs nanoridges onto SiO₂/Si substrates, and observed the Fabry-Perot resonance mode at room temperature, and achieving 1400 nm multimode lasing behavior under continuous wave optical pumping at 4.5 K^[69], as shown in Fig. 10.

In previous studies, researchers found that the refractive index of silicon is larger than that of III-V materials such as InP, GaAs, and InGaAs. The light field generated by the III-V material will continuously leak into the silicon substrate, so it cannot form the guided wave mode that can propagate, and it cannot form a resonant cavity. In 2019, the researchers

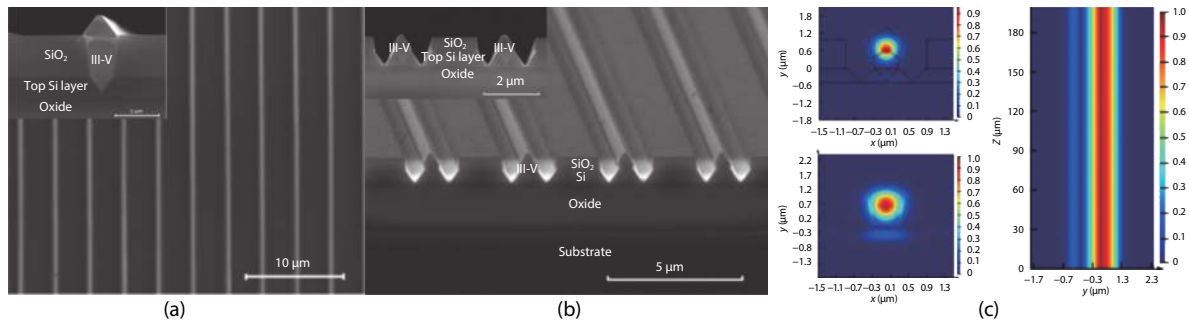


Fig. 11. (Color online) (a) SEM image of III-V nanowires on the SOI substrate. (b) SEM images of III-V nanowires on the SOI substrate after etching. (c) The FDTD simulation results of a III-V nanowire on the SOI substrate after etching.

found that after removing the silicon around the III-V nanowires (bottom), the entire III-V nanowires were wrapped in air, and the refractive index of the air was approximately 1, which was much smaller than the III-V material. This structure has a good limit on light and can form a guided wave mode to provide optical gain^[70], as shown in Fig. 11.

ART technology is still in the laboratory stage, and there is still a long way to go for large-scale applications. The materials grown by ART technology are now only optically pumped^[71], and the next major task is to achieve electric pumping. Further research is required to perform electric pumping on a large scale.

3. Conclusion

III-V compound materials and lasers on Si substrates is a rapidly evolving research field with tremendous potential. Direct epitaxial quantum dot lasers have been able to electrically pump lasers at room temperature. Bonded lasers have already been put into commercial use. High quality III-V compound materials can be grown with ART technology. These all show the possibility of combining with traditional CMOS technology, which can be used to make high-speed communication networks in the future.

Acknowledgments

This work was supported by the National Key Technology R&D Program (Grant No. 2018YFA0209001) and Frontier Science Research Project of CAS (Grant No. QYZDY-SSW-JSC021).

References

- [1] Kim S, Yokoyama M, Taoka N, et al. Self-aligned metal source/drain In_xGa_{1-x}As n-metal-oxide-semiconductor field-effect transistors using Ni-InGaAs Alloy. *Appl Phys Lett*, 2011, 98(24), 21
- [2] Noda H, Murai F, Kimura S. Threshold voltage controlled 0.1-μm MOSFET utilizing inversion layer as extreme shallow source/drain. International Electron Devices Meeting, 1993
- [3] Lee C G, Wang X D, Kysar J W, et al. Measurement of the elastic properties and intrinsic strength of monolayer graphene. *Science*, 2008, 321(5887), 385
- [4] Geim A K, Novoselov K S. The rise of graphene. *Nat Mater*, 2009, 6, 183
- [5] Coldren L A, Corzine S W, Mashanovitch M L. Diode lasers and photonic integrated circuits. Wiley, 1995
- [6] Almeida V R, Barrios C A, Panepucci R R, et al. All-optical control of light on a silicon chip. *Nature*, 2004, 431(7012), 1081
- [7] Michel J, Liu J, Kimerling L C. High-performance Ge-on-Si photo-detectors. *Nat Photonics*, 2000, 4(8), 527
- [8] Sun C, Wade M T, Lee Y, et al. Single-chip microprocessor that communicates directly using light. *Nature*, 2015, 528(7583), 534
- [9] Vlasov Y, Green W M J, Xia F J. High-throughput silicon nanophotonic wavelength-insensitive switch for on-chip optical networks. *Nat Photonics*, 2008, 2(4), 1
- [10] Wesołowski K. Introduction to digital communication systems. Wiley, 2009
- [11] Won R, Paniccia M J. Integrating silicon photonics. *Nat Photonics*, 2010, 4(8), 498
- [12] Andrew L, Qi J, Mingchu T, et al. Continuous-wave InAs/GaAs quantum-dot laser diodes monolithically grown on Si substrate with low threshold current densities. *Opt Express*, 2012, 20(20), 22181
- [13] Bringans R D, Biegelsen D K, Swartz L. Atomic-step rearrangement on Si(100) by interaction with arsenic and the implication for GaAs-on-Si epitaxy. *Phys Rev*, 1991, 44(7), 3054
- [14] Chen S, Li W, Wu J, et al. Electrically pumped continuous-wave III-V quantum dot lasers on silicon. Semiconductor Laser Conference, 2016
- [15] Mori H, Tachikawa M, Sugo M, et al. GaAs heteroepitaxy on an epitaxial Si surface with a low-temperature process. *Appl Phys Lett*, 1993, 63(14), 1963
- [16] Sakai S, Soga T, Takeyasu M, et al. Room-temperature laser operation of AlGaAs/GaAs double heterostructures fabricated on Si substrates by metalorganic chemical vapor deposition. *Appl Phys Lett*, 1986, 48(6), 413
- [17] Tang M, Chen S, Jiang W, et al. Optimisation of 1.3-μm InAs/GaAs quantum-dot lasers monolithically grown on Si substrates. Semiconductor Laser Conference, 2014
- [18] Ting S M, Fitzgerald E A. Metal-organic chemical vapor deposition of single domain GaAs on Ge/Ge_xSi_{1-x}/Si and Ge substrates. *J Appl Phys*, 2000, 87(5), 2618
- [19] Windhorn T H, Metzger G M, Tsaur B Y, et al. AlGaAs double-heterostructure diode lasers fabricated on a monolithic GaAs/Si substrate. *Appl Phys Lett*, 1984, 45(4), 309
- [20] Takano Y, Hisaka M, Fujii N, et al. Reduction of threading dislocations by InGaAs interlayer in GaAs layers grown on Si substrates. *Appl Phys Lett*, 1998, 73(20), 2917
- [21] Asai K, Katahama H, Shiba Y. Dynamical formation process of pure edge misfit dislocations at GaAs/Si interfaces in post-annealing. *J Appl Phys*, 1994, 33(9A), 4843
- [22] Takagi Y, Yonezu H, Hachiya Y, et al. Reduction mechanism of threading dislocation density in GaAs epilayer grown on Si substrate by high-temperature annealing. *Jpn J Appl Phys*, 1994, 33(6R), 3368
- [23] Kohama Y, Kadota Y, Ohmachi Y. InP grown on Si substrates with GaP buffer layers by metalorganic chemical vapor deposition. *Jpn J Appl Phys*, 1989, 28(8), 1337
- [24] Fischer R, Kopp W, Morkoc H, et al. Low threshold laser operation

- at room temperature in GaAs/(Al, Ga)As structures grown directly on (100)Si. *Appl Phys Lett*, 1986, 48(20), 1360
- [25] Zhou X L, Pan J Q, Liang R R, et al. Epitaxy of GaAs thin film with low defect density and smooth surface on Si substrate. *J Semicond*, 2014, 35, 073002
- [26] Li Y, Giling L J. A closer study on the self-annihilation of anti-phase boundaries in GaAs epilayers. *J Cryst Growth*, 1996, 163(3), 203
- [27] Tang M, Chen S, Wu J, et al. 1.3- μm InAs/GaAs quantum-dot lasers monolithically grown on Si substrates using InAlAs/GaAs dislocation filter layers. *Opt Express*, 2014, 22(10), 11528
- [28] Sugo M, Mori H, Sakai Y, et al. Stable cw operation at room temperature of a 1.5- μm wavelength multiple quantum well laser on a Si substrate. *Appl Phys Lett*, 1992, 60(4), 472
- [29] Liu H, Wang T, Qi J, et al. Long-wavelength InAs/GaAs quantum-dot laser diode monolithically grown on Ge substrate. *Nat Photonics*, 2011, 5(7), 416
- [30] Chen S, Li W, Wu J, et al. Electrically pumped continuous-wave III-V quantum dot lasers on silicon. *Nat Photonics*, 2016, 10(5), 307
- [31] Jinkwan K, Bongyong J, Joohang L, et al. All MBE grown InAs/GaAs quantum dot lasers on on-axis Si (001). *Opt Express*, 2018, 26(9), 11568
- [32] Norman J C, Jung D, Zhang Z, et al. A review of high-performance quantum dot lasers on silicon. *IEEE J Quantum Electron*, 2019, 55(2), 1
- [33] Jung D, Herrick R, Norman J, et al. Impact of threading dislocation density on the lifetime of InAs quantum dot lasers on Si. *Appl Phys Lett*, 2018, 112(15), 153507
- [34] Liu A Y, Zhang Y C, Norman J, et al. High performance continuous wave 1.3 μm quantum dot lasers on silicon. *Appl Phys Lett*, 2014, 104(4), 041104
- [35] Zhu S, Shi B, Li Q, et al. 1.5 μm quantum-dot diode lasers directly grown on CMOS-standard (001) silicon. *Appl Phys Lett*, 2018, 113(22), 221103
- [36] Wan Y, Qiang L, Liu A Y, et al. Sub-wavelength InAs quantum dot micro-disk lasers epitaxially grown on exact Si (001) substrates. *Appl Phys Lett*, 2016, 108(22), 1
- [37] Norman J, Kennedy M J, Selvidge J, et al. Electrically pumped continuous wave quantum dot lasers epitaxially grown on patterned, on-axis (001) Si. *Opt Express*, 2017, 25(4), 3927
- [38] Isenberg J, Warta W J. Free carrier absorption in heavily doped silicon layers. *Appl Phys Lett*, 2004, 84(13), 2265
- [39] Krishnamoorthy A V, Chirovsky L M F, Hobson W S, et al. Vertical-cavity surface-emitting lasers flip-chip bonded to gigabit-per-second CMOS circuits. *IEEE Photonics Technol Lett*, 1999, 11(1), 128
- [40] Fang A W, Erica L, Kuo Y H, et al. A distributed feedback silicon evanescent laser. *Opt Express*, 2008, 16(7), 4413
- [41] Fang A W, Hyundai P, Oded C, et al. Electrically pumped hybrid AlGaInAs-silicon evanescent laser. *Opt Express*, 2006, 14(20), 9203
- [42] Fang A W, Koch B R, Jones R, et al. A distributed Bragg reflector silicon evanescent laser. *IEEE Photonics Technol Lett*, 2008, 20(20), 1667
- [43] Groote A D, Cardile P, Subramanian A Z, et al. Transfer-printing-based integration of single-mode waveguide-coupled III-V-on-silicon broadband light emitters. *Opt Express*, 2016, 24(13), 13754
- [44] Hyundai P F, Alexander F K, Satoshi K, et al. Hybrid silicon evanescent laser fabricated with a silicon waveguide and III-V offset quantum wells. *Opt Express*, 2005, 13(23), 9460
- [45] Justice J, Bower C, Meitl M, et al. Wafer-scale integration of group III-V lasers on silicon using transfer printing of epitaxial layers. *Nat Photonics*, 2012, 6(9), 612
- [46] Pasquariello D, Hjort K J. Plasma-assisted InP-to-Si low temperature wafer bonding. *IEEE J Sel Top Quantum Electron*, 2002, 8(1), 118
- [47] Keyvaninia S, Verstuylt S, Van Landschoot L, et al. Heterogeneously integrated III-V/silicon distributed feedback lasers. *Opt Lett*, 2013, 38(24), 5434
- [48] Sui S, Tang M T, Yang Y, et al. Sixteen-wavelength hybrid AlGaInAs/Si microdisk laser array. *IEEE J Quantum Electron*, 2015, 51, 2600108
- [49] Andrijasevic D, Austerer M, Andrews A M, et al. Hybrid integration of GaAs quantum cascade lasers with Si substrates by thermocompression bonding. *Appl Phys Lett*, 2008, 92(5), 157
- [50] Yuan L, Tao L, Yu H, et al. Hybrid InGaAsP-Si evanescent laser by selective-area metal-bonding method. *IEEE Photonics Technol Lett*, 2013, 25(25), 1180
- [51] Yuan L, Tao L, Chen W, et al. A buried ridge stripe structure InGaAsP-Si hybrid laser. *IEEE Photonics Technol Lett*, 2015, 27(4), 352
- [52] Hong T, Wang Y, Yu H Y, et al. A Selective area metal bonding method for Si photonics light sources. *IEEE International Conference on Group IV Photonics*, 2010
- [53] Yu H, Yuan L, Tao L, et al. 1550 nm evanescent hybrid InGaAsP-Si laser with buried ridge stripe structure. *IEEE Photonics Technol Lett*, 2016, 28(10), 1146
- [54] Langdo T A, Leitz C W, Currie M T, et al. High quality Ge on Si by epitaxial necking. *Appl Phys Lett*, 2000, 76(25), 3700
- [55] Li Q, Han S M, Brueck S R J, et al. Selective growth of Ge on Si(100) through vias of SiO₂ nanotemplate using solid source molecular beam epitaxy. *Appl Phys Lett*, 2003, 83(24), 5032
- [56] Matyi R J, Shichijo H, Tsai H L, et al. Patterned growth of gallium arsenide on silicon. *J Vac Sci Technol B*, 1988, 6(2), 699
- [57] Woodbridge K, Barnes P, Murray R, et al. GaAs / AlGaAs pin MQW structures grown on patterned Si substrates. *J Cryst Growth*, 1993, 127(1-4), 112
- [58] Park J S, Bai J, Curtin M, et al. Defect reduction of selective Ge epitaxy in trenches on Si(001) substrates using aspect ratio trapping. *Appl Phys Lett*, 2007, 90(5), 3344
- [59] Li J Z, Bai J, Park J S, et al. Defect reduction of GaAs epitaxy on Si (001) using selective aspect ratio trapping. *Appl Phys Lett*, 2007, 91(2), 2293
- [60] Li S, Zhou X, Kong X, et al. Evaluation of growth mode and optimization of growth parameters for GaAs epitaxy in V-shaped. *J Cryst Growth*, 2015, 426, 147
- [61] Li S Y, Zhou X L, Kong X T, et al. Selective area growth of GaAs in V-grooved trenches on Si (001) substrates by aspect-ratio. *Chin Phys Lett*, 2015, 32, 028101
- [62] Wang G, Leys M R, Loo R, et al. Selective area growth of high quality InP on Si (001) substrates. *Appl Phys Lett*, 2010, 97(12), 1
- [63] Paladugu M, Merckling C, Loo R, et al. Site selective integration of III-V materials on Si for nanoscale logic and photonic devices. *Cryst Growth Des*, 2012, 12(10), 4696
- [64] Li S, Zhou X, Kong X, et al. Catalyst-free growth of InP nanowires on patterned Si (001) substrate by using GaAs buffer layer. *J Cryst Growth*, 2016, 440, 81
- [65] Li S, Zhou X, Li M, et al. Ridge InGaAs/InP multi-quantum-well selective growth in nanoscale trenches on Si (001) substrate. *Appl Phys Lett*, 2016, 108(2), 021902
- [66] Wang Z, Tian B, Pantouvaki M, et al. Room-temperature InP distributed feedback laser array directly grown on silicon. *Nat Photonics*, 2015, 9(12), 837
- [67] Tian B, Merckling C, Thourhout D V, et al. Room temperature InGaAs/InP distributed feedback laser directly grown on silicon. *Lasers & Electro-optics*, 2016
- [68] Kunert B, Guo W, Mols Y, et al. III/V nano ridge structures for optical applications on patterned 300 mm silicon substrate. *Appl Phys Lett*, 2016, 109(9), 511
- [69] Han Y, Li Q, Zhu S, et al. Continuous-wave lasing from InP/InGaAs

- nanoridges at telecommunication wavelengths. [Appl Phys Lett, 2017, 111\(21\), 212101](#)
- [70] Li Y, Wang M, Zhou X, et al. InGaAs/InP multi-quantum-well nanowires with a lower optical leakage loss on V-groove-patterned SOI substrates. [Opt Express, 2019, 27\(2\), 494](#)
- [71] Han Y, Ng W K, Xue Y, et al. Telecom InP/InGaAs nanolaser array directly grown on (001) silicon-on-insulator. [Opt Lett, 2019, 44\(4\), 767](#)