REVIEWS

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Recent advances of heterogeneously integrated III–V laser on Si

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Abstract: Due to the indirect bandgap nature, the widely used silicon CMOS is very inefficient at light emitting. The integration of silicon lasers is deemed as the 'Mount Everest' for the full take-up of Si photonics. The major challenge has been the materials dissimilarity caused impaired device performance. We present a brief overview of the recent advances of integrated III–V laser on Si. We will then focus on the heterogeneous direct/adhesive bonding enabling methods and associated light coupling structures. A selected review of recent representative novel heterogeneously integrated Si lasers for emerging applications like spectroscopy, sensing, metrology and microwave photonics will be presented, including DFB laser array, ultra-dense comb lasers and nanolasers. Finally, the challenges and opportunities of heterogeneous integration approach are discussed.

Key words: heterogeneous integration; lasers; silicon photonics; integrated circuits

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1. Introduction

By exploiting mature and standard microelectronics CMOS processes, silicon photonics[1, 2] have been booming with rapidly and widely commoditized silicon photonics integrated circuits (PICs) in various passive photonic devices[3], electro-optic modulators[4, 5], or photodetectors[6], etc. thanks to the high-yield, low fabrication cost, low power consumption and compact footprint to co-integrate photonic and microelectronic components together[2, 7]. However due to their inherent nature of indirect bandgap, full-scale application of silicon photonics in industry is still hampered by absence of directly integrated light sources and the famed silicon laser enigma has been in the spotlight over last 20 years. Nowadays the chip level convergence of optics and electronics is becoming a necessity for the next-generation processors and data communications with high dense intra- and inter-chip interconnections in Si photonics, cost-efficient and technically viable integration of high-performance III–V light sources into silicon PICs are drawing enormous attention. Such light sources should combine both low power consumption and high efficiency with a compact footprint, good optical coupling and thermal dissipation while maintaining low cost and large-scale manufacturability. Intensive research progress has been made to the realization of integrating electrically-pumped III–V lasers in Si photonics, in which the monolithic integration, hybrid integration and heterogeneous integration have been considered as competitive solutions.

Recently, substantial efforts have been devoted toward light sources on Si by monolithic integration or hybrid integration. Monolithically integrated on-chip light sources are regarded to be the ultimate goal of silicon lasers, as the epitaxial growth may realize the high-density integration of lasers in Si photonics economically if the CMOS compatibility could be well solved. Because of the dissimilarity between III–V and group IV materials however, there are several fundamental challenges such as the threading dislocations (TDs), anti-phase boundaries (APBs) and different coefficient of thermal expansion. The TDs are due to the large lattice constant mismatch (i.e. 8% for InP/Si and 4% for GaAs/Si) which could result in strain on the epilayer that render poor quality of III–V materials and also compromise the device performance; The APBs caused by the polar (III–Vs) and nonpolar (Si substrates) property could form the electrically charged planar defects acting as non-radiative recombination centers and current leakage paths for optoelectronic devices; The thermal coefficient gap however will create the thermal cracks between epilayers that preventing thicker III–Vs layers grown on Si. Recently, III–V quantum dot (QD) material has revolutionized monolithic integration of III–V light sources on Si over quantum well (QW) counterparts as being less sensitive to defects and temperature[8–10], highlighting the very exciting results of high output power, low threshold current densities and much longer lifetime, also the benefits of smaller parasitic capacitances, and a recent good review paper can be found at Ref. [11]. However, it is still in the early stage of research, and the fabrication process is not mature, besides, the material quality and laser reliability still need to be improved. Hybrid integration on the other hand, relies on optically connecting pre-fabricated known-good III–V lasers by flip-chip mounting either on top of or next to the silicon PICs. This approach could maintain the superior performance characteristics of native GaAs or InP substrate light sources and allow devices to be tested before system assembly. However, the pitch density and the size of the bumps limit the integration density, also the accurate alignment between III–V lasers and silicon waveguides could be very challenge as the expensive and slow active alignment techniques should be deployed to make possible the precision in the micrometer or sub-micrometer range. In practice, this approach need to monitor the coupling efficiency

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Table 1. Overall comparison between different III–V lasers integration strategies on silicon.

Technology	Integration density	Cost/CMOS compatibility	Complexity/Maturity
Monolithic integration	Potentially high	Potentially low/No	Early R&D
Hybrid integration	Low	High/No	Low/High
Direct bonding	Medium	Medium/No	High/Medium
Adhesive bonding	Medium	Medium/No	Low/Medium

continuously while optimizing the position of the devices, and some additional passive devices (microlenses, prisms, etc) may also be needed to accommodate the size differences of mode field. Normally the optical coupling losses are above 2 dB between III–V laser array to an silicon waveguide array with trident spot-size converters using butt coupling, and the alignment tolerance is about ~1 μm[12].

Heterogeneous integration, referring to III–V gain material on die/wafer-level or even complete devices transferred to Si substrates via a variety of chemical or physical bonding techniques, such that light generated in the III–V epitaxial layers is evanescently coupled into silicon circuits vertically. Compared with monolithic integration, this approach has much higher tolerance in lattice mismatch, and combines the excellent III–V light sources and superior Si passive waveguide components together. On the other hand, the clear advantage over hybrid integration lies in that no stringent positioning alignment is necessary. In general, heterogeneous integration approach could utilize the highly precise lithography to process III–V thin films and align the III–V gain devices with underneath bonded wafer-level SOI circuit, enabling potentially lower cost and high density of integration, is now considered as the most feasible way toward efficient Si laser integration. Heterogeneous integration itself can be differentiated by direct bonding or indirect bonding in terms of whether an insertion layer is applied. Indirect bonding is mainly including metals or polymers such as divinylsiloxane-benzocyclobutane (DVS-BCB) to perform the adhesives in between. A good review of heterogeneous integration Si laser is recently published in Ref. [13].

The overall comparison among the different III–V lasers integration methods on silicon are summarized in Table 1.

In this review paper, recent demonstrated heterogeneous integration of III–V lasers on Si will be presented with a special focus on direct/adhesive bonding enabling procedures. We will start by introducing the main bonding technologies, followed by the optical coupling structures for III–V/Si light routing. Then we will review the latest advance of heterogeneously integrated III–V lasers on Si, including DFB laser array, comb laser and one-dimensional (1D) photonic crystal cavity (PhC) laser. In the final section, we will have a discussion and summary.

2. Bonding technology

By combining known-good III–V epitaxial layer with silicon photonics via bonding technology, one can take advantage of the mature CMOS compatible processing, while maintaining utilizing III–V materials as on-chip light sources and allowing wafer-scale processing of devices after bonding.

2.1. Direct bonding

Direct bonding is a technique that brings stringently polished, flat and clean wafers or dies preparation into contact for integration. The general fabrication process to improve the bonding strength is rather complex, including the ultraclean conditions and atom-scale smooth surfaces. Besides, the high-temperature SOI processing (> 600 °C) will greatly damage the III–V wafer during manufacturing process, so special procedure is required to strictly prohibit a high-temperature anneal[14]. A low-temperature annealing method (< 400 °C) has been investigated by introducing O_2 plasma or SiO_2 covalent[15] surface treatment, which facilitates the creation of OH-bonds after the removal of the native oxide layer and enables strong van der Waals force or covalent bonds between III–Vs and SOI wafers up to 300 mm, is now emerging as an attractive approach. The O_2 plasma-assisted and SiO_2 covalent wafer bonding process flow are shown in Fig. 1 and summarized below:

1. Hydrophobic surfaces clean: Prepare samples to remove the native oxide in standard buffered HF solution (SOI) or 39% NH_4OH (InP).

2. O_2 plasma treatment: Prepare samples in an O_2 plasma surface treatment to grow an ultra-thin (~15 nm) plasma oxide layer with smooth (RMS roughness < 0.5 nm) hydrophilic surfaces. Especially, the O_2 energetic ion bombardment can efficiently remove hydrocarbons and water attached dirties on the sample surface.

3. SiO_2 covalent bonding: Deposit SiO_2 using PECVD on both surfaces or thermally grow SiO_2 on Si to clean the hydrophilic surface. Employ chemical mechanical polishing (CMP) to improve surface topography and make sure the surface RMS roughness less than 1 nm.

4. Activation process: Passivate the two surfaces with a high density of polar hydroxyl groups (–OH), bridge bonds between the mating surfaces, enable spontaneous bonding at room temperature. O_2 plasma-treated samples are dipped in deionized water and blow-dried or placed in a vaporized NH_4OH environment. Thick SiO_2-covered samples are boiled in diluted RCA-1 solution at 75 °C for 10 min, a step to clean and form an Si–OH-passivated surface, then blow dried. Similar O_2 plasma treatment[16] and a quick dip in very dilute HF solution (0.025%) for 1 min[12, 16] can help suppress interfacial voids and enhance the ultimate bonding strength.

5. Anneal and cooling: Anneal the bonded sample at 300 °C with external coaxial pressure (1–2 MPa) for more than one hour after immediate physical mating typically in air at room temperature.

6. Selective InP substrate removal: Selectively remove the InP substrate in a 3HCl : 1H_2O solution to leave thin (< 2 μm) InP-based epitaxial layers on Si at room temperature after annealing and cooling process.

2.2. Adhesive bonding

The fabrication procedures of adhesive bonding by DVS-BCB are much more relaxed and not limited by the material dissimilarities. DVS-BCB is an excellent adhesive exhibiting good physical properties such as high bond strength, high degree of planarization, high optical clarity, good thermal stabil-

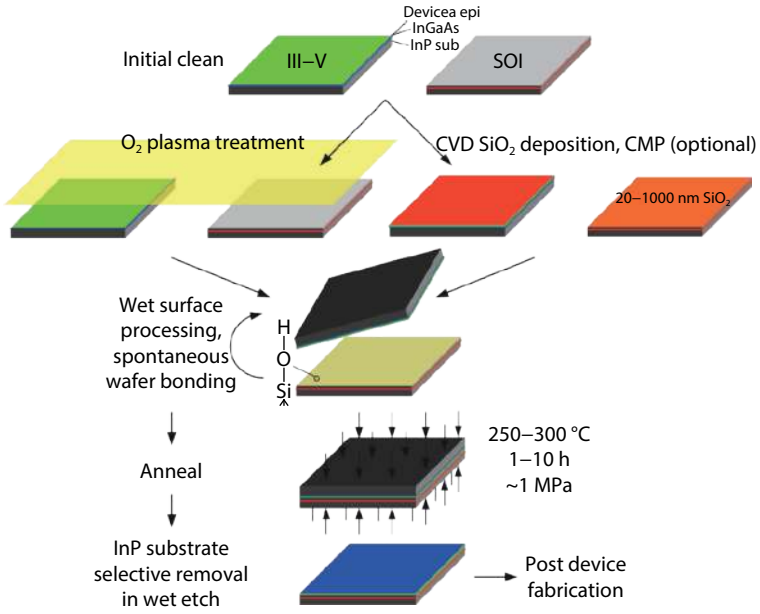

Fig. 1. (Color online) Schematic O_2 plasma-assisted and SiO_2 covalent wafer bonding process flow. Reproduced from Ref. [15].

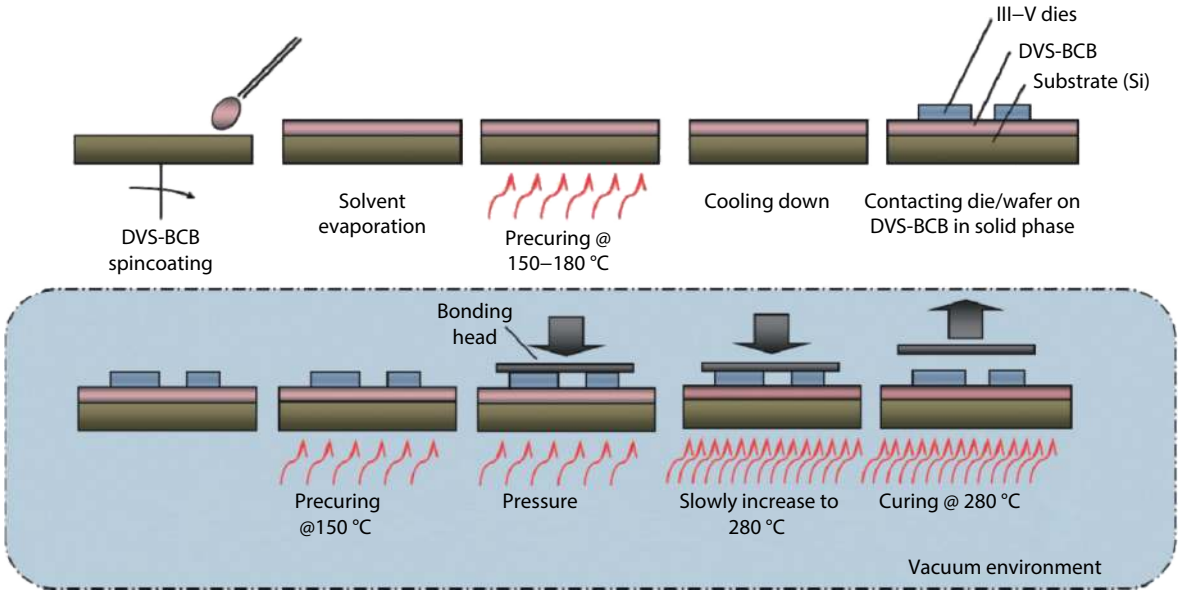

Fig. 2. (Color online) Schematic process flow for DVS-BCB adhesive bonding, referred to as "cold bonding". Reproduced from Ref. [17].

ity, low refractive index and curing temperature[13]. However, repeatable thin BCB layer for efficient light coupling and thermal dissipation is a challenge in the bonding process. A new "cold bonding" process has been developed to solve this issue[17]. In this new method, a uniform and ultra-thin bonding thickness (~50 nm) has been realized, effectively thin enough for good coupling. Accordingly, BCB-assisted adhesive bonding now has become a practical approach for the heterogeneous integration of III–V material on a SOI wafer. The adhesive bonding process is schematically depicted in Fig. 2 and summarized below :

1. Surface clean and BCB dilution: Immerse the sample into a standard clean (SC-1) solution (i.e., NH_4OH : H_2O_2 : H_2O 1 : 1 : 5) and heat for 15 min at 70 °C or by using a microwave O_2 plasma to clean the SOI. Dilute the DVS-BCB with mesitylene then spin-coated onto the SOI substrate, thin bonding layer thickness (< 50 nm) can be achieved for better coupling to the topography of the silicon PIC.

2. Pre-curing: Pre-cure the spun DVS-BCB to evaporate all the solvents and partially polymerized, thereby improving the bonding layer thickness uniformity. Afterwards, deposite a thin (< 10 nm) silicon oxide layer to improve the adhesion to DVS-BCB.

3. Substrate removal and mounting: Remove the InP/InGaAs sacrificial layer pair on the III–V wafer/die is by selective wet etching using HCl : H_2O (4 : 1) and H_2SO_4 : H_2O_2 : H_2O solutions (1 : 1 : 18), so as to removes particles and contaminants from the III–V die surface prior to bonding. Then rinse the III–V die with DI water, dry and mount on the SOI die at room temperature by using low accuracy 500 μm alignment machine or more accurately using a flip-chip machine.

4. Bonding: Bring the III–V dies into contact with the DVS-BCB coated silicon photonics substrate and load in a wafer bonder. After pumping to vacuum and heating the sample to 150 °C with a ramp of 15 °C/min for 10 min, bonding pressure between 200 to 400 kPa is applied. Then further

increase the temperature to 280 °C with a ramp of 1.5 °C/min and fully cure for one hour. After the curing, cool down the bonded samples (at 6–10 °C/min) and unload from the processing chamber.

5. Post processing: Remove the III–V substrate by grinding or by a selective wet etching using HCl. Transfer the III–V membrane to a Si sample with the functional layers bonded to the SOI die to get ready for further processing.

The adhesive bonding is very versatile due to the much simpler bonding process, virtually can apply to any compound semiconductor. Multiple die bonding and full wafer bonding have been already demonstrated[17] with ultra-thin BCB layer for the coupling between III–V gain material and silicon waveguide. Since the adhesive BCB can planarize the surface, interface roughness requirements are relaxed, and the cleanliness requirements are not that strict, which lead to a significant reduction in the bonding preparation workload. Attributed to low volume shrinkage and low-temperature operation of the adhesive, the DVS-BCB also has the advantages of high bonding strength and void-free bonds, reducing the risk of III–V layer damage[17]. The largest disadvantage of DVS-BCB adhesive bonding however is probably the low thermal conductivity that generates a high thermal resistance[17], which degrades the laser performance at high operation temperature. Hence the heat dissipation should be addressed in this approach in applications. The comparison of the direct bonding and DVS-BCB adhesive bonding is summarized below in Table 2.

Table 2. General characteristics of direct bonding and adhesive bonding.

Bonding characteristics	Direct bonding	Adhesive bonding
Surface roughness tolerance	Low	High
Bonding strength	High	High
Bonding induced strain	Low	Low
Integration density and uniformity	High	Medium high
Complexity	Medium	Low
Stability	High	High
Scalability	High	High

3. Coupling structures

For heterogeneous integration of Si laser, there are several important requirements like the low coupling loss, small footprint and an overall high assembly yield, along with the low cost and large-scale production capability. Among various Si/III–V heterogeneously integrated devices by employing direct and adhesive bonding technologies, a common criterion is how to design a compact yet efficient light coupling structure to transfer the optical mode from an active III–V light sources to a silicon photonic circuits. There have been several coupling methods, including vertical[18] and lateral directional couplers[16], grating-assisted coupler[19] or an adiabatic coupler[20–22]. From the mode coupling theory, for directional coupler, the coupling length must be beta matched so that the modes from the incident waveguide can completely couple into a superposition of modes of the other waveguide, which is difficult between III–V and Si waveguides with dissimilar refractive index. The directional couple is also very sensitive to wavelength variations introduced by design inaccuracy or fabrication error, render it not a practical method. Grating-assisted coupler however can achieve high coupling coefficients with higher tolerance, but bandwidth is limited due to the Bragg grating conditions.

From the theory of coupled waveguides, the adiabatic coupler doesn't rely on evanescent tails, but by using taper that transforms the modes into supermodes of two or more coupled waveguide system instead[23–25]. The mode evolution is shown in Figs. 3(a) and 3(b), the supermodes power transferring from the upper amplifying III–V section to the lower silicon waveguide is caused by the adiabatic widening of the silicon waveguide. By designing the coupling structure with tailoring the waveguide width to form the even or odd supermodes of the coupled system, the optical energy is confined to either the silicon or to the III–V waveguide, as shown in Figs. 3(c) and 3(d), in this way, the III–V waveguide for gain, the slilicon waveguide for passive routing and output coupling component waveguides can be optimized separately with much relaxed tolerance and also could be extremely broadband. This methodology can be extended straightforward to couple light from III–V laser source to strip silicon waveguide and is now developped as the mainstream coupling structure.

Typical inverted adiabatic taper coupling structure design in a heterogeneously integrated distributed feedback (DFB) Si laser has been exploited[22]. The design of the gain and underneath Si coupling section is schematically illustrated in Fig. 4(a). High efficiency and large optical bandwidth coupling between the III–V membrane layer and the silicon waveguide layer have been well realized by the adiabatic inverted taper coupler I and II. Firstly, the III–V waveguide (2 or 3 μm wide) provides optical gain and confine the optical mode by etching through the active layer for the n-type contact access. Then in the section Taper I the III–V mesa width is tapered more abruptly from 2 or 3 μm to 900 nm over 30 or 50 μm respectively. In the Taper II, the width of the III–V mesa is tapered from 900 to 300 nm, while the silicon rib waveguide underlying is tapered from 300 nm to 1 μm over 150 μm. Finally, the light is guided by the 400 nm silicon rib waveguide after the coupling region. A low-loss 400 to 220 nm waveguide transition with taper length of 30 μm and tip width of 100 nm is used for transferring light to the standard 220 nm silicon device layer. High coupling efficiency over 95% and low power reflection are achieved as shown in Fig. 4(b). Single-facet output power coupled to a silicon waveguide is 14 mW at around 1550 nm with 50 dB side-mode suppression ratio (SMSR) and continuous wave (CW) operation up to 60 °C.

Although the adiabatic tapered couplers have been proved to be robust, high efficient and broadband[21, 22, 26–28], the relative long coupling length (CL) from tens to hundreds microns hampered the integration level and miniaturization of PIC. In order to densely integrate the III–V semiconductors with the Si PICs, researchers from Shanghai Jiao Tong University[29] have optimized the adiabatic taper structure and also propose two novel coupler structures based on slot and subwavelength grating (SWG) waveguides as shown in Fig. 5. According to the perturbation theory, the optical field propagation in a perturbed dielectric structure can be described by

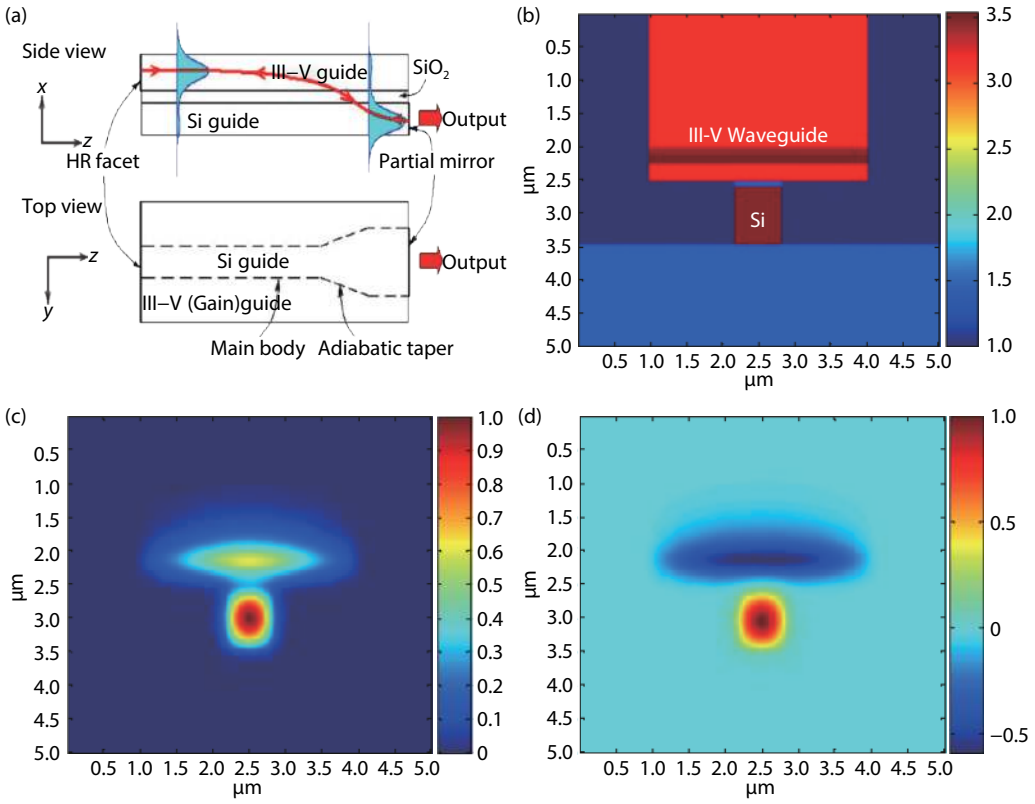

Fig. 3. (Color online) (a) Side view of the proposed hybrid laser structure and the evolution of the lasing supermode power transfer between the upper amplifying III–V section and adiabatic tapered lower silicon waveguide. (b) Refractive index profile of the coupled system. (c) Even supermode of the coupled system (at the phase-matching point). (d) Odd supermode of the coupled system (at the phase-matching point). Reproduced from Refs. [23, 24].

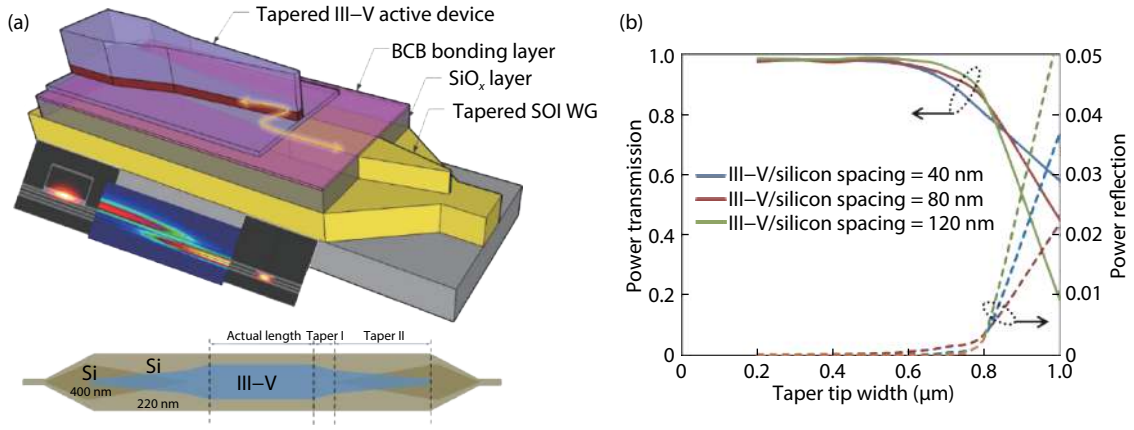

Fig. 4. (Color online) (a) Three-dimensional view of the coupling structure in the gain section with representative mode profiles in two cross-sections. (b) Coupling power transmission and reflection. Reproduced from Ref. [21].

the coupled mode theory. When the gap between two waveguides is small enough, one waveguide mode can be coupled into another mode due to the overlapping of the evanescent waves, and the amplitude of different waveguide modes along the propagation direction are determined by a set of mode coupling Eqs. (1)–(3)[30], where A, B and β_a, β_b are the optical mode amplitudes and propagation constants of waveguide a and b, respectively. κ_{ab} and κ_{ba} represent the coupling coefficients.

$$\frac{dA}{dz} = -i\kappa_{ab}Be^{i2\delta z}, \tag{1}$$

$$\frac{dB}{dz} = -i\kappa_{ba}Ae^{-i2\delta z}, \tag{2}$$

$$2\beta = \beta_a - \beta_b. \tag{3}$$

Through theoretically analysis, the optical mode coupling process between Si taper and III–V first section without p-InP layer determines the final coupling efficiency. The SOI chip and III–V materials are bonded through a 50 nm thick BCB layer. The Si coupler width shrinks from 600 to 150 nm at the length of 3 μm. Upon the Si taper, the width of n-InP taper increases from 1 to 2 μm, and the widths of tapered

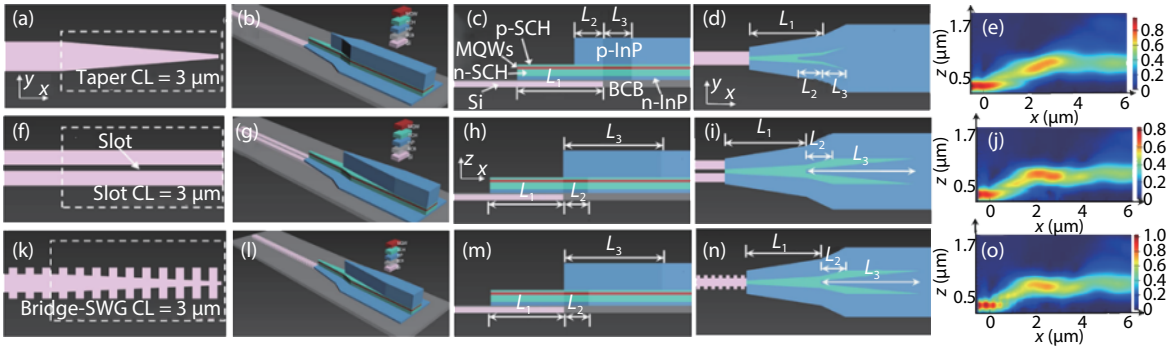

Fig. 5. (Color online) Schematics of heterogeneous integration of Si waveguides and III–V laser sources through (a)–(d) taper coupler, (f)–(i) slot coupler and (k)–(n) bridge-SWG coupler. (e), (j) and (o) Mode transformation from Si taper waveguide, Si slot waveguide, Si bridge-SWG waveguide to III–V lasers, the coupling ranges are from 0 to 4 μm, 0 to 5.5 μm, 0 to 5 μm, respectively. Reproduced from Ref. [29].

SCH and MQW layers are all from 150 to 500 nm.

In their design, the multistep or complex shape tapered structure is chosen to reduce the CL as shown in Fig. 5. The optimized III–V tapered coupler consists of three sections. The first section (L_1) is a vertical coupler, and partially covered with a 1 μm tapered p-InP layer (L_2) which is the second section. The third section is a 1 μm long tapered III–V materials (L_3). These three coupling structures possess excellent compactness which is highly demanded for Si PIC, the entire CL is only 4 μm for taper coupler (Figs. 5(a)–5(d)), 5.5 and 5 μm for slot coupler (Figs. 5(f)–5(i)) and bridge-SWG coupler (Figs. 5(k)–5(n)) respectively. These couplers are the most compact compared with other state-of-the-art couplers. In addition, high efficiency and high fabrication tolerance can be achieved at the same time. For such short couplers, the fundamental TE mode coupling efficiency can still reach 93.7% and 95.5% for slot and bridge-SWG couplers at the wavelength of 1550 nm, respectively. Especially for the bridge-SWG coupler, the fundamental TE mode coupling efficiency can maintain higher than 90% in 100 nm wavelength range when the Si taper tip width varies from 100 to 200 nm. These ultra-compact couplers, which can be practically fabricated by existing technology, also exhibit outstanding fabrication tolerances.

4. New advances in bonding based heterogeneous integration technologies

For heterogeneous integrated Si lasers, the ability to change structures of both III–V components plus the additional degree of optimizing the bonded silicon/III–V cross-section have greatly enhanced the overall performance. Compared with monolithic III–V lasers on PICs which has significant incident photon density flux on exposed III–V facets, heterogeneously integrated active components have no related degradation mechanisms hence can greatly improve their reliability by minimizing III–V facet. Various structures of heterogeneously integrated III–V components on silicon platform have been demonstrated with continuously improved performance comparable or even better than their native III–V counterparts with more complex PICs over the past decade, some previous intensive reviews can be found in Refs. [28, 31, 32], here we give an overview of recent advances of the heterogeneous integrated Si lasers, including III–V DFB array, III–V comb laser and III–V PhC nanolasers on Si for emerging applications like spectroscopy, sensing, metrology and microwave photonics.

4.1. III–V DFB laser array on Si

Due to efficient phase shift, single wavelength mode and low spectral Lorentzian linewidth, various DFB lasers on heterogeneous silicon photonics platform have been studied since the first demonstration[33], following with different targeted applications[22, 27, 34] in data interconnects and passive optical networks. InP DFB laser bonded on SOI with ultrafast modulation speed of 56 Gb/s using direct and electro-absorption modulation has been recently demonstrated, exceeding the bandwidth of commercially available InP modules (40 Gb/s)[35].

Apart from traditional applications in data communications utilizing from the near-infrared to some of mid-infrared (MIR) wavelengths (1.1–8 μm), MIR (2–20 μm) region has shown great potential for many applications including spectroscopy, thermal imaging and free-space communication[36]. Ghent University has recently demonstrated heterogeneous integration of 2.3 μm InP-based type-II quantum-well DFB lasers heterogeneously integrated with Si waveguides under CW operation at 5 °C[37]. Subsequently they demonstrated the DFB laser arrays[38]. The III–V-on-silicon DFB laser array operates in CW up to 25 °C with an on chip output power of 2.7 mW covering a broad wavelength range from 2.28 to 2.43 μm. When the III–V gain section length is reduced to 700 μm the laser array with wavelength span of 85 nm is achieved and can be tuned continuously over 3 nm. By adjusting the III–V gain section pitch, two four-wavelength DFB arrays with 10 nm continuous tuning range and 40 dB SMSR are also realized as shown in Figs. 6(d) and 6(e). This heterogeneously integrated DFB laser array makes an important step forward for the compact on-chip integrated silicon sensing system, showing great potential of portable and wearable monitoring of various chemical, biological or spectroscopic instruments.

4.2. III–V comb lasers on Si

Optical-frequency combs have revolutionized the research field of frequency metrology by connecting the radio frequency (RF) domain and the optical domain, which can precisely measure the optical frequencies by the down-conversion to the RF domain. Optical-frequency combs vision a wide range of exciting applications, including the construction of optical clocks[39], spectroscopy[40, 41]. Tremendous researches have been explored for comb generation, including

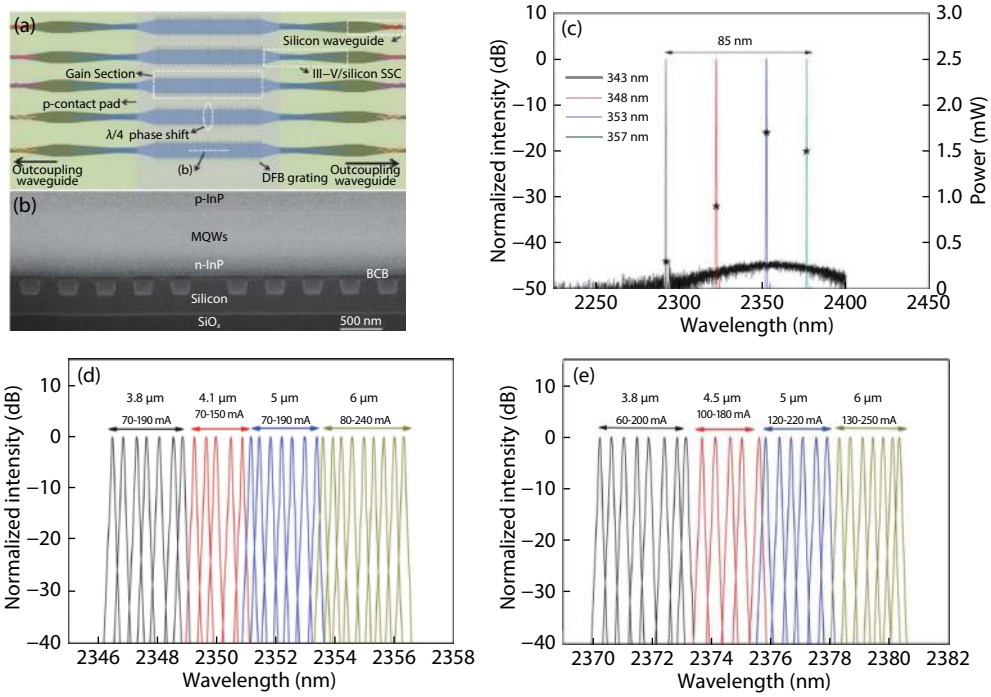

Fig. 6. (Color online) (a, b) Schematic of the III–V-on-silicon DFB laser array and SEM image of the longitudinal cross section of the gain section. (c) Normalized lasing spectra of four 700 μm long DFB lasers with a grating pitch ranging from 343 to 357 nm. (d, e) Evolution of the lasing spectra as a function of the bias current (20 mA step) for four DFB lasers with different gain section widths and silicon grating pitches of 353 nm (left) and 357 nm (right). Reproduced from Ref. [38].

mode-locked fiber/titanium-sapphire lasers, intensity modulation of a CW laser and strong nonlinear interactions[40, 42], etc, however, most of the approaches are either bulky or expensive. By leveraging high-volume semiconductor processing with advanced materials, the electrically pumped chip-scale, low-power-consumption comb source is highly desired and has been recently drawing enormous attention[42], which could inspire low-cost, low power and compact solutions. Researchers from National Institute of Standards and Technology (NIST)[43] has recently demonstrated heterogeneous III–V/Si ring-resonator laser with C-band tenability, narrow linewidth and rapid frequency control as the synthesizer. This is guided by nonlinear frequency combs on separate silicon chips and pumped by off-chip laser. The laser frequency output of the optical-frequency synthesizer can be programmed by a microwave clock across 4 THz near 1550 nm with 1 Hz resolution. The measurements verify that the output of the synthesizer is exceptionally stable (synthesis error of 7.7×10^{-15} or below).

Recently a new III–V/Si ultra-dense comb laser[44] based on the heterogeneous integration has been demonstrated as shown in Figs. 7(a)–7(c). The comb laser consists of a III–V laser integrated on the 400 nm layer thickness SOI wafer with a 30-nm thick DVS-BCB adhesive bonding layer; A length of 37.4 mm low loss (0.7 dB/cm) silicon spiral waveguide acts as the long laser cavity; Two semiconductor optical amplifiers work as the optical gain; Two silicon waveguide based distributed Bragg reflectors (DBR) perform as the two feedback mirrors. For mode-locking, the MLL is working in anti-colliding pulse mode, and a 40 μm long saturable absorber (SA) above the DBR next to the output coupler is defined to electrically isolate it from the gain sections by etching two 15-μm wide isolation slots in the III–V p-contact layer. The III–V/Si MLL is passively locked at 1 GHz with gain section biased at 91 mA and the SA reversely biased at –2.6 V. Fig. 7(d) shows the overview of the measured 5 MHz high-resolution optical spectrum with 10-dB optical bandwidth spans more than 15 nm. This optical comb contains more than 1400 phase locked lines as the line spacing of the longitudinal modes is only 1 GHz, presenting the densest comb ever generated by an integrated MLL up to date. Fig. 7(e) shows the measured RF spectrum of the pulse trains. The pure fundamental tone indicates high quality mode-locking with negligible residual amplitude modulation, and the 10-dB linewidth of the fundamental tone is measured below 900 Hz. An ultra-narrow optical linewidth below 250 kHz is also indicated as shown in Fig. 7(f). In order to function as an optical comb generator, one needs to stabilize both the repetition rate and the offset frequency of the comb. Hence the fully heterogeneously integrated comb laser in hybrid mode-locking mode, which stabilizes the repetition rate of the optical comb without negatively affecting the bandwidth and linewidth of the individual comb lines shown above, could provide unique advantages of compactness, robustness, low power consumption and low cost, which may enable cost-sensitive applications such as mobile spectroscopic analysis.

4.3. III–V PhC nano lasers on Si

Compact and energy efficient active components are very important in application like the optical interconnects on a silicon PIC. Wavelength-scale PhC resonators provide enhanced light-mater interactions and control of spontaneous emission, has exhibited the highest quality value (Q) reported over modal volume ratios, which make possible the low-threshold, thresholdless laser emission or efficient all-optical switching[45]. To attain compactness, high modulation and

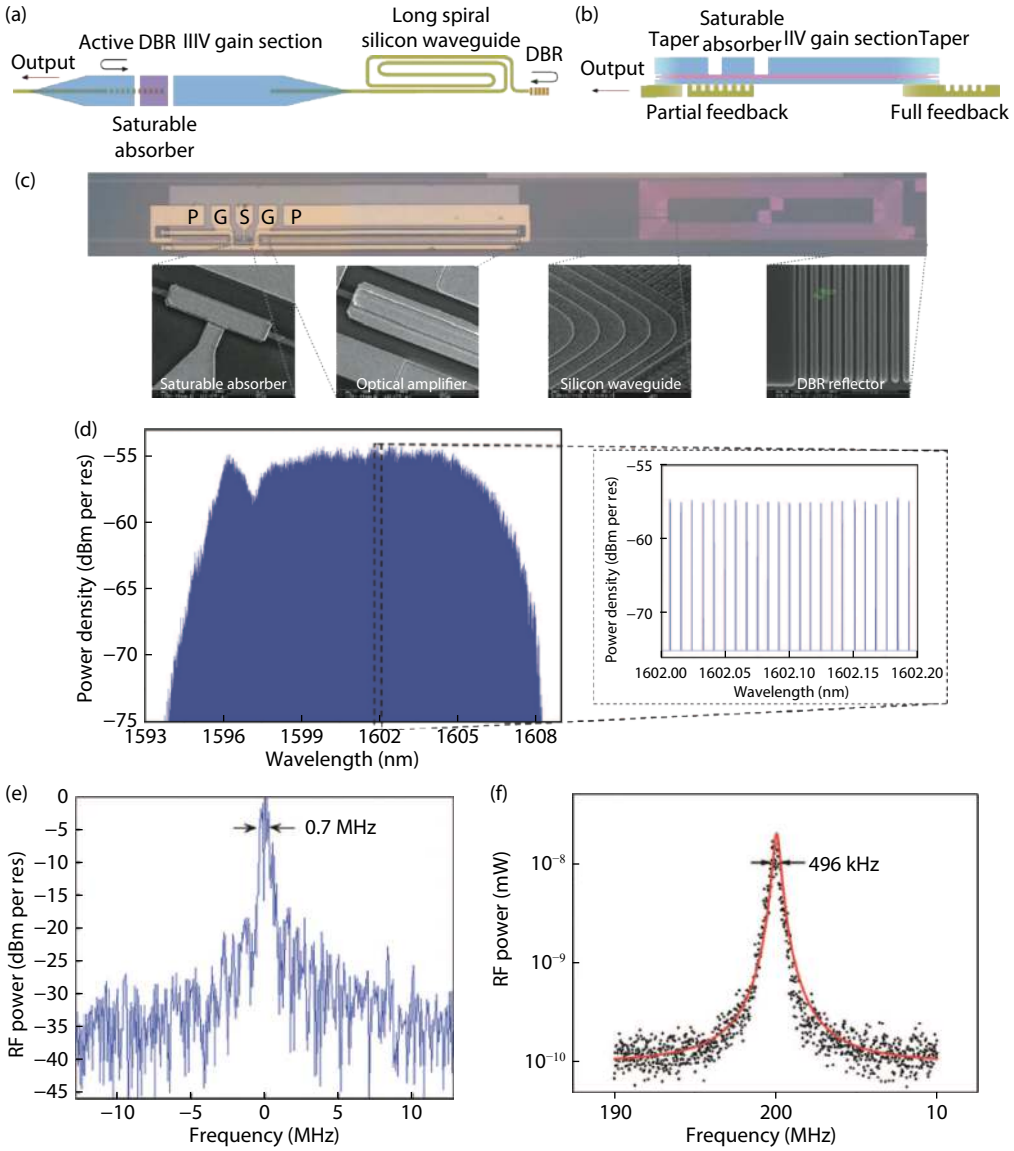

Fig. 7. (Color online) (a–c) Illustration and microscope image of the anti-colliding III–V-on-Si MLL design. (d) Optical comb generated by the passively locked 1 GHz MLL with details of evenly spaced optical modes in the comb. (e) Beat between the optical comb and the tunable laser at a wavelength of 1600 nm. (f) Measured optical linewidth of the MLL indicates an optical linewidth below 250 kHz (delayed self-heterodyne method). The black dots are the measured data, and the red curve is the corresponding Lorentzian fitting. Reproduced from Ref. [44].

power efficiency in the hybrid platform, recently exciting progress has also been made in silicon-integrated nanolasers that are different from the traditional laser configurations. High Q PhC nanocavities as active components[46–48] bonded on Si substrates have been extensively studied[49–54], with some unique properties including the unique singular density of states and photon transport within photonic bands[55]. However, the electrodes design however is very important, as the small laser size and tight localization of electromagnetic filed are difficult for efficient electrical injection due to electrodes placement, which will impair the heat dissipation, also incur unexpected large nonradiative area and optical loss[56].

Université Paris-Sud has recently reported the InP PhC lasers heterogeneously integrated on Si by BCB bonding[57]. The fabricated InP PhC nanolaser heterogeneously bonded on Si is shown in Figs. 8(a) and 8(b). The 1D PhC laser consists of a length of 15 μm III–V rib waveguide bonded on top of a 220 × 550 nm SOI waveguide by a transparent bilayer for evanescent wave coupling that composed of 40 nm BCB and 400 nm SiO_2. As shown in Figs. 8(c) and 8(d), the heterogeneously integrated laser works in CW mode at room temperature, showing a single-mode emission with over 60 dB SMSR at the wavelength of 1.56 μm. The series resistance and turn-on voltage are measured to be 1.8 kΩ and 0.75 V respectively. The threshold current is 100 μA with 9 μW output power, and a record high wall-plug and differential quantum efficiencies above 10% is demonstrated[53, 58, 59]. The heterogeneously integrated PhC III–V laser on Si laser exhibits ultracompact and power-efficient properties for electrical data to optical domain conversion, paves the way toward densely integrated optoelectronic circuits with the convergence of microelectronics and photonics.

5. Discussion and conclusion

We have reviewed the recently demonstrated heterogeneous integration of III–V lasers on Si with a special focus on direct/adhesive bonding enabling methods, coupling structures

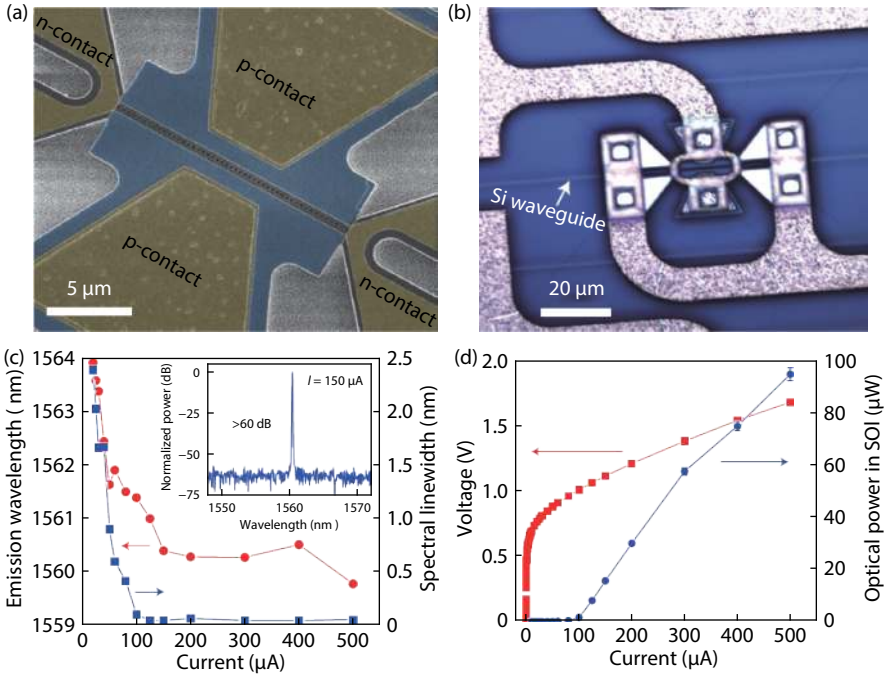

Fig. 8. (Color online) InP PhC nanolaser bonded on Si . (a) SEM image of the fabricated hybrid nanolaser after metallic contact deposition. (b) Optical microscope image of the structure in its final stage. (c) Emission wavelength and spectral linewidth against injection current at room temperature; inset: lasing spectrum at an injection current of 150 μA. (d) *L–I–V* measurements of the nanolaser at room temperature. Reproduced from Ref. [57].

for III–V/Si light routing and novel laser configurations for applications beyond traditional telecommunications. Tremendous progress in heterogeneous integration with years of extensive R&D presents opportunities for the realization of on-chip Si light sources or novel device architectures with additional functions and enhanced performance, exhibits the highest maturity combining the strengths of both III–V platform and silicon photonics platform. This approach allows wafer-scale processing of devices after bonding III–V thin films on silicon, enables potentially lower cost, greatly relaxed alignment tolerance and high density of integration. Especially the adhesive bonding could be versatile to implement on-chip light sources for a varsity of applications with the scalability for high-volume and low-cost fabrication demand. Traditional data communications with high dense intra- and inter-chip interconnections, next-generation processors and high-performance computing have been the primary drive for the development forward as the aforementioned newly demonstrated directly modulated 50 Gb/s[60], 56 Gb/s[35] heterogeneously integrated Si laser and broadband coverage DFB Si laser arrays[38]. The emerging new application scenarios such as the spectroscopy, sensing, metrology and microwave photonic applications push the research further, with some novel heterogeneous laser configurations and functionalities are being explored such as the combs lasers[42, 43] and nanolasers[54, 59, 61].

For the evolution of photonic integrated circuits, the prevailing trend that drives the evolution of PICs is higher integration density, lower cost and higher power efficiency following the performance and economic development. From research side, a number of foundries such as AIM Photonics, CEA-LETI, IMEC and IME are currently exploring this process of integrating III–V materials with CMOS scaling. The heterogeneous integration Si laser is also preferred by industry for the commercial deployment, an encouraging step of such is that Intel has released the successful silicon photonics quad small form-factor pluggable (QSFP) format transceiver in CMOS Foundry that supports 100G communications in 2016[62] as the prime example with a million units per year into data centers and 5G wireless front haul applications. Intel's 400G products are expected to enter volume production in the second half of 2019. Juniper Networks and Hewlett Packard Enterprise (HPE) are actively investing in the technology as well.

However, there are still some difficulties to overcome in heterogeneous integration that cause some degradation compared with the III–V devices on their native substrate. For direct bonding method, due to the stringent requirements of ultraclean and extremely smooth surfaces, the associated complexity is still considerable. For adhesive bonding method, the heat dissipation is challenging due to the high thermal resistance introduced by the bonding layer and the underlying buried oxide, rendering some difficulties of integrate high-density laser devices on Si chips. Although for monolithic integration method, the practical light sources, such as the electrical pumping, active-passive coupling, wafer-scale epitaxy technique and high yield and reliability still need huge efforts, it's fair to say that in the long term, monolithic integration of QD lasers on SOI platform represents the most promising integration approach for realizing reliable, power efficient, high-density integration of laser diodes on silicon chips. This may enable a major breakthrough towards the realization of large-scale, cost-effective full functional silicon photonics. Especially the V-groove growth technique that allows the co-integration of III–V and Si photonic components as well as electronic devices while avoiding thick buffer layers and non-stand-

ard wafers.

In summary, up to date, with the combination of high-quality III–V material, novel Si photonic design and advanced fabrication techniques with more efforts in R&D plus the continuing impetus from new areas of applications, heterogeneously integrated Si laser sources may extend to more interesting research areas and commercial mass-production in the near future.

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