COMMENTS AND OPINIONS

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Progress in integrating III–V semiconductors on silicon could drive silicon photonics forward

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Xinlun Cai received his PhD in Bristol University in U.K. in 2012, where he worked on design and fabrication of semiconductor ring lasers and silicon photonic devices for spatial division multiplexing. From 2012 to 2014, he worked as a postdoc in Bristol University for silicon quantum photonic devices. From 2014 to present, he worked as a full professor in Sun Yat-sen Univerisity.

Why integrating III–V semiconductor on silicon

Photonics is an enabling technology and play a significant role in today's information age. In the last few decades, starting from the fiber long haul optical communications, optical interconnects have gradually replaced copper interconnects due to its advantage of the bandwidth distance product. As photonics is moving closer and closer to the processor and memory of computers, and eventually, to on-chip level, silicon photonics becomes a viable solution for future optical interconnections due to the feasibility of high-bandwidth, high-density I/O capability and dense integration enabled by the high index contrast. More importantly, silicon photonics can leverage the complementary metal oxide semiconductor (CMOS) facilities already developed in microelectronic industry. This means it has the potential to greatly reduce the cost of photonic devices and circuits. Besides optical interconnects, silicon photonics also has applications in research in bio-sensing, spectroscopy and more exotic domains such as quantum optics and opto-mechanics. Silicon-based devices and circuits have become widely available from commercial wafer foundries, such as TSMC, IMEC and Globle Foundries.

Despite the tremendous progress have been made in the last two decades, the field of silicon photonics still faces a major challenge: the lack of an integrated efficient, reliable and electrically-pumped silicon laser. To date, most of the practical applications of silicon photonics have had to rely on external semiconductor laser sources that couple into silicon photonic chip through either optical fiber or lens, or on flip-chip integration of separately processed semiconductor laser chip. However, neither of those approaches can be scaled to very high volume production. Over the last few years, the photonic research community has made significant progress toward realizing fully integrated semiconductor lasers on silicon, either by wafer-bonding techniques that heterogeneously integrate direct-bandgap III–V materials onto silicon circuits, or by direct epitaxy of III–V quantum dots on silicon.

Integrated silicon lasers through wafer bonding

Wafer bonding techniques involves integrating III–V epitaxial layer on patterned silicon circuits via bonding techniques, and the light generated in the III–V material is vertically coupled into silicon circuits by evanescent coupling. Therefore, this design is not subject to lattice match limitations. Bonding techniques could be divided into direct bonding and indirect bonding. Direct bonding normally involves bringing flat and clean wafers or dies into contact to realize a strong interfacial bond. Strictly planar surfaces are generally required to fulfill high-quality direct bonding, rendering complicated fabrication process. Indirect bonding techniques, like benzocyclobutene (BCB) assisted bonding, is more tolerant to non-planar substrates, which requires no complicated fabrication and is free from material limitations. Therefore, BCB assisted bonding is more widely used in hybrid integrated platforms. The wafer bonding techniques provide a way to fabricate the active III–V lasers with lithographic precision and alignment accuracy in silicon, and this can be fabricated in a back-end process after the silicon fabrication, which is in principle fully compatible with the CMOS fabrication procedure.

Direct epitaxy of III–V quantum dots on silicon

While bonding offers a powerful method for hybridly or heterogeneously integrating dissimilar materials, direct epitaxy—growing high quality III–V material on silicon—remains to be the dream of ultimate solution for integrated silicon laser. Such a process would allow for efficient wafer-scale manufacture of silicon laser, which can be lower cost and higher yield than wafer bonding. However, direct epitaxy involves several tremendous technical challenges. The biggest challenge for direct epitaxy lies in the fact that there is large lattice mismatch between silicon and the III–V materials, resulting in dislocations during epitaxial growth. One solution to this problem is to grow very thick buffer layers—but it requires a long process time, and also increases the difficulty of integration with other devices. Significant progress had been made by the teams at University College London, U.K. (UCL), and the University of California, Santa Barbara, USA (UCSB), demonstrating that through the introduction of a few quan-

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tum dot layers into the buffer zone the thickness of the buffer layers can substantially be reduced. Quantum dots can also be used as gain media and, more importantly, they are less sensitive to remaining defects than quantum wells. Both of UCL and UCSB teams were able to demonstrate electrically pumped lasers grown on silicon, operating at room temperature. These remarkable accomplishments confirm that the monolithic Si-based QD laser is a promising candidate for integrated lasers for Si photonics. More recently, high-temperature, high-power, and low-threshold operation has been demonstrated with quantum dot lasers directly grown on silicon. These devices are already rivaling performance of lasers on native substrates, and would stand to be very competitive as an integrated light source once schemes of highly efficient coupling between the lasers and silicon waveguides are developed.

Prospect

Future terabit-per-second datacom and interconnect applications will likely require fully integrated solutions, with volumes of multi-millions compact and power-efficient optical modules per year. Compared with III–V based photonic devices, integrating III–V semiconductors on silicon photonic integrated circuits (PICs) offer the advantage of large silicon substrates and CMOS-compatible fabrication technology, raising the potential for high performance at low cost. Both wafer bonding and direct epitaxy of III–V on silicon hold promise for the production of next generation PICs, and it is too soon to tell which technology will be the mainstream technology in the future. What is clear is that, after significant efforts from research groups all over the world, this field is advancing very rapidly, and the goal of the future research is to bring the III–V on silicon performance on par with, or even better than, the conventional III–V based technology and meeting future demands on lower cost, size, weight, and power (cSWaP).