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Source-field-plated Ga_2O_3 MOSFET with a breakdown voltage of 550 V

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Abstract: Ga_2O_3 metal–oxide–semiconductor field-effect transistors (MOSFETs) with high-breakdown characteristics were fabricated on a homoepitaxial n-typed β-Ga_2O_3 film, which was grown by metal organic chemical vapor deposition (MOCVD) on an Fe-doped semi-insulating (010) Ga_2O_3 substrate. The structure consisted of a 400 nm unintentionally doped (UID) Ga_2O_3 buffer layer and an 80 nm Si-doped channel layer. A high k HfO_2 gate dielectric film formed by atomic layer deposition was employed to reduce the gate leakage. Moreover, a source-connected field plate was introduced to enhance the breakdown characteristics. The drain saturation current density of the fabricated device reached 101 mA/mm at V_{gs} of 3 V. The off-state current was as low as 7.1×10^{-11} A/mm, and the drain current I_{ON}/I_{OFF} ratio reached 10^9. The transistors exhibited three-terminal off-state breakdown voltages of 450 and 550 V, corresponding to gate-to-drain spacing of 4 and 8 μm, respectively.

Key words: Ga_2O_3; MOSFET; breakdown voltage; filed plate

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1. Introduction

Gallium oxide (Ga_2O_3) has recently attracted significant attention as a new semiconductor material for high-power and high-efficiency applications in recent years due to its outstanding characteristics such as ultra-wide bandgap (~4.8 eV), high critical electronic breakdown field (8 MV/cm), and low cost advantages[1]. The Baliga's figure-of-merit, which was used to evaluate the value index of semiconductor materials for high power devices, is as high as 3444 for β-Ga_2O_3, much larger than that of GaN (870) and SiC (340)[1].

Since the first β-Ga_2O_3 metal–semiconductor field-effect transistor (MESFET) was fabricated in 2012[2], a great deal of progress has been made in the development of Ga_2O_3 based field-effect transistors. In 2013, a single-crystal Ga_2O_3 metal–oxide–semiconductor field-effect transistor (MOSFET) was reported in which an Al_2O_3 gated dielectric film formed by atomic layer deposition was adopted. The three-terminal off-state breakdown voltages (V_{br}) reached 370 V[3]. Fabrication of β-Ga_2O_3 MOSFET with a breakdown voltage exceeding 750 V was realized by introducing a gate-connected field plate. The drain current I_{ON}/I_{OFF} ratio was as high as 10^9[4]. Zhou *et al.* reported a high-performance depletion-mode β-Ga_2O_3 on insulator (GOI) field-effect transistors (FETs) by transferring the β-Ga_2O_3 nanomembrane to the SiO_2/Si substrate, which obtained a recorded high drain current of 1.5 A/mm[5]. Although there have been many subsequent developments in Ga_2O_3 based FETs, domestic achievements remain far behind those which have been achieved by foreign investigators.

Our group reported a β-Ga_2O_3 MOSFET with HfO_2 as a gate dielectric, in which the I_{on}/I_{off} ratio was as high as 10^8. However, the three-terminal off-state breakdown voltage was just 113 V[6]. Our group investigated the effect of a gate recess on the electronic characteristics of β-Ga_2O_3 MOSFETs. An enhanced-mode device with a threshold voltage of +3 V was achieved in which the breakdown voltage reached 190 V[7]. However, the performances of the fabricated β-Ga_2O_3 MOSFETs, especially for the breakdown voltage, lag far behind other reported results.

A field plate can suppress the peak electronic field in a MOSFET channel, and effectively improve the breakdown characteristics. In the reported Ga_2O_3 MOSFETs, a just gate-connected field plate was adopted, which increased the breakdown voltage greatly. A source-connected field plate is also a very effective option, which has been widely used in GaN and SiC based power devices. In this paper, a source-connected field plate was introduced into Ga_2O_3 MOSFETs for the first time resulting in increased high-breakdown voltage. The Ga_2O_3 MOSFETs were fabricated on homoepitaxial n-typed β-Ga_2O_3 film. High k HfO_2 gate dielectric film formed by atomic layer deposition was adopted to reduce the gate leakage. In the device, gate-to-drain spacing (L_{gd}) of 4 μm was observed and three-terminal off-state breakdown voltage was measured as 450 V, and reached 550 V as the spacing increased to 8 μm. Finally, the breakdown voltage of 550 V is the highest among domestic reports.

2. Experiments

A schematic cross section of the fabricated Ga_2O_3 MOSFET is shown in Fig. 1. A 400 nm unintentionally doped (UID) Ga_2O_3 buffer layer and an 80 nm Si-doped channel layer were grown by metal organic chemical vapor deposition (MOCVD) on an Fe-doped semi-insulating (010) Ga_2O_3 substrate. The Si donor concentration was 1.0×10^{18} cm^{-3}, whilst electron mobil-

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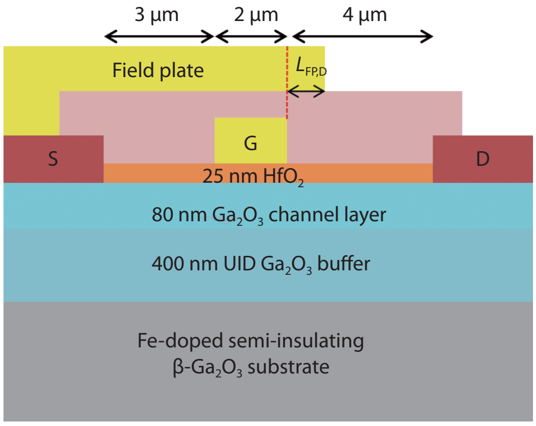

Fig. 1. (Color online) Schematic cross section of the fabricated Ga_2O_3 MOSFET with L_{gd} of 4 μm.

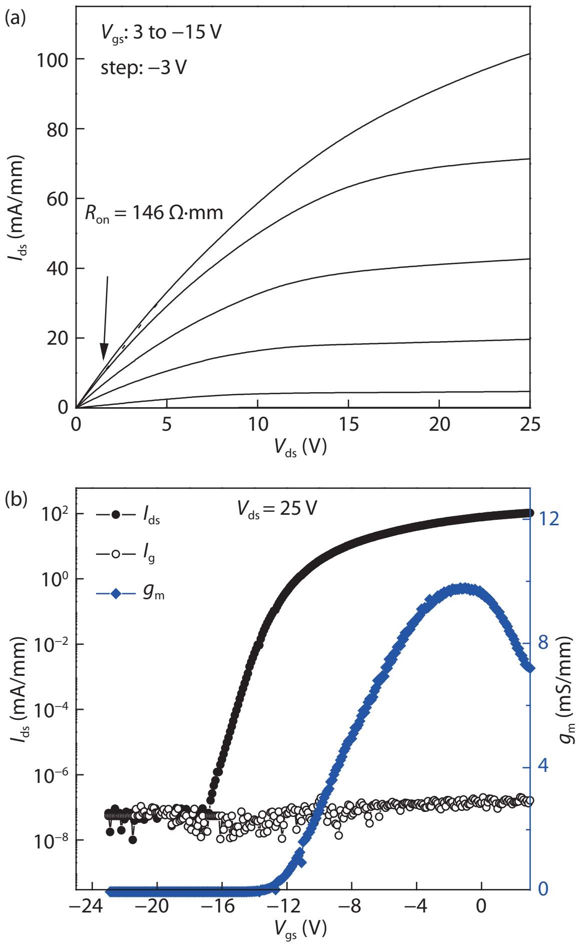

Fig. 2. (Color online) (a) DC output and (b) transfer characteristics of the Ga_2O_3 MOSFET with L_{gd} of 4 μm.

ity was measured at 25 $cm^2/(V{\cdot}s)$. Device fabrication began with mesa isolation, which was performed using BCl_3/Ar inductively coupled plasma (ICP). The mesa height was about 200 nm. The source and drain Ohmic contacts were formed by depositing Ti/Au (15/200 nm) by using e-beam evaporation and lift-off technology. These contacts were annealed in a rapid thermal annealing system for 1 min at 480 °C in nitrogen. With a transmission line method pattern, the specific contact resistance was measured to be 8.5 Ω·mm. A 25 nm HfO_2 gate dielectric layer was then deposited on the surface at 250 °C by atom-

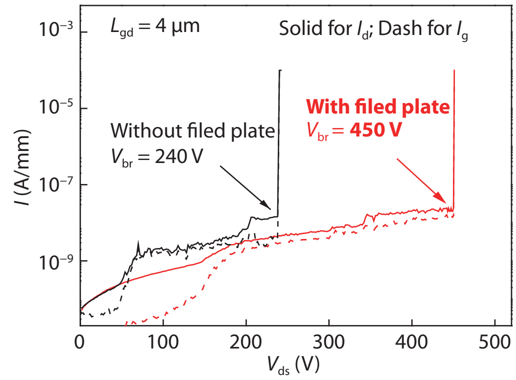

Fig. 3. (Color online) Three-terminal off-state breakdown characteristics for the Ga_2O_3 MOSFET with and without source-field plate.

ic layer deposition. A Ni/Au Schottky contact was fabricated using e-beam evaporation and lift-off technology. As shown in Fig. 1, the gate length (L_g) and gate-to-source distance (L_{gs}) were set at 2 and 3 μm, respectively. The gate-to-drain spacing (L_{gd}) at 4, 8, 15, and 20 μm was also prepared. An 80 nm SiN passivation layer was deposited on the device surface by plasma enhanced chemical vapor deposition (PECVD). SiN/HfO_2 recess was carried out on the source and drain regions by BCl_3 reactive ion etching (RIE). Finally, a Ni/Au source-field plate was realigned to the source contact with a drain extension ($L_{FP,D}$) of 0.8 μm (as shown in Fig. 1).

3. Results and discussion

Standard DC I–V measurements were performed using a semiconductor characterization system at room temperature. Fig. 2(a) illustrates the output characteristics of the fabricated Ga_2O_3 MOSFET from V_{gs} = 3 V to V_{gs} = −15 V with a gate step of −3 V. In the device, the gate length (L_g) and gate-to-source distance (L_{gs}) were 2 and 3 μm, respectively. The gate-to-drain spacing (L_{gd}) was 4 μm. The fabricated Ga_2O_3 MOSFET exhibited good pinch-off characteristics at V_{gs} of −15 V, and showed a maximum drain current (I_D) of 101 mA/mm at V_{gs} of 3 V. The value of on-resistance (R_{on}) was calculated to be 146 Ω·mm from the drain current curve at V_{gs} = 3 V. Fig. 2(b) shows the transfer curve of the fabricated Ga_2O_3 MOSFET at V_{ds} = 25 V. The value of the threshold voltage (V_{th}) for the fabricated device was extracted at −13.7 V, which was defined as the I_D of 1 μA/mm. Once the gate voltage was lower than the pinch-off voltage, the off-state current was mainly dominated by gate leakage, which was about 7.1 × 10^{-11} A/mm. The I_{ON}/I_{OFF} ratio was measured to be as high as 10^9.

The breakdown characteristics of the Ga_2O_3 MOSFETs with L_{gd} of 4 μm were measured and shown in Fig. 3. The breakdown characteristics of devices with and without source field plate were both measured. During the measurements, the gate bias was set as −18 V. For the samples without a field plate, the three-terminal off-state breakdown voltage was measured to be 240 V. The source-connected field plate enhanced the breakdown characteristics greatly, and the breakdown voltage reached 450 V. There existed a peak electronic field near the gate in the gate-to-drain area. The drain extension in the source-field plate effectively suppressed the peak electric field and improved the breakdown voltage. Structures of source field plate, such as drain extension and passivation thickness, have an important impact on the breakdown characterist-

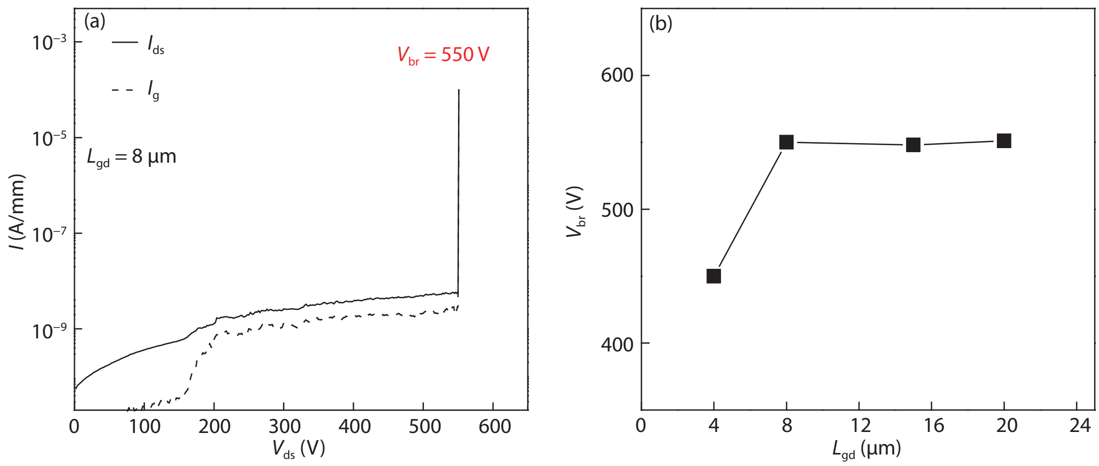

Fig. 4. (Color online) Breakdown characteristics for the Ga_2O_3 MOSFET with L_{gd} of (a) 8 μm and (b) different gate-to-drain length.

ics, which need to be further investigated in detail.

The breakdown characteristics of the Ga_2O_3 MOSFETs with L_{gd} of 8 μm with a source field plate were measured and are shown in Fig. 4(a). The drain extension ($L_{FP,D}$) of the source-field plate was also 0.8 μm. The breakdown voltage increased from 450 to 550 V as the gate-to-drain length increased from 4 to 8 μm. Further increasing the gate-to-drain length, the breakdown voltage became saturated and showed no change, as shown in Fig. 4(b). The width of the depleted region in the Ga_2O_3 MOSFET barely changed once the gate-to-drain length was larger than a certain value. Moreover, the drain extension ($L_{FP,D}$) was all set to be 0.8 μm with different gate-to-drain lengths. As a result, the breakdown voltage of the device did not increase after the gate-to-drain length was longer than 8 μm. Optimization of the structure of the source field plate, such as drain extension and passivation thickness, and the breakdown characteristics can be further improved, which will be investigated in further research.

4. Conclusions

In summary, n-typed β-Ga_2O_3 film was grown by MOCVD on a semi-insulating Ga_2O_3 substrate, which consisted of a 400 nm UID Ga_2O_3 buffer layer and 80 nm Si-doped channel layer. High-breakdown Ga_2O_3 MOSFETs were fabricated by using two key techniques: one is high k HfO_2 gate dielectric film, which was adopted to reduce the gate leakage, and the other is source-connected field plate, which was to suppress the peak electric field in the Ga_2O_3 channel. As a result, the off-state current was as low as 7.1×10^{-11} A/mm, providing a drain current I_{ON}/I_{OFF} ratio of 10^9. Moreover, the three-terminal off-state breakdown voltage reached 550 V in the device with L_{gd} of 8 μm. The drain extension ($L_{FP,D}$) is essential to improving the breakdown characteristics, and should be optimized according to different gate-to-drain lengths. In our future studies, the effect of drain extension ($L_{FP,D}$) on the electric characteristics of Ga_2O_3 MOSFETs will be investigated.

Acknowledgements

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