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REVIEWS

A review of the most recent progresses of state-of-art gallium oxide power devices

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Abstract: Until very recently, gallium oxide (Ga_2O_3) has aroused more and more interests in the area of power electronics due to its ultra-wide bandgap of 4.5–4.8 eV, estimated critical field of 8 MV/cm and decent intrinsic electron mobility limit of 250 $cm^2/(V{\cdot}s)$, yielding a high Baliga's figures-of-merit (FOM) of more than 3000, which is several times higher than GaN and SiC. In addition to its excellent material properties, potential low-cost and large size substrate through melt-grown methodology also endows β-Ga_2O_3 more potential for future low-cost power devices. This article focuses on reviewing the most recent advances of β-Ga_2O_3 based power devices. It will be starting with a brief introduction to the material properties of β-Ga_2O_3 and then the growth techniques of its native substrate, followed by the thin film epitaxial growth. The performance of state-of-art β-Ga_2O_3 devices, including diodes and FETs are fully discussed and compared. Finally, potential solutions to the challenges of β-Ga_2O_3 are also discussed and explored.

Key words: gallium oxide; power electronics; power devices

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1. Introduction

Motivated by achieving high breakdown voltage and high energy conversion efficiency simultaneously, ultra-wide bandgap semiconductor materials and devices with high carrier mobility are powerful competitors of the next generation power electronics. Ultra-wide bandgap materials like diamond, β-Ga_2O_3 and AlN have attracted most of the attentions, due to their high Baliga's figure of merit (BFOM), defined as $\varepsilon\mu E_c^3$, where ε, μ and E_c are the dielectric constant, carrier mobility and critical breakdown field (E_c), respectively[1–9]. Compared to diamond and AlN, the monoclinic β-Ga_2O_3 has the advantages of potential low cost and large size substrate through melt-grown method and the easy control of the n-type doping, while on the contrary, both diamond and AlN are difficult to be doped and the high quality single crystalline native substrate are extremely expensive[7, 8]. β-Ga_2O_3 with an ultra-wide bandgap of 4.6–4.9 eV, estimated E_c = 8 MV/cm and decent intrinsic electron mobility limit of 250 $cm^2/(V{\cdot}s)$, yielding a high BFOM of more than 3000, which is several times higher than that of GaN and SiC, showing that β-Ga_2O_3 is more promising candidate for power electronics by simultaneous achieving higher breakdown voltage (BV) and lower specific on-resistance ($R_{on, sp}$) from the material point of view.

Although some progresses have been achieved, the performance and development of β-Ga_2O_3 based devices are still far behind the GaN and SiC's. While in fact, the research of β-Ga_2O_3 both on material and device still present itself as a virgin area, such that more universities, research institutes, national laboratories, and government funding are needed to have a fully discovering and understanding about the material properties, how to enhance device performances and make them comparable or even higher when compared with the device performance of GaN and SiC. In this review article, recent advances of the state-of-art material growth and device technologies are summarized, showing the great promise of β-Ga_2O_3 as power device channel material.

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2. Basic material properties of β-Ga_2O_3

There are 5 polymorphs of β-Ga_2O_3, namely α, β, γ, δ, and ε[10–15]. Among which, the monoclinic (β-) phase of β-Ga_2O_3 denotes the most stable one until its melting point, while other polymorphs are metastable and will convert into β phase at an elevated temperature (T) above 750–900 °C. The crystal structure and lattice parameters of β-Ga_2O_3 are shown in Fig. 1, with lattice constant a = 12.2 Å, b = 3.0 Å and c = 5.8 Å, respectively. The unit cell possesses two crystallographically inequivalent Ga positions, one with tetrahedral geometry Ga (I) and one

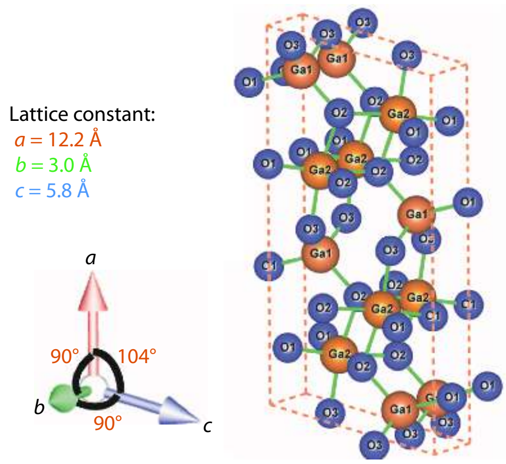

Fig. 1. (Color online) Atomic unit cell of β-Ga_2O_3 with lattice constant and angle marked.

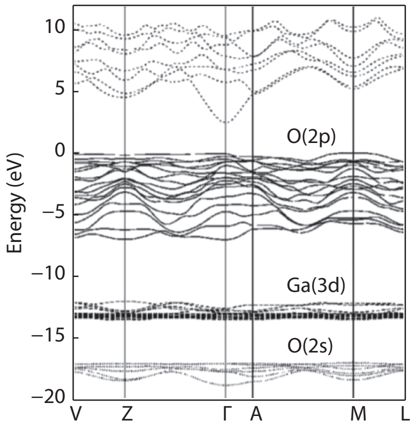

Fig. 2. Band structure of β-Ga_2O_3 with Fermi energy aligned to zero. Reprint from Appl Phys Lett, 88, 261904 (2006). Copyright 2006 American Institute of Physics.

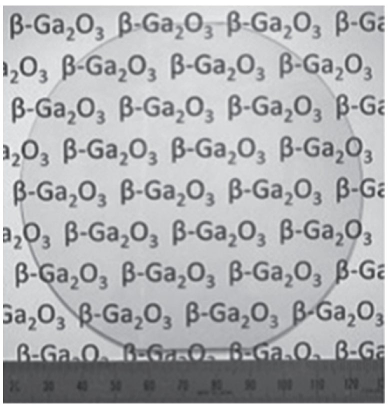

Fig. 3. Photograph of 4-inch-diameter β-Ga_2O_3 wafer. Reprinted from Higashiwaki *et al.*, J Phy D, 50 (2017). Copyright 2017 IOP Publishing[30].

with octahedral geometry Ga (II). The oxygen ions are arranged in 'distorted cubic' array. Oxygen atoms have three crystallographically different positions and are denoted as O(I), O(II) and O(III), respectively. Two oxygen atoms are coordinated trigonally and one is coordinated tetrahedrally. The different position of Ga and O atoms leads to an anisotropic optical, electrical and physical properties, for example its different thermal conductivity at (-201), (100), (010) and (100) planes. The upper valence and lower conduction band structure of β-Ga_2O_3, calculated from density functional theory (DTF) is shown in Fig. 2, as reported by He *et al.*[13]. It is generally accepted that the bandgap from DFT is underestimated due to the ground state theory. More accurate bandgap value of β-Ga_2O_3 is extracted to be around 4.8 eV from hybrid DFT, which is in agreement with absorption and resolved photoemission experiment[16, 17]. The electron effective mass is calculated to be around $0.3m_o$, where m_o is the free electron mass. However, the flatness of valence band shows the large effective mass of holes, indicating an extremely low hole mobility even the p-type doping can be resolved. In addition to the challenges of the p-type doping and low hole mobility issues, the extremely low thermal conductivity of 10–25 W/(m·K) both from theoretical calculation and experiment turns out to be the most detrimental property of using β-Ga_2O_3 native substrate and potential solutions will be described in the future section.

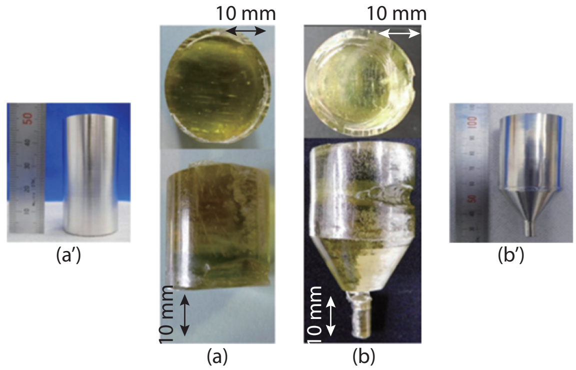

Fig. 4. (Color online) β-Ga_2O_3 crystals grown by the VB method in either (a) a full-diameter crucible (a′), and (b) or in a conical crucible (b′). Reprinted from Hoshikawa *et al.*, J Cryst Growth 447, 36 (2016). Copyright 2016 Elsevier[31].

3. Bulk substrate growth and thin film epitaxial growth

The success achieving of large diameter single crystalline and low defect density β-Ga_2O_3 native substrates is the main stimulation of devoting tremendous efforts to realize the application of β-Ga_2O_3 based materials and devices. Particularly, the development of melt-grown method offers the great promise of accomplishing low cost commercial substrates, which is advantageous over the growth techniques of SiC and bulk GaN. Standard growth techniques of β-Ga_2O_3 including Czochralski method (CZ)[18–20], edge-defined film fed (EFG)[21], floating-zone (FZ)[22–24] and vertical Bridgman (VB)[25–27] growth methods. Tomm *et al.* first studied the CZ growth of the β-Ga_2O_3 single crystals and later Galazka et al carried out a comprehensive study on the same method[28, 29]. It is reported that a diameter of 2 inches cylindrical β-Ga_2O_3 single crystal have been demonstrated with this CZ method. It is generally accepted that the EFG is the most promising growth method for β-Ga_2O_3, combing the capability of achieving large size and high quality for future high-volume production, which is also a standard method for sapphire substrate. Growth rate as high as 15 mm/h and large size of 4 inches have been accomplished even at this premature stage, as shown in Fig. 3[30]. FZ method is always used as a route to synthesis β-Ga_2O_3 rod for basic research purpose with typical growth rate of 6 mm/h and diameter of 10 mm. VB methods provide another useful alternative methodology to achieve β-Ga_2O_3 single crystals by providing the advantage of easy release of the crystals after growth. The single crystal with diameter of 25 mm is obtained through this method, as shown in Fig. 4[31]. It should be noted that the unintentional incorporation of the Si and Ir atoms from the β-Ga_2O_3 seed and crucible leads to the unintentionally doped (UID) n-type conducting in the material so that deep acceptors like Mg and Fe are commonly used to compensate those n-type dopants to achieve the semi-insulating property.

Developing high quality β-Ga_2O_3 thin film epitaxial growth is of equal importance when compared to the β-Ga_2O_3 substrate, since β-Ga_2O_3 thin film always serve as the channel layer for power devices such as diodes and MOSFETs. Accurate control of the dopants and minimization of defects and imperfections are always two challenges for thin film epitaxial growth. Homoepitaxial growth of high quality β-Ga_2O_3 thin

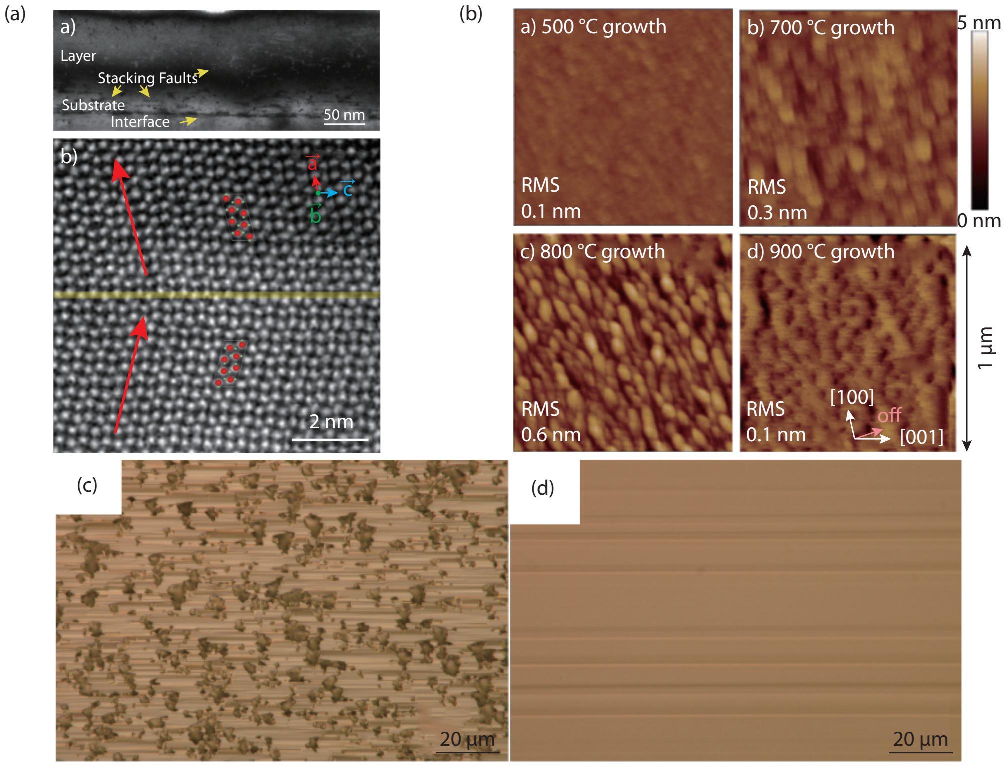

Fig. 5. (Color online) (a) HRTEM image of an undoped homoepitaxial β-Ga_2O_3 layer from MOVPE method. (b) Surface morphologies of 60-nm-thick β-Ga_2O_3 (010) layers grown on Sn-doped β-Ga_2O_3 (010) substrates at a growth rate of 1 nm/min under slightly Ga-rich conditions at the growth temperatures of 500, 700, 800, and 900 °C, respectively. NDIC microscopy images of β-Ga_2O_3 surfaces after HVPE growth on (001) β-Ga_2O_3 substrates for 1 h at (c) 800 and (d) 1000 °C. Reprinted from Refs. [33, 37, 41].

Table 1. Properties of β-Ga_2O_3 relative to some other major semiconductors used for power electronics applications, considering their different kinds of FOM.

Material Parameter	Si	GaAs	4H-SiC	GaN	Diamond	β-Ga_2O_3
Bandgap E_g (eV)	1.14	1.43	3.25	3.4	5.5	4.8
Dielectric constant ε	12	13	10	9	5.5	11
Breakdown field E_C (MV/cm)	0.3	0.4	2.5	3.3	10	8
Carrier mobility μ ($cm^2/(V\cdot s)$)	1450	8400	1000	1200	2000	300
Saturation velocity v_{sat} (10^7 cm/s)	1	1.2	2	2.5	1	2
Thermal conductivity κ (W/mK)	150	50	370	250	2000	10–30
FOM relative to Si						
Baliga FOM = $\varepsilon\mu E_c^3$	1	14.7	317	846	24 660	3200
Johnson FOM = $E_c^2 v_{sat}^2/4\pi^2$	1	1.8	278	1089	1110	2844
Baliga High Frequency FOM = μE_c^2	1	10	46	100	1500	142
Keyes FOM = $\kappa[(cv_{sat})(4\pi\varepsilon)]^{1/2}$	1	0.3	3.6	1.8	41.5	0.2

films on its native substrates can be carried out by the following major ways: metalorganic chemical vapor deposition (MOCVD)[32–34], molecular beam epitaxy (MBE)[35–38], halide vapor phase epitaxy (HVPE)[39–42], mist-CVD and some other CVD techniques[43–49]. MOCVD and MBE are two of the most popular epitaxial growth tools, which are widely used in GaAs and GaN epitaxial growth. Baldini *et al.* reported on growing Sn-doped homoepitaxial layer on (100) substrate with MOCVD[50]. TEGA, molecular oxygen (O_2) and TESn were used as Ga, O and Sn precursors, respectively. The epi-layer has a RMS surface roughness of 0.6 nm and the main defects in the layers were stacking faults and twin lamella. Gogova *et al.* reported on achieving single-phase, smooth β-Ga_2O_3 layers doped with Si, with a dislocation density not exceeding those of the melt grown substrate. HRTEM image of grown thin film is shown in Fig. 5(a)[33]. Okumura *et al.* reported on using plasma-assisted MBE to grow the (010) β-Ga_2O_3 under Ga-rich conditions at growth temperatures above 650 °C with growth rate about 2.2 nm/min. Slightly Ga-rich conditions between 650 and 750 °C are optimal for a smooth surface with an RMS surface roughness of 0.1 nm at a high growth rate. Surface roughness at various growth temperature is shown in Fig. 5(b)[37]. HVPE is one of the most cost effective methodologies in terms of deposition rate, epi-layer quality and inexpensive facility. However, it generally ends up with a rough surface, which requires a post chemical mechanical polishing process to smooth. Murakami *et al.* reported on using GaCl and O_2 precursors for the HVPE of β-Ga_2O_3 thin film on (001) β-Ga_2O_3 substrate with a relative smooth surface morphology and low net carrier doping concentration of 10^{13} cm^{-3} at a limited growth rate of 5 μm/h and tem-

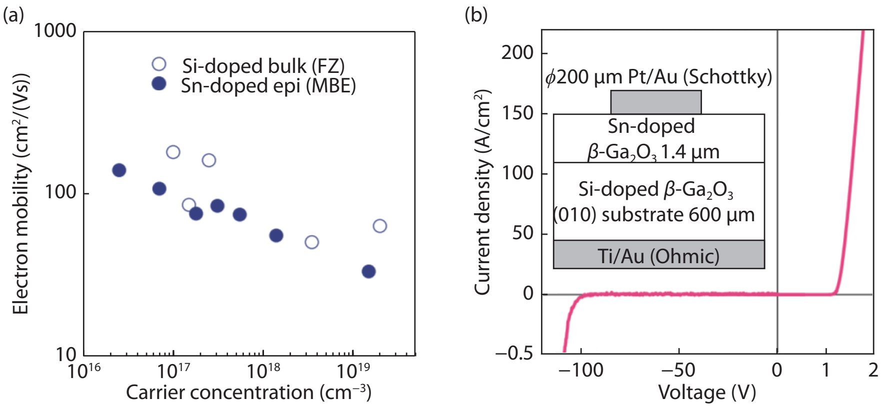

Fig. 6. (Color online) (a) Electron mobility as a function of carrier concentration. (b) *I*–*V* characteristics of Pt/β-Ga_2O_3 Schottky barrier diodes. The inset shows the schematic structure of the β-Ga_2O_3 SBD. Reprinted from Sasaki *et al.*, Appl Phys Express, 5, 035502 (2012)[52]. Copyright of 2012 Japanese Society of Applied Physics.

perature of 1000 °C. The microscopy images of β-Ga_2O_3 surfaces after HVPE growth on (001) β-Ga_2O_3 substrates for 1 h at (c) 800 and (d) 1000 °C[41] are shown in Fig. 5. Mist CVD is another inexpensive approach to grow different polymorphs of Ga_2O_3, like α-, β-, γ-phases at a relatively low growth temperature of 500–630 °C, while the solution is atomized via ultrasonication at a frequency of 2.4 MHz. Other phases can be transformed into β-phase after a high temperature annealing.

4. Device performances: diodes and FETs

As always emphasized by the β-Ga_2O_3 community, β-Ga_2O_3 holds promise for future power electronics due to its ultra-wide bandgap, high breakdown field and decent electron mobility induced high BFOM. Table 1 lists the comparisons of some major semiconductors as the channel materials for power devices. Some key FOMs used for representing how ideal of this material can be utilized for power electronics, such as Baliga, Johnson and Keys are also included. Baliga, Baliga high frequency, Johnson and Keyes FOMs are used to evaluate the power devices in terms of power handling capability and conduction loss, the measure of switching losses, the measure of suitability of a semiconductor material for high frequency power transistor applications and requirements, and the thermal dissipation capability for power density and speed, respectively. As shown in this Table 1, all other FOMs of β-Ga_2O_3 are significantly higher than that of SiC and GaN except Keyes FOM due to its obvious shortage of extremely-low thermal conductivity. Nevertheless, we should put all our endeavors to explore and demonstrate all its potentials and then push the device performance to its limit. Diodes and FETs are the most basic but most important elements of power electronics, which deserve thorough investigation. In this section, the most recent progresses of both diodes and FETs are comprehensively reviewed and solution to its low thermal conductivity issue is proposed.

4.1. Schottky barrier diodes on native substrates

Schottky Barrier Diodes (SBDs) with low turn on voltage (V_{on}), high forward current density and fast switching speed properties are ideal candidate for low switching/conduction losses and high frequency operations, which are indispensible components in power electronic circuits such as converters and inverters for power supplies and power factor corrections[51]. Sasaki *et al.* developed the first β-Ga_2O_3 SBD on its (010) native substrate with a 1.4 μm thick ozone MBE homoepitaxial grown drift layer and a breakdown voltage (BV) of more than 100 V is achieved[52]. The electron mobility of this Sn-doped thin film is reported to be as high as 100–150 $cm^2/(V{\cdot}s)$ at a doping concentration range of 10^{16}–10^{17} cm^{-3}. The mobility versus doping concentration and *I*–*V* characteristics are included in Fig. 6.

Following the 1st β-Ga_2O_3 SBD, many research groups have demonstrated high performance SBDs with BV around or exceeding 1 kV with or without field-plate or edge termination techniques. Konishi *et al.* reported on the 1st achieving of the BV more than 1 kV with a field-plate structure and a 7-μm thick HVPE grown β-Ga_2O_3 drift layer[53]. Diodes were fabricated by depositing full area back Ohmic contacts of Ti/Au (20 nm/230 nm) by E-beam evaporation, while the Schottky contacts were patterned by lift-off of E-beam deposited Schottky contacts Pt/Ti/Au (15 nm/5 nm/500 nm) on the epitaxial layers with a field plate length of 20 μm. The net donor concentration of this epitaxial layer is calculated to be 1.6 × 10^{16} cm^{-3} from *C*–*V* measurement. To achieve a high BV, a low density channel or drift layer is needed so as to flatten the electric field from the anode to cathode based on the Poisson Equation. The device has a specific on-resistance of 5.1 $m\Omega{\cdot}cm^2$, yielding a power FOM of 227 MW/cm^2, combined with the BV of 1076 V. The peak E at anode edge is simulated to be 5.1 MV/cm, which is much higher than the E_C of GaN and SiC. Fig. 7 shows the details of the device schematic, forward and reverse *J*–*V* characteristics.

Yang *et al.* also demonstrated 1 kV-class vertical β-Ga_2O_3 SBD without field-plate structure with a 10-μm thick β-Ga_2O_3 drift layer and Ni/Au as the anode[54]. The native substrate possesses a pit dislocation of 10^3 cm^{-2} and the epitaxial layer has a net doping concentration of 2 × 10^{16} cm^{-3}. It is found that the BV has a strong dependence on the anode diameter and the BV is around 1 KV and 800 V at an anode diameter of 105 and 205 μm, respectively, as shown in Fig. 8(a). The diode is also reported to achieve a high power FOM of 150 MW/cm^2 with a $R_{on,sp}$ of 6 $m\Omega{\cdot}cm^2$. By further shrinking the anode diameter to 25 μm, the BV is further increased to be 1.6 kV at a decent power FOM of 100 MW/cm^2, as shown in Fig. 8(b)[55]. This

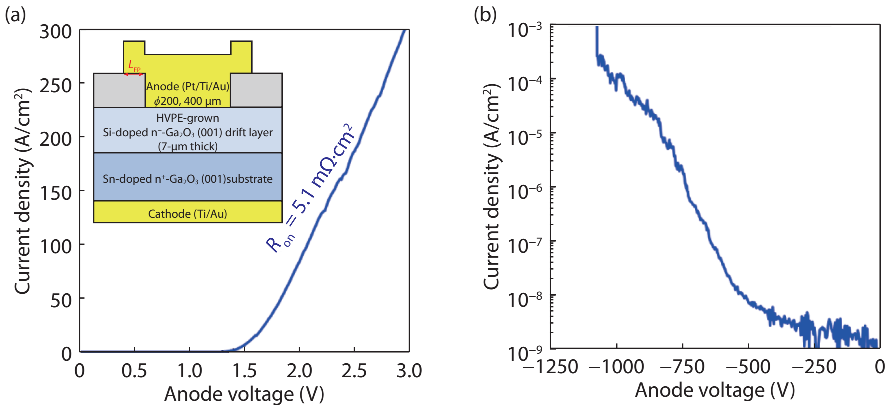

Fig. 7. (Color online) (a) Forward and (b) reverse *J–V* characteristics of β-Ga_2O_3 FP-SBD at room temperature. Inset shows the cross-section device schematic of the vertical SBD. Reprinted from Appl Phys Lett, 110, 103506 (2017). Copyright 2017 American Institute of Physics[53].

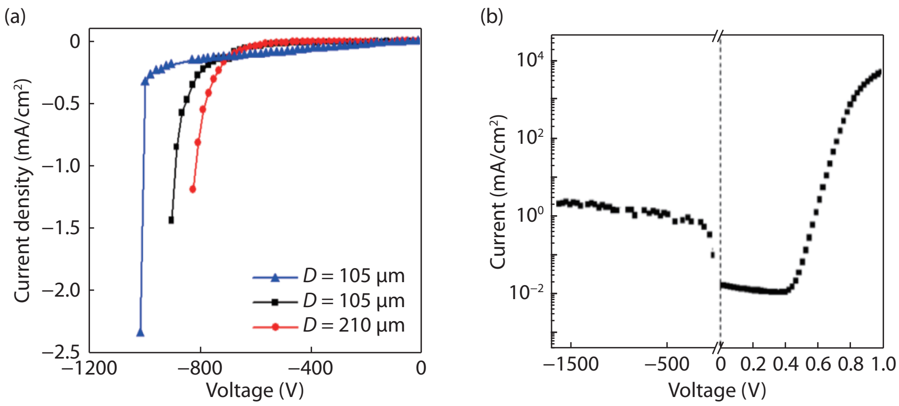

Fig. 8. (Color online) (a) Reverse *I–V* characteristics of 3 diodes with two different diameters, showing a diameter dependence of the BV, and (b) forward and reverse *I–V* characteristics from a 20 μm diameter diode. Reprinted from Appl Phys Lett, 110, 192101 (2017) and IEEE Electron Device Lett. Copyrights 2017 American Institute of Physics and 2017 IEEE[54, 55].

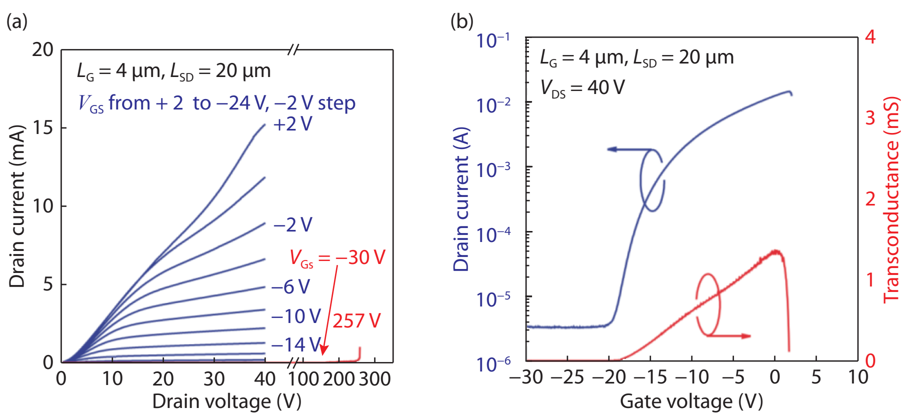

Fig. 9. (Color online) (a) DC output characteristics of β-Ga_2O_3 MESFET and (b) transfer characteristics of the same MESFET at V_{DS} = 40 V. Reprinted from Appl Phys Lett, 100, 013504 (2012). Copyrights 2012 American Institute of Physics[57].

anode diameter dependent BV is most likely related with defects in the epitaxial layer. With larger anode area, higher quantities of defects are expected underneath the anode so that once a point defect is damaged under the high E condition the whole diode is destroyed, resulting in a reduced BV. Through growth optimization, the carrier concentration in the epitaxial layer can be further reduced to 2×10^{15} cm^{-3}. Combined with a 20-μm thick drift layer, the BV can be enhanced to 2300 V. Meanwhile, a high current of 2 A can be also achieved by enlarging the anode area to 0.2 cm^2[56].

4.2. Field effect transistors (FETs) on native substrates

4.2.1. Depletion-mode high-power FETs

The first metal-semiconductor-FET (MESFET) was demonstrated by Higashiwaki *et al.* with a Sn-doped β-Ga_2O_3 epitaxial channel on a semi-insulating (010) β-Ga_2O_3 substrate[57]. This circular MESFET is with a gate length (L_G) of 4 μm and source-drain (L_{SD}) of 20 μm demonstrates a BV of more than

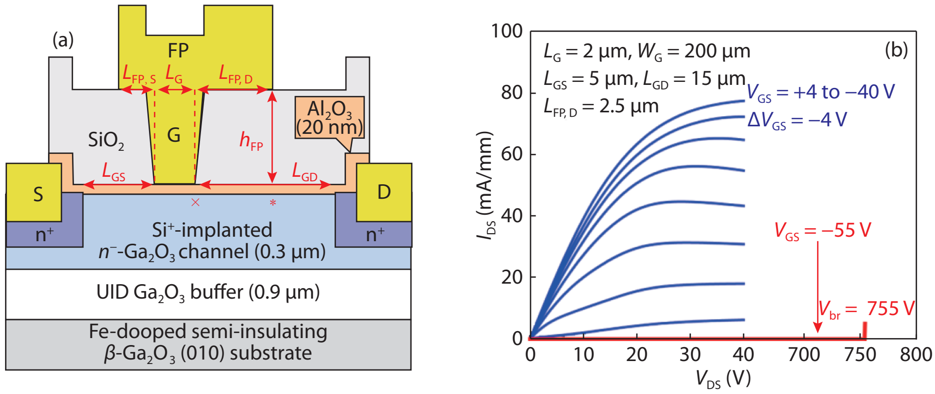

Fig. 10. (Color online) (a) Schematic cross section of a β-Ga_2O_3 MOSFET with a gate-connected FP structure and (b) Output characteristics of the MOSFET with maximum I_D of 78 mA/mm and BV of 750 V. Reprinted from IEEE Electron Device Lett, 37, 2 (2016). Copyright of 2016 IEEE[58].

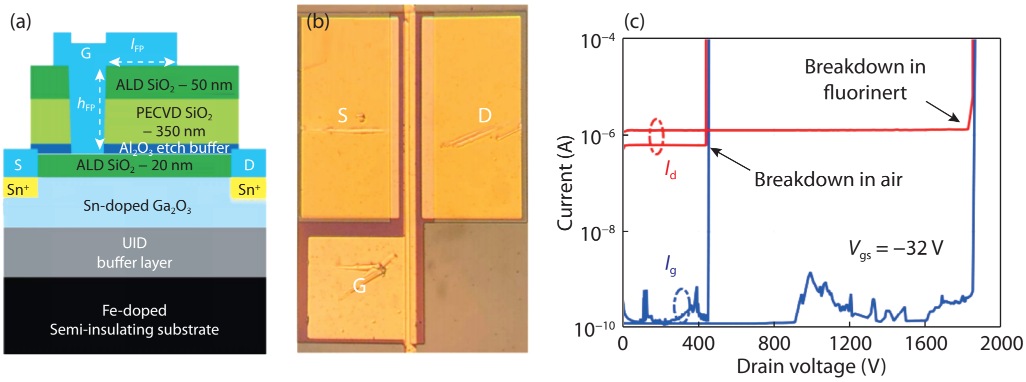

Fig. 11. (Color online) (a) Cross-section view and (b) optical image of the fabricated field-plated Ga_2O_3 MOSFET with SOG S/D doping. (c) Three-terminal breakdown measurement of the field-plated Ga_2O_3 MOSFET and a record-high BV of 1850 V is demonstrated. Reprinted from IEEE Electron Device Lett, 39, 9 (2018). Copyright of 2018 IEEE[59].

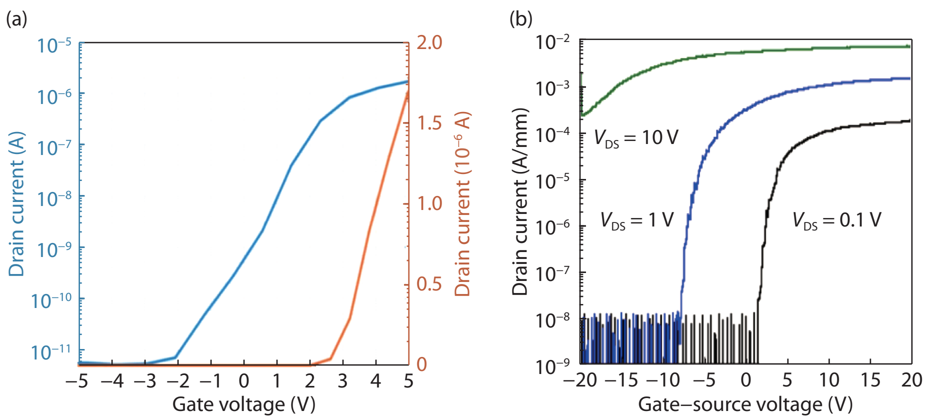

Fig. 12. (Color online) I_D–V_{GS} characteristics of (a) Zeng's and (b) Tadjer's E-mode MOSFET. Reprinted from IEEE Device Research Conf and ECS J, Solid State Sci, Technol, 39, 9 (2018). Copyright of 2016 IEEE[60] and 2016 ECS[5].

250 V, drain current (I_D) of 15 mA and on/off ratio around 10^4. Output and transfer characteristics are plotted in Fig. 9. Following the MESFET, metal-oxide-semiconductor FETs (MOSFETs) start to attract the power device community's attention to resolve the shortcomings of the MESFET. The first lateral depletion-mode (D-mode) β-Ga_2O_3 MOSFET power device with BV more than 600 V was reported by Wong *et al.*[58]. The device structure is shown as Fig. 10(a) with a MBE grown and Si-doped channel with doping concentration of 3×10^{17} cm^{-3}, a heavily doped source and drain contacts and a FP length of 2.5 μm. A maximum I_D of 80 mA/mm, peak g_m of 3.5 mS/mm and high on/off ratio of more than 10^9 are achieved simultaneously. Pulsed I_D–V_{DS} shows no current collapse phenomenon, verifying the great promise of β-Ga_2O_3 MOSFET as a candidate for power device application. Recently, Zeng *et al.* has pushed the BV to be 1850 V by adopting a FP structure and a 400-nm thick composite field plate oxide at a L_{GD} = 20 μm[59]. It is believed that the introduction of another 50 nm of ALD SiO_2 is helpful in improving the BV, rather than a simply plasma-enhanced CVD (PECVD) SiO_2 layer underneath the gate FP elec-

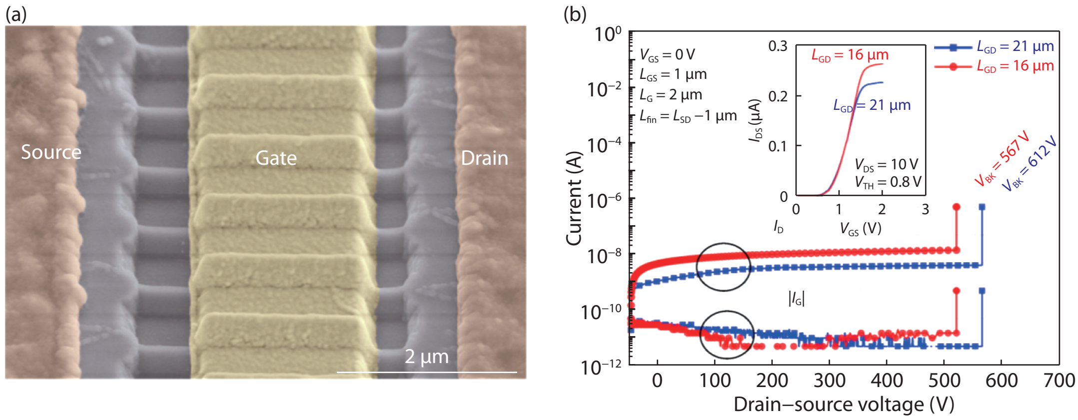

Fig. 13. (Color online) (a) Tilted false-colored SEM image of a fabricated E-mode β-Ga_2O_3 Fin-MOSFET and (b) The breakdown characteristics of β-Ga_2O_3 Fin-MOSFET with L_G = 2 μm and L_{GD} = 16, 21 μm at V_{GS} = 0 V. The inset shows the transfer characteristics of the same device indicating a V_{TH} = 0.8 V. Reprinted from Appl Phys Lett, 109, 213501 (2016). Copyrights 2016 American Institute of Physics[4].

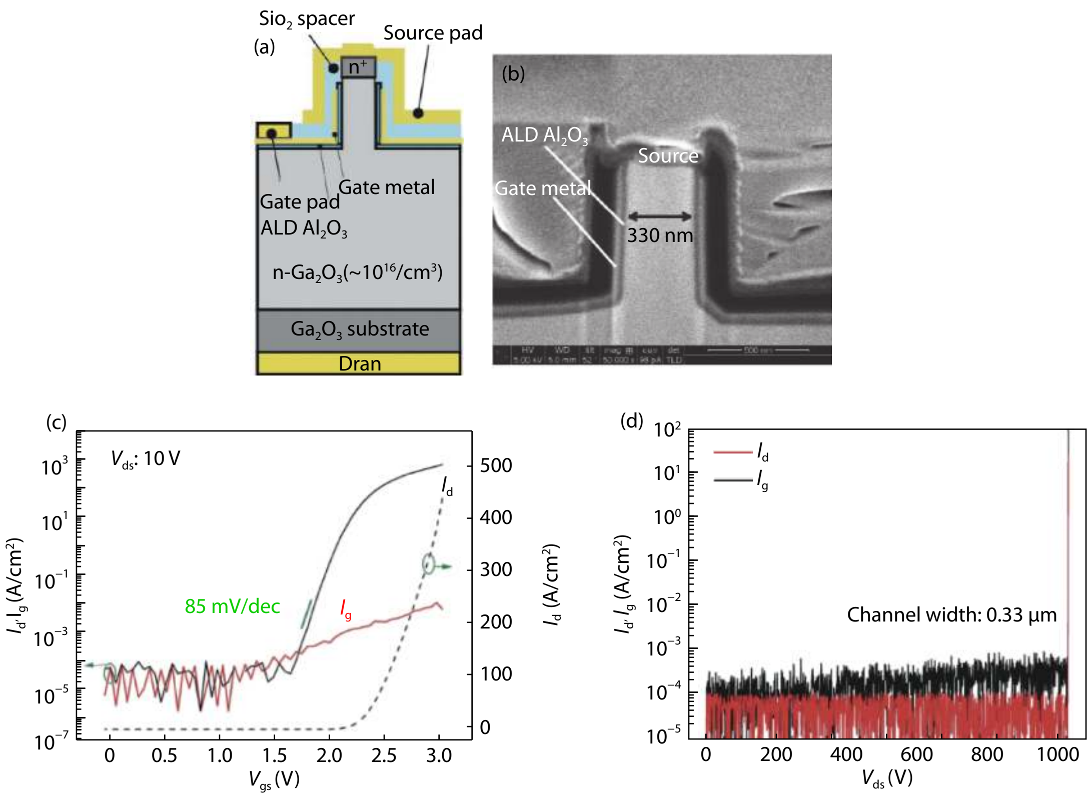

Fig. 14. (Color online) (a) Schematic cross-section and (b) SEM image of a vertical E-mode β-Ga_2O_3 Fin-MOSFET, (c) transfer characteristics of the device with a V_{TH} = 2.2 V, on/off ratio of 108, and on-current of 400 A/cm^2. (d) The breakdown characteristics of β-Ga_2O_3 Fin-MOSFET with channel width of 330 nm. Reprinted from IEEE Electron Device Lett, 39, 869, 2018. Copyright of 2018 IEEE[61].

trode, where the premature breakdown happens and also a high-quality ALD SiO_2 is available to sustain a higher E_C. The device structure and breakdown characteristics are described in Fig. 11.

4.2.2. Enhancement-mode (E-mode) high-power FETs

Zeng *et al.* reported on achieving the first E-mode β-Ga_2O_3 MOSFET by adopting a high work function Au gate electrode and low doping (6×10^{15} cm^{-3}) MBE β-Ga_2O_3 channel, so that E-mode operation with V_T of 3 V and BV of 400 V are demonstrated[60]. Later, Tadjer *et al.* fabricated a (001) β-Ga_2O_3 MOSFET with V_T = 2.9 V and HfO_2 as the gate dielectric[5]. Figs. 12(a) and 12(b) are the I_D–V_{GS} characteristics of Zeng's and Tadjer's E-mode MOSFET. Chabak *et al.* demonstrated the E-mode β-Ga_2O_3 MOSFET via incorporating a fin-array structure with triangular fin-width of 300 nm and fin-height of 200 nm, such that the high work function Ni gate electrode can deplete the β-Ga_2O_3 channel from two side walls with V_T around 1 V[4]. On/OFF ratio greater than 10^5 and a three-terminal BV of more than 600 V are achieved at a 21-μm gate-drain spacing, as shown in Fig. 13. Hu *et al.* has adopted a similar Fin-structure to achieve an E-mode operation on a vertical MOSFET[61]. A 10-μm thick HVPE β-Ga_2O_3 layer on (001) substrate with low charge doping concentration of 2×10^{16} cm^{-3} is used as the starting wafer. By shrinking the fin-width to 330 nm or even smaller, the V_T is extracted to be 1.2–2.2 V. A current

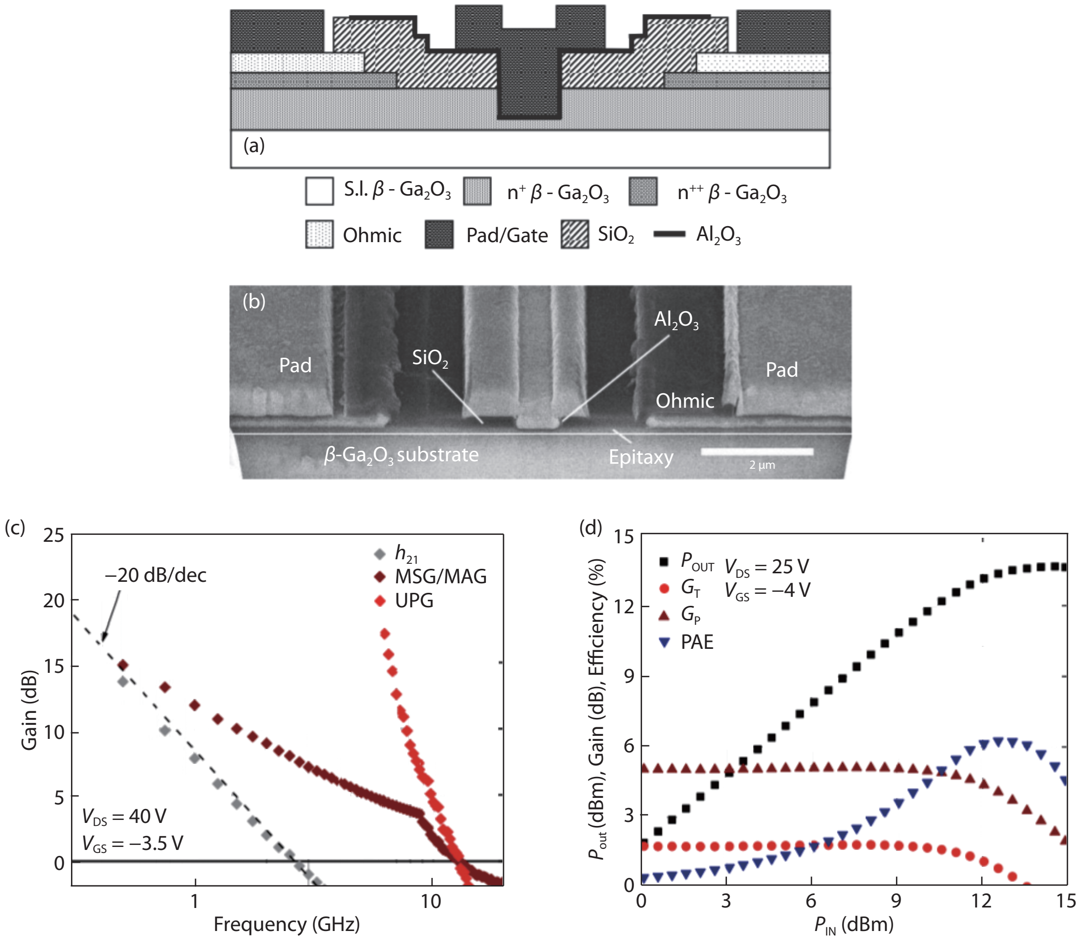

Fig. 15. (Color online) (a) A device cross section schematic is shown for the β-Ga_2O_3 MOSFET under test. (b) A focused ion beam (FIB) cross sectional image of the device. (c) Extrinsic small signal RF gain performance recorded at $V_{GS} = -3.5$ V (peak gm) and $V_{DS} = 40$ V (d) 800 MHz Class-A power sweep of a 2 × 50 μm β-Ga_2O_3 gate recessed MOSFET. Reprinted from IEEE Electron Device Lett, 38, 790, 2017. Copyright of 2017 IEEE[62].

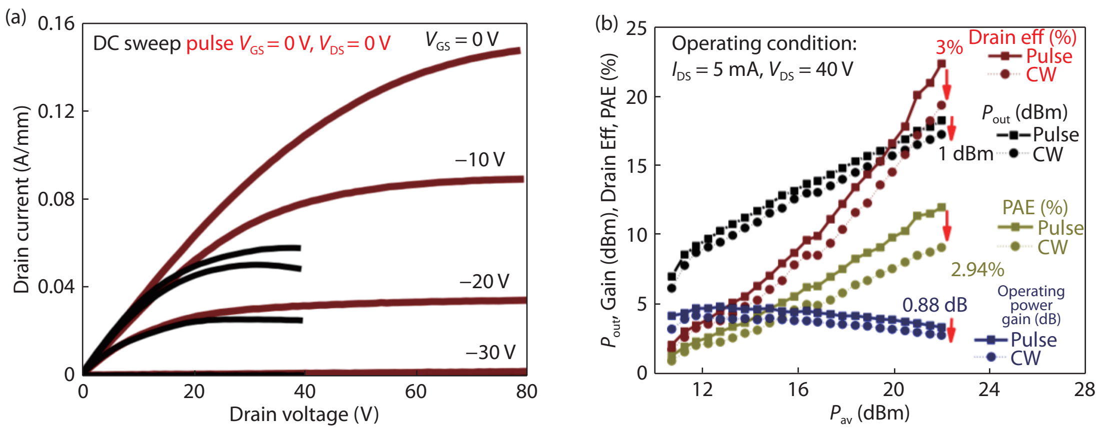

Fig. 16. (Color online) (a) DC output characteristics and pulsed I–V from a quiescent bias of $V_{GS} = V_{DS} = 0$ V up to $V_{DS} = 80$ V with 1 μs pulse length and 1 ms period (b) Pulsed and CW large signal measurements at 1 GHz with input available power sweep up to 22 dBm, measured at $V_{DS} = 40$ V with $I_{DS} = 5$ mA. Reprinted from IEEE Electron Device Lett, 39, 1572, 2018. Copyright of 2018 IEEE[63].

on/off ratio of 10^8, $R_{on,sp}$ of 13–18 mΩ·cm^2, BV up to 1057 V and output current of more than 200 A/cm^2 are demonstrated. Figs. 14(a)–14(d) depict the device structure of the vertical E-mode β-Ga_2O_3 MOSFET, on-state I_D–V_{GS} and three-terminal OFF-state breakdown measurement results, respectively.

4.2.3. High frequency RF Power FETs

Green *et al*. reported on demonstrating the first β-Ga_2O_3 RF transistor on a Si-doped MOCVD β-Ga_2O_3 channel with doping concentration of 10^{18} cm^{-3} and a (100) substrate[62]. By recessing the β-Ga_2O_3 epi-channel, peak transconductance of 21 mS/mm and extrinsic cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) of 3.3 GHz and 12.9 GHz are achieved. Meanwhile, CW class-A power amplifier demonstrate a output power density (P_{out}), power gain, and power-added efficiency

Table 2. Comparison of CW and pulse large signal measurements performed at two different operating power levels of 0.4 and 0.8 W/mm. larger differences in performance between cw and pulsed modes can been seen with increasing operating power. Reprinted from IEEE Electron Device Lett, 39, 1572, 2018. Copyright of 2018 IEEE.

Parameter	Operating condition 0.4 W/mm 25 °C (I_{DS} = 5 mA, V_{ds} = 40 V)		Operating condition 0.8 W/mm 25 °C (I_{DS} = 10 mA, V_{DS} = 40 V)	
	CW	Pulse	CW	Pulse
P_{out} (dBm)	17.42	18.28	17.63	19.52
P_{out} (W/mm)	0.11	0.13	0.11	0.17
Drain Eff (%)	19.56	22.40	13.83	17.04
PAE (%)	9.09	12.01	3.23	6.85
Max gain (dB)	4.17	4.81	2.08	3.68
Channel temperature (°C)	58	28	97	36

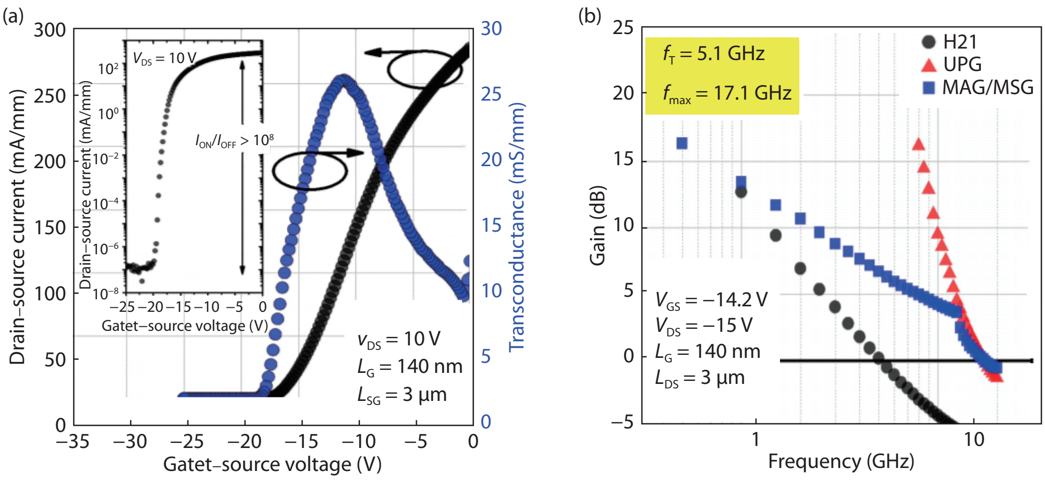

Fig. 17. (Color online) Transfer characteristics of the thin-channel BGO MOSFET with T-gate. The G_M reaches 25 mS/mm with current density over 275 mA/mm, and the inset shows a good I_{ON}/I_{OFF} ratio greater than 10^8. (b) Small signal gain at V_{DS} = 15 V of the thin-channel BGO MOSFET with f_t/f_{max} = 5.1/17.1 GHz. Reprinted from IEEE IMWS-AMP, 2018. Copyright of 2018 IEEE[64].

(PAE) of 0.23 W/mm, 5.1 dB and 6.3%, respectively at the frequency of 800 MHz. Device structure, small signal and large signal performances are described in Fig. 15. Singh *et al.* carried out the study on the pulsed large signal RF performance of field-plated β-Ga_2O_3 MOSFET[63]. It is revealed that reduced self-heating when pulse resulted in a PAE of 12%, drain efficiency of 22.4%, P_{out} of 0.13 W/mm and a maximum gain up to 4.8 dB at 1 GHz for a device with L_g = 2 μm. Self-heating effect at high V_{DS} and I_{DS} caused by the low thermal conductivity is the main factor limiting the device performances, while the trapping effect has the minimal impact on the performance degradation. Pulsed I_D–V_{DS} measurement and large signal load pull measurement results are shown in Fig. 16 and the comparison between CW and pulsed results are shown in Table 2, indicating the self-heating effect is the primary detrimental factor of degrading device performance. Chabak *et al.* reported on achieving high performance β-Ga_2O_3 RF transistor by utilizing a higher doped but thinner Si doped MOVPE (100) channel with submicron T-shape gate[64]. A record-high f_T/f_{max} of 5/17 GHz at V_{DS} = 15 V and V_{GS} = −14.2 V is achieved, along with a peak g_m of 25 mS/mm. DC and RF results are shown in Fig. 17.

4.3. High performance nano-membrane β-Ga_2O_3 SBDs and FETs on foreign substrates

4.3.1. Field-plated lateral β-Ga_2O_3 SBDs on sapphire substrate

β-Ga_2O_3 crystal possesses an unique property that its (100) surface has a large lattice constant of 12.23 Å along [100] direction, which allows a facile cleavage into thin belts or nano-membranes[65]. Hence, by transferring β-Ga_2O_3 nano-membrane from its bulk substrate to a wider bandgap and higher thermal conductivity substrate can minimize low-thermal conductivity of β-Ga_2O_3 bulk substrate induced severe self-heating effect while maintaining its high breakdown characteristics. Importantly as a research route, it provides an effective methodology to investigate fundamental material property of β-Ga_2O_3 and fully explore device potentials without using many β-Ga_2O_3 epitaxy wafers. Hu *et al.* reported on the first high performance lateral β-Ga_2O_3 SBD on sapphire substrate by transferring high quality β-Ga_2O_3 nano-membrane channel from its low defect density bulk substrate[66]. Annealed Ti/Au (60/120 nm) is used as the cathode while Ni/Au (60/120 nm) is used as the anode metal and the β-Ga_2O_3 nano-membrane is with thickness around 400 nm. The SBDs have an on-current on/off ratio of 10^7–10^8 with turn-on voltage (V_{on}) of 1 V determined by the linear extrapolation of the forward I–V. The $R_{on,\,sp}$ of each SBD is determined to be R_{on} = 3.29, 5.94, 12.7, and 34.2 mΩ·cm^2 for $L_{Schottky\text{-}Ohmic}$ = 4, 6, 11, and 15 μm, respectively. The off-state BV is measured to be 0.64 kV, 0.85 kV, 1.2 kV and 1.7 kV, yielding a power FOM of 0.124, 0.121, 0.113, and 0.09 GW/cm^2 for $L_{Schottky\text{-}Ohmic}$ = 4, 6, 11, and 15 μm, respectively, by considering the FOM = $BV^2/R_{on,\,sp}$. Device structure, forward I–V and reverse breakdown characteristics are shown in

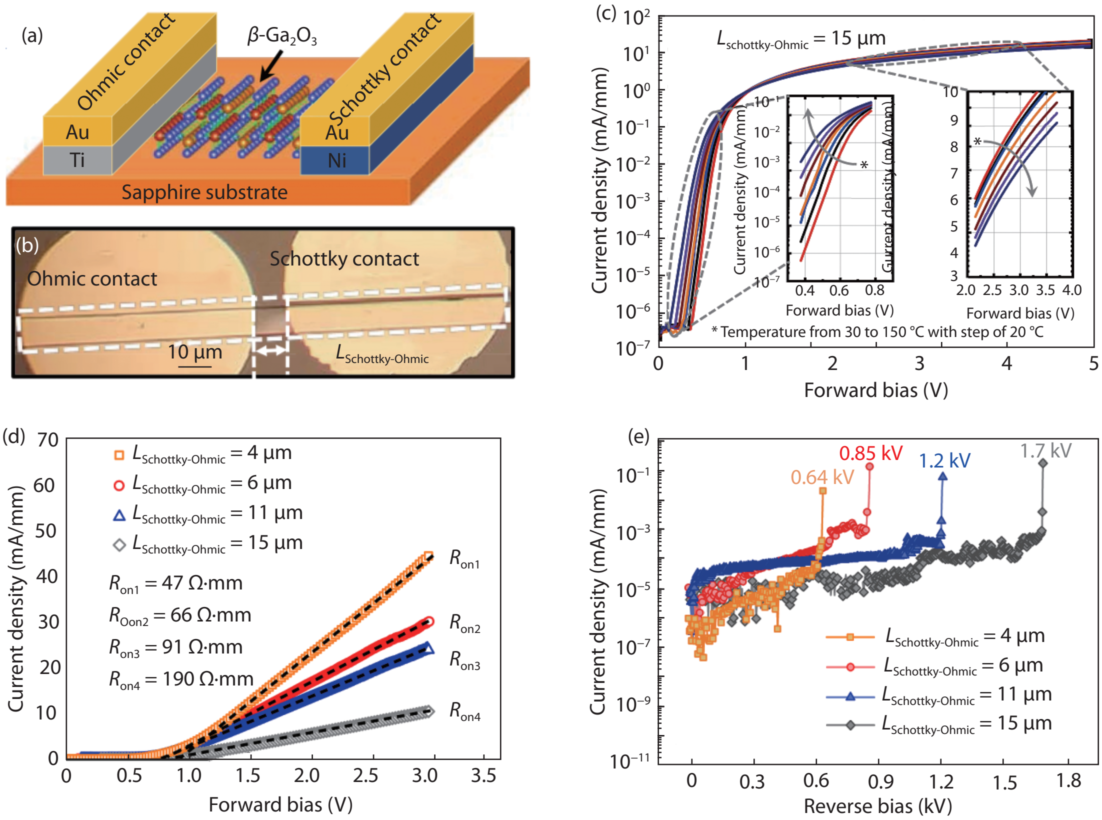

Fig. 18. (Color online) (a) Schematic-view and (b) top-view microscopy image of a fabricated lateral β-Ga_2O_3 SBD on sapphire substrate. (c) Log-scale forward characteristics of β-Ga_2O_3 SBD with $L_{Schottky\text{-}Ohmic}$ = 15 μm at the temperature range from 30 to 150 °C with 20 °C as a step. (d) Linear-scale forward I–V characteristics of β-Ga_2O_3 SBDs with various $L_{Schottky-Ohmic}$. (e) Reverse I–V characteristics of lateral β-Ga_2O_3 SBDs with various $L_{Schottky-Ohmic}$. Reprinted from IEEE JEDS 6, 815, 2018. Copyright of 2018 IEEE[66].

Fig. 18. Following the first lateral β-Ga_2O_3 SBD, Hu *et al.* also developed a field-plated lateral β-Ga_2O_3 SBD with record-high reverse blocking voltage of more than 3 kV and high DC power FOM of 500 MW/cm^2[51]. In this study, an even thicker (650 nm) β-Ga_2O_3 nano-membrane channel is used to improve the on-current and hence reducing the $R_{on,sp}$ and the field plate structure is used to mitigate the E crowding effect at the anode edge. The record-high BV of more than 3 kV is demonstrated on a SBD with $L_{Schottky\text{-}Ohmic}$ = 24 μm with low $R_{on,sp}$ of 24.3 mΩ·cm^2. In addition to the high BV of more than 3 kV, a record high power FOM of 0.5 GW/cm^2 is also achieved on the SBD with $L_{Schottky\text{-}Ohmic}$ = 16 μm and BV = 2.25 kV. The device structure, reverse characteristics and benchmark comparisons between lateral and vertical SBDs are shown in Fig. 19.

4.3.2. High performance back-gate D/E-modes β-Ga_2O_3 on insulator (GOOI) FETs

Zhou *et al.* reported on achieving record-high on-current with a back-gated FETs based on β-Ga_2O_3 nano-membrane channels[67, 68]. Figs. 20(a) and 20(b) are the schematic of a GOOI FET and atomic force microscopy (AFM) image of a β-Ga_2O_3 surface after cleavage, which shows atomically flat and uniform within the whole nano-membrane. Device fabrication commenced with 6 mm by 6 mm (-201) β-Ga_2O_3 bulk substrate with Sn doping concentration of 3 × 10^{18} cm^{-3} and 8 × 10^{18} cm^{-3}. Various β-Ga_2O_3 nano-membranes with thickness from 50 to 150 nm, confirmed by the AFM measurements, were chosen for the device fabrication. Fig. 21(a) presents the D-mode DC output characteristics (I_D–V_{DS}). Devices have a L_{CH} of 0.3 μm, channel width (W) of 0.15 μm and channel thickness (t) of 70 nm for 8.0 × 10^{18} cm^{-3}, and W = 0.6 μm and t = 100 nm for 3.0 × 10^{18} cm^{-3} device, respectively. A record high maximum I_D (I_{DMAX}) of 1.5 A/mm is obtained, which is more than 2 times of lower doping channel. The device also has a much lower R_{on} of 5 Ω·mm compared with that of 11 Ω·mm with 3.0 × 10^{18} cm^{-3} doping concentration. Fig. 21(b) is the log-scale I_D–g_m–V_{GS} transfer characteristics of the same D-mode GOOI FET with 8.0 × 10^{18} cm^{-3} doping concentration. This D-mode GOOI FET has a threshold voltage (V_T) of –135 V, extracted from the log-scale I_D–V_{GS} at V_{DS} = 1 V and I_D = 0.1 mA/mm. Figs. 21(c) and 21(d) depict the I_D–V_{DS} output and I_D–g_m–V_{GS} transfer characteristics of an E-mode GOOI FET with L_{CH} = 0.3 μm, t = 55 nm and W = 0.17 μm for 8.0 × 10^{18} cm^{-3}, and t = 75 nm and W = 0.45 μm for 3.0 × 10^{18} cm^{-3} device also shown in Fig. 21(c) as black dashed curves for comparison. A record high I_{DMAX} = 1.0 A/mm for higher doping channel is obtained, which is more than 80% higher than lower doping channel. E-mode GOOI FET has a V_T of 2 V determined from the I_D–V_{GS} at V_{DS} = 1 V and I_D = 0.1 mA/mm. Further scaling the L_{CH} shows no significant help in boosting the I_{DMAX}, which is primarily limited by the high R_C of low doping channel underneath the contact. The improved I_{DMAX} of D/E-mode devices mainly originate from the higher doping concentration induced lower R_c rather than the simply L_{CH} scaling. Finally, benefiting from its wide-bandgap and a low damage transfer process, both D/E-

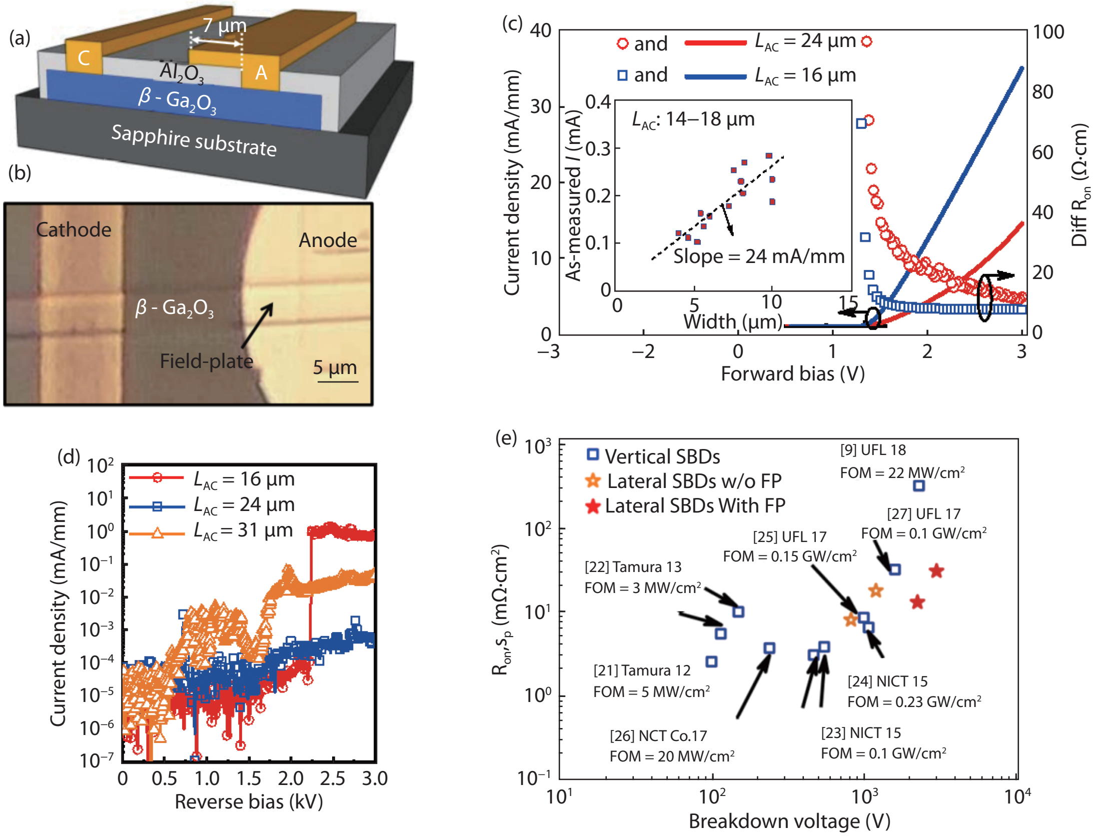

Fig. 19. (Color online) (a) Tilted 3-D schematic-view and (b) top-view microscopy image of a fabricated lateral field-plated β-Ga_2O_3 SBD on Sapphire substrate. (c) Forward I–V and differential R_{on}–V characteristics in linear scale. The inset shows as-measured current dependence on the width of the SBD at a similar L_{AC} of 14–18 μm. (d) Reverse I–V characteristics of lateral SBDs with field plate structure and various L_{AC}. (e) DC $R_{ON,SP}$ versus BV of some both lateral and vertical β-Ga_2O_3 SBDs. Reprinted from IEEE Electron Device Lett, 39, 1564, 2018. Copyright of 2018 IEEE[51].

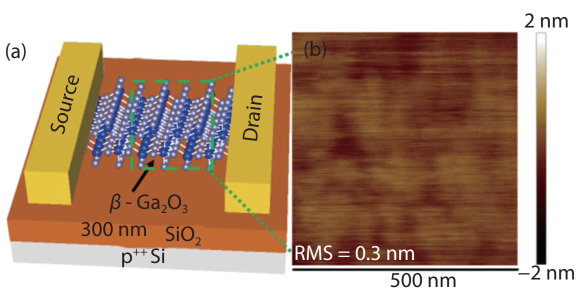

Fig. 20. (Color online) (a) Schematic view of a GOOI FET with a 300 nm SiO_2 layer on Si substrate and (b) AFM image of the atomic flat β-Ga_2O_3 surface after cleavage. Reprinted from IEEE Electron Device Lett, 38, 103, 2017. Copyright of 2017 IEEE[68].

mode devices have achieved high on/off ratio of 10^{10} and low SS of 150–165 mV/dec for a 300 nm thick SiO_2.

4.3.3. VT dependence on the β-Ga_2O_3 Nano-membrane Thickness

It is found that the V_T shifts from negative values in D-mode to positive values in E-mode by shrinking β-Ga_2O_3 nano-membrane thickness. Fig. 22(a) describes the thickness dependent representative I_D–V_{GS} characteristics. Obviously, the V_T is shifted from negative to positive when the thickness is slowly reduced. Fig. 22(b) summarizes the extracted thickness dependent V_T of 15 devices. Generally, they all follow the same trend as shown in Fig. 22(a). The determined thickness dependent V_T may be valuable in the realization of high performance top gate E-mode GOOI FETs in the near future.

The significant V_T shift with respect to different β-Ga_2O_3 nano-membrane thickness is due to the surface depletion of the unpassivated device surface, which has tremendous dangling bonds and surface states on the device surface[69]. This is the reason why E-mode GOOI FETs can also be realized in high doping β-Ga_2O_3 nano-membrane. The surface depletion effect could be verified by using ALD to deposit 15 nm Al_2O_3 on top to passivate the top surface. As shown in Fig. 23(a), the V_T is significantly shifted to the left for more than 70 V after an ALD passivation, verifying the existence of top and bottom surface depletion on unpassivated GOOI FET surfaces. Based on the surface depletion, each surface depleted charge density (n_s) can be estimated by using the TCAD C–V simulation to match the measured and simulated V_T from E-mode devices with V_T near zero. The n_s is determined and simulated to be 1.2×10^{13} cm^{-2} and 2.2×10^{13} cm^{-2} for 3.0×10^{18} cm^{-3} and 8.0×10^{13} cm^{-3} nano-membranes with thickness of 80 nm and 55 nm, respectively. Higher n_s for higher doping β-Ga_2O_3 nano-membrane is most likely related to the higher surface states with more Sn^{+4} dopants. Therefore, the actual C–V curve and I_D–V_{GS} curves are significantly shifted to the right compared with the ideal case without considering surface depletion. Fig. 23(b) shows the simulated C–V curve for E-mode GOOI FET and the V_T from C–V simulation is in good agreement with the V_T from I_D–V_{GS} characterization. Figs. 23(c) and 23(d) are the simulated band diagram of the E-mode GOOI FET at V_{GS} = 0 V with lower doping and higher doping channels by

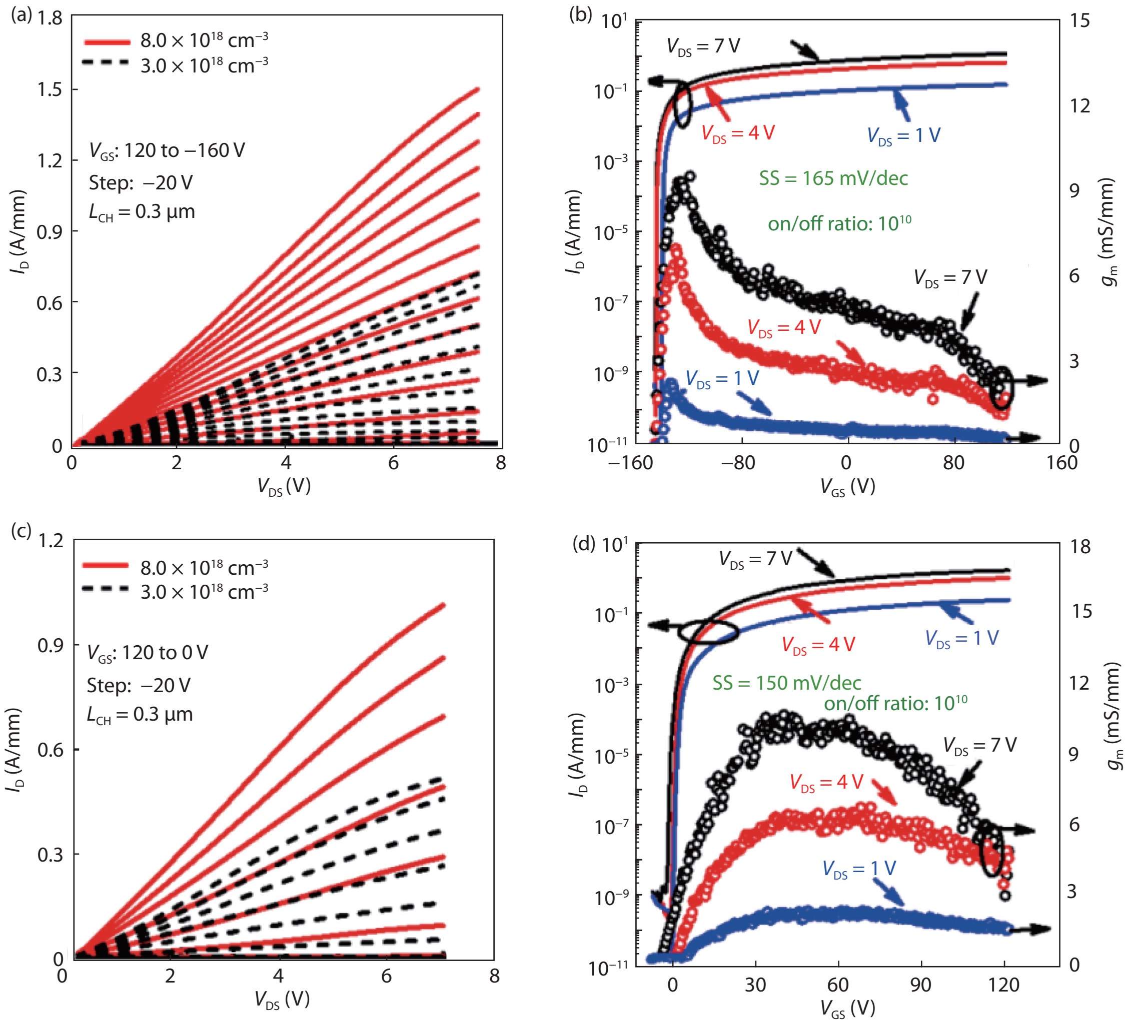

Fig. 21. (Color online) (a) and (c) are I_D–V_{DS} output characteristics of D- and E-mode GOOI FETs with 3.0×10^{18} and 8.0×10^{18} cm^{-3} doping channel, respectively. (b) and (d) are I_D–g_m–V_{GS} transfer characteristics of D-mode and E-mode GOOI FETs with 8.0×10^{18} cm^{-3} doping channel, respectively. Record high I_{DMAX} of 1.5 and 1.0 A/mm are demonstrated for D/E mode devices. Both D and E-mode devices have high on/off ratio of 10^{10} and low SS of 150–165 mV/dec for 300 nm SiO_2. Reprinted from Appl Phys Lett, 111, 092102, 2017. Copyright of 2017 AIP[67].

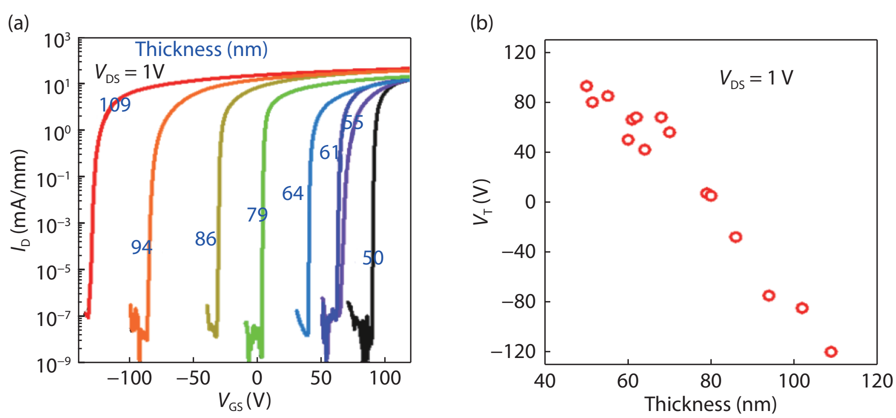

Fig. 22. (Color online) (a) Thickness dependent I_D–V_{GS} plots of various GOOI FETs from D-mode of thicker β-Ga_2O_3 to E-mode of thinner β-Ga_2O_3. (b) Thickness dependent V_T extracted at V_{DS} = 1 V of 15 devices. Reprinted from IEEE Electron Device Lett, 38, 103, 2017. Copyright of 2017 IEEE[68].

considering surface depletion effect. The top and bottom depletion regions pull up the conduction band of β-Ga_2O_3 with very few carriers left behind in the nano-membrane, so that E-mode GOOI FET can be formed.

4.3.4. Solutions to the severe self-heating effects on β-Ga_2O_3 FETs

Self-heating effect induced temperature increase and non-uniform distribution of dissipated power have emerged

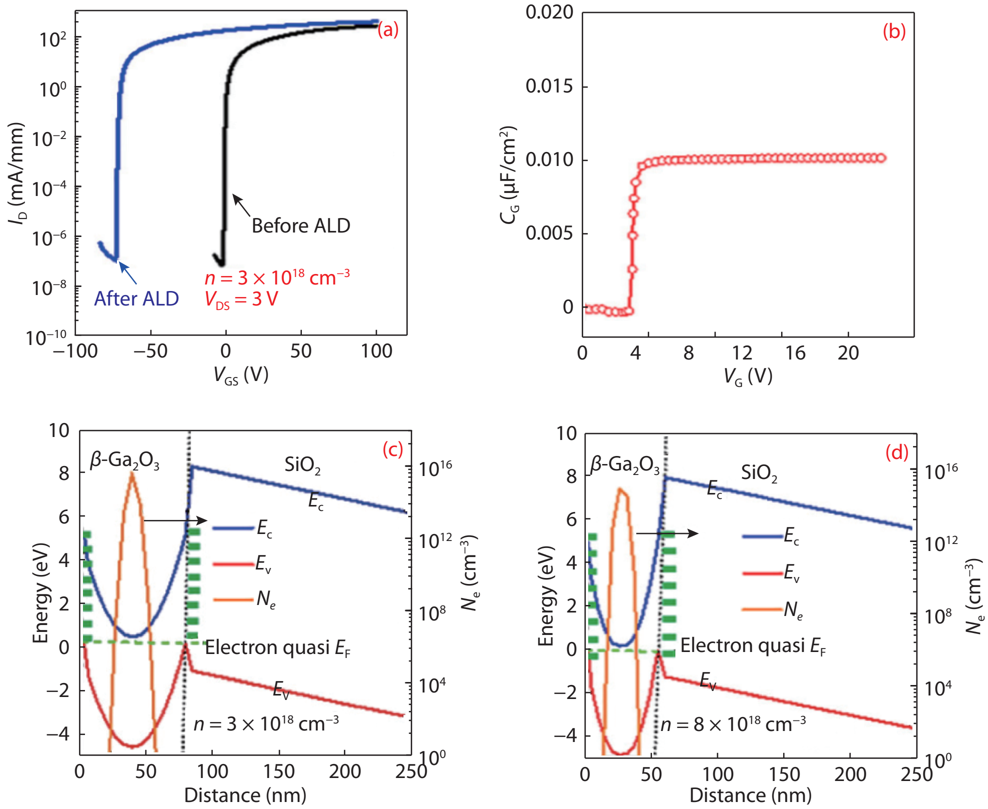

Fig. 23. (Color online) (a) I_D–V_{GS} comparison between GOOI FETs with and without ALD passivation for β-Ga_2O_3 nano-membrane with doping concentration of 3.0 × 10^{18} cm^{-3}, (b) simulated C–V curve for E-mode GOOI FET at a β-Ga_2O_3 nano-membrane thickness of 80 nm and doping concentration of 3.0 × 10^{18} cm^{-3} after considering the top and bottom negative surface charge (n_s = 1.2 × 10^{13} cm^2) depletion effect. Band diagram and electron density distribution of E-mode GOOI FETs with surface negative charge depletion on (c) lower doping (n_s = 1.2 × 10^{13} cm^{-2}) and (d) high doping (n_s = 2.2 × 10^{13} cm^{-2}) β-Ga_2O_3 nano-membrane channels at V_{GS} = 0 V. Reprinted from Appl Phys Lett, 111, 092102, 2017. Copyright of 2017 AIP[67].

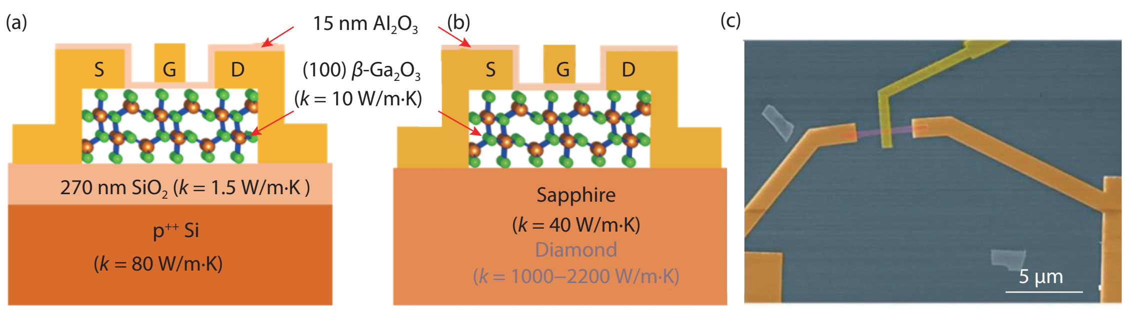

Fig. 24. (Color online) Cross-section schematic view of a top-gate GOOI FET on (a) SiO_2/Si and (b) sapphire and diamond substrates with different κ marked. 15 nm of Al_2O_3 is used as the gate dielectric, Ti/Al/Au (15/60/50 nm) is used as the source/drain electrodes, and Ni/Au (30/50 nm) is used the gate electrode. (c) False-colored SEM top-view of a GOOI FET with L_G = 1 μm and L_{SD} = 6 μm. Reprinted from ACS Omega 2,11, 2017. Copyright of 2017 ACS[71].

as one of the most dominant concerns in the degradation of the I_D, output power density (P), as well as the gate leakage current, device variability, and reliability[70]. This effect would become severe in high power device with a low thermal conductivity (κ) substrate such as β-Ga_2O_3, whose κ is just 10–25 W/m·K, which has become one of major challenges to realize practical application. An effective approach to mitigate low κ problem is to utilize a higher κ substrate rather than the β-Ga_2O_3 native substrate through a potential wafer bonding technique. Nowadays, all the GOOI FETs were fabricated on the SiO_2/Si substrate, however the κ of SiO_2 is just 1.5 W/(m·K). For the thermal management of GOOI FETs, a higher κ substrate is urgently needed. Diamond has the highest thermal conductivity (κ = 1000–2200 W/(m·K)) among all available substrates; thus, it is of great interest to investigate the heat dissipation effect of β-Ga_2O_3 devices on diamond. Meanwhile, diamond is also a current blocking substrate for transferred β-Ga_2O_3 nanomembranes due to its wide bandgap of 5.47 eV. In this section, sapphire and diamond substrates are used as a thermal conductor for GOOI FETs to solve the severe self-heating effect and enhance the thermal dissipation and boost device performance[71, 72]. An ultra-fast, high-resolution thermos-reflectance (TR) imaging technique[73] is introduced and then applied to the top-gate GOOI FET to examine the reduced self-heating ef-

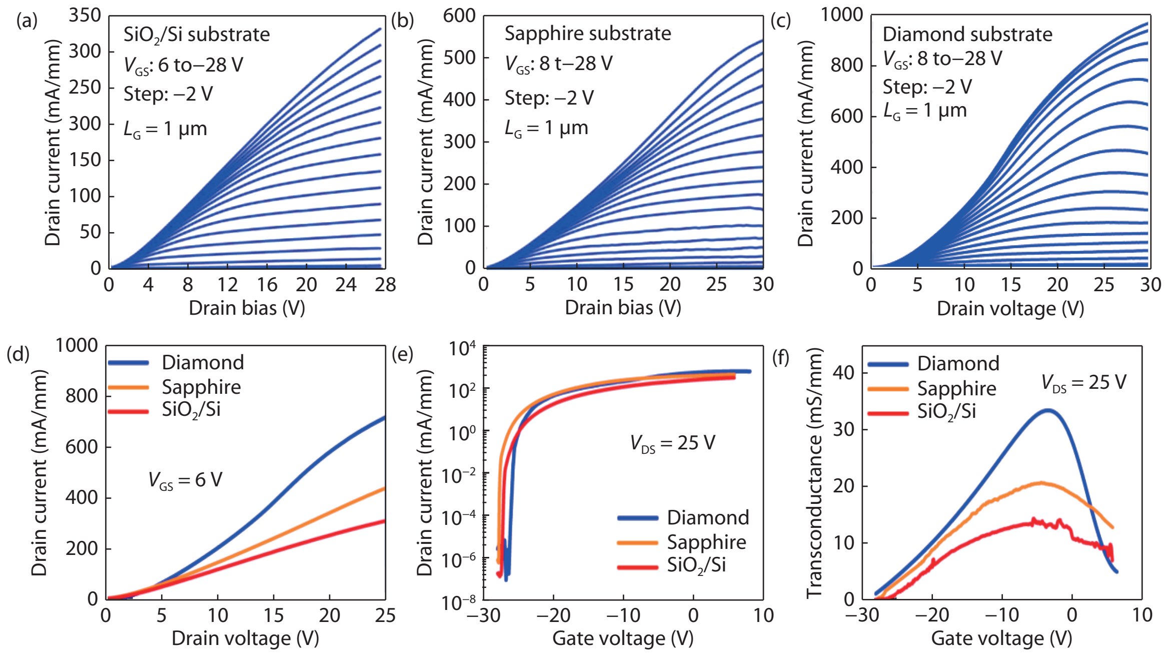

Fig. 25. (Color online) I_D–V_{DS} characteristics of GOOI FETs on (a) SiO_2/Si, (b) sapphire and (c) diamond substrates with L_{SD} = 6–6.5 μm and L_G = 1 μm. A high I_{DMAX} = 960 mA/mm is demonstrated on top-gate β-Ga_2O_3 GOOI FETs. Comparison of (d) I_D–V_{DS} (e) log-scale I_D–V_{GS} and (f) linear-scale g_m–V_{GS} of β-Ga_2O_3 FETs on a diamond, sapphire and SiO_2/Si substrates. I_D–V_{GS} transfer characteristics of GOOI FETs on three substrates with high on/off ratio of 10^9 and low SS of 65 mV/dec, yielding a low D_{it} of 2.6 × 10^{11} eV^{-1}·cm^{-2}. Higher g_m shows higher electron μ on diamond due to the reduced device temperature. Reprinted from ACS Omega 2,11, 2017. Copyright of 2017 ACS[71] and 2018 IEEE[72].

fect and local surface temperature increase magnitude on sapphire and diamond substrates compared with SiO_2/Si substrate. After substituting SiO_2/Si with sapphire and diamond substrates, the top-gate GOOI FET has 70% and 2 times higher I_{DMAX}, ~ 3 times and 8 times lower device surface temperature change ΔT, and 3 times and 8 times lower thermal resistance (R_T), respectively.

Figs. 24 (a)–24(c) are the device schematic and SEM images of fabricated GOOI FETs, respectively. Source and drain regions were defined by the VB6 EBL, followed by Ti/Al/Au (15/60/50 nm) metallization and lift-off processes. 15 nm of Al_2O_3 was deposited by ASM F-120 ALD at 180 °C with trimethyl-aluminum (TMA) and H_2O as precursors. Finally, Ni/Au (50/50 nm) is deposited as the gate electrode, followed with lift-off process.

Figs. 25(a), 25(b) and 25(c) show the well-behaved DC I_D–V_{DS} of three top-gate GOOI FETs with L_{SD} of 6/6.5 μm, L_G of 1 μm, and channel thickness of 73/75/74 nm on SiO_2/Si, sapphire and diamond substrates, respectively. I_{DMAX} of 960, 535 and 325 mA/mm for diamond, sapphire and SiO_2/Si substrates are obtained. I_{DMAX} of GOOI FET on diamond and sapphire substrates is around 3 times and 1.7 times of that on SiO_2/Si substrate, originating from better transport properties at a lower device temperature. Fig. 25(d) is the I_D–V_{DS} comparison at a fixed V_{GS} = 6 V. Figs. 25(e) and 25(f) depict the I_D–V_{GS} and g_m–V_{GS} of GOOI FETs on three substrates at V_{DS} = 25 V. High on/off ratio of 10^9 and low SS of 65 mV/dec are achieved on both devices due to the wide bandgap and high-quality ALD Al_2O_3/β-Ga_2O_3 interface, yielding a low interface trap density (D_{it}) of 2.6 × 10^{11} eV^{-1}·cm^{-2} by the equation SS = 60 × (1 + qD_{it}/C_{ox}) mV/dec at room temperature, where C_{ox} is the oxide capacitance. One interesting phenomenon is that the peak g_m of diamond and sapphire substrate is 34 mS/mm and 21 mS/mm, which is around 2 times and 60% higher than the g_m of SiO_2/Si substrate. The extrinsic electron field-effect mobility (μ_{FE}) of GOOI FET on diamond, sapphire and SiO_2/Si are roughly extracted to be 43, 30.2 and 21.7 cm^2/(V·s), respectively, benefiting from the less SHE on diamond.

Figs. 26(a), 26(b) and 26(c) are the merged optical and TR thermal image views of GOOI FETs on SiO_2/Si, sapphire and diamond substrates at steady state and different P conditions. As higher V_{DS} is applied, the device is heated up simultaneously and the corresponding ΔT is increased. At P = 717 W/mm^2 on the SiO_2/Si substrate, the ΔT is measured to be 106 K, whereas in contrast the ΔT is just 43 and 21 K at a higher P = 917 W/mm^2 and P = 1237 W/mm^2 on the sapphire and diamond substrates, respectively. Fig. 26(d) depicts the measured and simulated ΔT versus P (W/mm^2) for the Ga_2O_3 FETs on a diamond substrate, performed both by TR imaging and Raman thermography. Good agreement among these three methods can be observed, with the highest temperature measured by Raman thermography to be 164 °C (ΔT = 141 K) at DC output power of 6565 W/mm^2 (64.7 W/mm or V_{DS} = 35 V for this particular exfoliated FET geometry). Fig. 26(e) shows the good agreement of the TR measured and the simulated ΔT versus P (W/mm^2) on different substrates. For both the measurement and simulation results, the clear observation is that at the same P, the GOOI FET on the diamond substrate has more than 8 times lower ΔT compared to that on SiO_2/Si. The R_T of diamond, sapphire and SiO_2/Si substrates are calculated to be 1.71 × 10^{-2}, 4.62 × 10^{-2} and 1.47 × 10^{-1} mm^2·K/W, respectively, through R_T = $\Delta T/P$. The reduced R_T of GOOI FET on diamond and sapphire demonstrate that a higher κ substrate can be more effective in dissipating the heat on the devices. With less heat on the device, the temperature is lower so that the μ is higher to achieve a higher I_{DMAX} of 960 mA/mm for a better device performance.

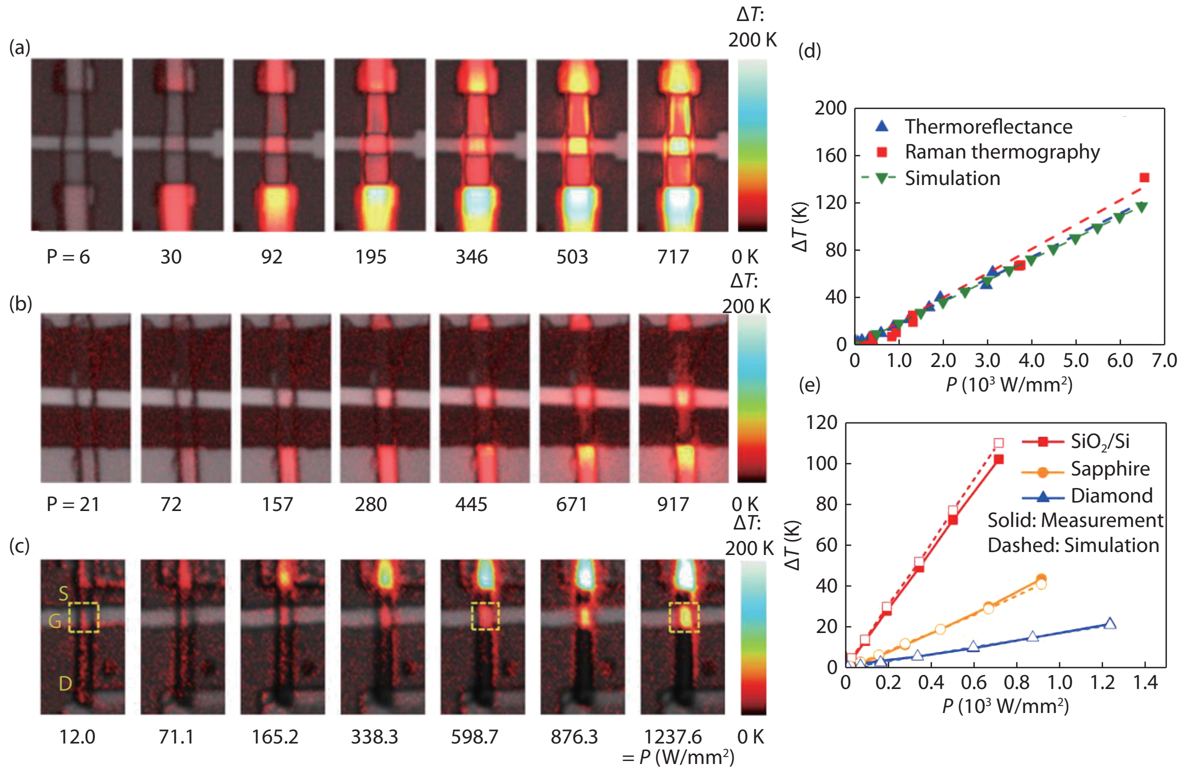

Fig. 26. (Color online) TR and charge-coupled device (CCD) camera merged images of GOOI FET on (a) SiO_2/Si, (b) sapphire and (c) diamond substrates when device P is increased by increasing V_{DS} at V_{GS} = 0 V. (d) Comparison of measured or simulated ΔT versus P (W/mm²) characteristics of top-gate GOOI FETs on a diamond substrate using TR imaging, Raman thermography and the thermal simulations. (e) Measured by TR method and simulated ΔT versus P characteristics of top-gate GOOI FETs on different substrates. The ΔT of GOOI FET on the SiO_2/Si substrate is more than 3 and 8 times of that on the sapphire and diamond substrates at the same P. As a result, the R_T of GOOI FET on the sapphire substrate is 4.62 × 10^{-2} and 1.71 × 10^{-2} mm²·K/W, which is less than 1/3 and 1/8 of that on the SiO_2/Si substrate. Reprinted from ACS Omega 2,11, 2017. Copyright of 2017 ACS[71].

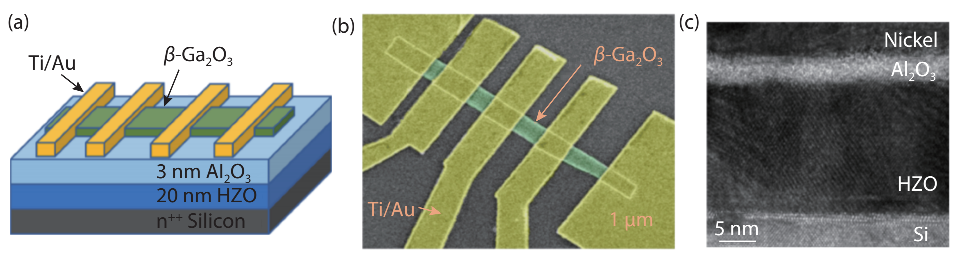

Fig. 27. (Color online) (a) Schematic view of β-Ga_2O_3 FE-FETs. The gate stack includes a heavily n-doped Si as the gate electrode, 20 nm HZO as the ferroelectric insulator, 3 nm Al_2O_3 as the capping layer. Ti/Au (30/60 nm) is used as the source/drain electrodes. Sn-doped n-type β-Ga_2O_3 (86 nm) is used as the channel. (b) Top-view false-color SEM image of representative β-Ga_2O_3 FE-FETs on the same membrane with different channel lengths. (c) Cross-sectional view of the HZO/Al_2O_3 gate stack, capturing the polycrystalline HZO and the amorphous Al_2O_3. Reprinted from ACS Omega 2,10, 2017. Copyright of 2017 ACS[74].

4.3.5. β-Ga_2O_3 nano-membrane ferroelectric (FE)-FET with steep ss for wide bandgap logic application

High-temperature solid-state devices and circuits are required for many applications such as in aerospace, automotive, nuclear instrumentations and geothermal wells. Silicon-based complementary metal–oxide–semiconductor (CMOS) technology is not able to operate at such high temperatures, which is limited by its relatively small band gap of 1.12 eV. CMOS circuits using wide band gap semiconductors are promising in these high temperature logic applications. As for the logic application, steep SS is required so as to minimize the power supply so that power consumption and SHE are less severe. In this section, β-Ga_2O_3 FE-FETs with ferroelectric HZO as a gate dielectric stack is reviewed[74]. Fig. 27(a) shows the schematic diagram of β-Ga_2O_3 FE-FETs, which consists of a 86 nm thick β-Ga_2O_3 nanomembrane as the channel, a 3 nm amorphous Al_2O_3 layer and a 20 nm polycrystalline HZO layer as the gate dielectric, a n^{++} silicon substrate as the gate electrode, and a Ti/Au source/drain as the metal contacts. Fig. 27(b) shows the false-color SEM image of the fabricated β-Ga_2O_3 FE-FETs with four different channel lengths, capturing the β-Ga_2O_3 membrane and the Ti/Au electrodes.

Fig. 28(a) shows the normalized I_D–V_{GS} characteristics in the log scale of a β-Ga_2O_3 FE-FET. The back-gate bias is swept from −0.4 to 2 V in 40 mV per step, whereas the V_{DS} is biased at

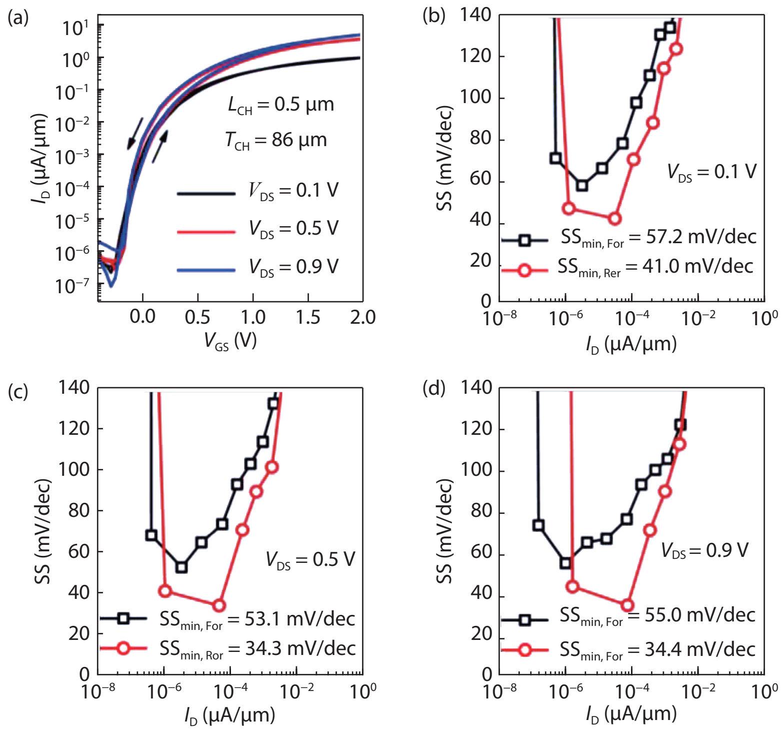

Fig. 28. (Color online) (a) I_D–V_{GS} characteristics in the log scale of a β-Ga_2O_3 FE-FET. This device has a channel length of 0.5 μm and a channel thickness of 86 nm. SS versus I_D characteristics of the same device in (a) at (b) V_{DS} = 0.1, (c) V_{DS} = 0.5, and (d) V_{DS} = 0.9 V. SS less than 60 mV/dec at room temperature is demonstrated for both forward and reverse V_{GS} sweeps. Reprinted from ACS Omega 2,10, 2017. Copyright of 2017 ACS[74].

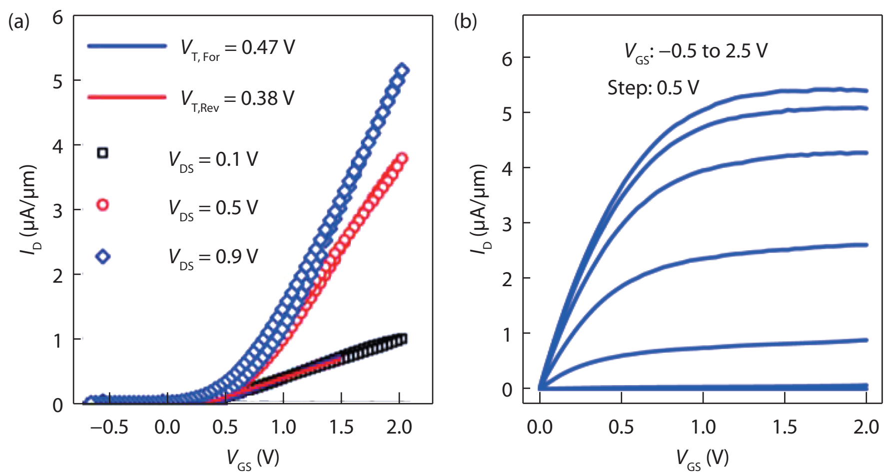

Fig. 29. (Color online) (a) I_D–V_{GS} characteristics in the linear scale of the same β-Ga_2O_3 FE-FET as in Fig. 9. (b) I_D–V_{DS} characteristics of the same β-Ga_2O_3 FE-FET as in Fig. 9. Reprinted from ACS Omega 2,10, 2017. Copyright of 2017 ACS[74].

0.1, 0.5, and 0.9 V. The whole sweep takes roughly 1 min. This device has a L_{CH} of 0.5 μm and a thickness of 86 nm. This particular thickness is chosen to tune the V_T slightly above zero. The I_D–V_{GS} characteristics were measured in bidirectional both forwardly (V_{GS} from low to high) and reversely (V_{GS} from high to low). SS is extracted as a function of I_D for both forward sweep ($SS_{min,For}$) and reverse sweep ($SS_{min,Rev}$) at various V_{DS}. Figs. 28(b)–28(d) show the SS–I_D characteristics extracted from Fig. 28(a) at V_{DS} = 0.1, 0.5, and 0.9 V, respectively. The device exhibits $SS_{min,For}$ = 57.2 mV/dec and $SS_{min,Rev}$ = 41.0 mV/dec at V_{DS} = 0.1 V, $SS_{min,For}$ = 53.1 mV/dec and $SS_{min,Rev}$ = 34.3 mV/dec at V_{DS} = 0.5 V, and $SS_{min,For}$ = 55.0 mV/dec and $SS_{min,Rev}$ = 34.4 mV/dec at V_{DS} = 0.9 V. SS less than 60 mV/dec at room temperature is demonstrated for both forward and reverse V_{GS} sweeps even at relatively high V_{DS}. Ga_2O_3 MOSFETs with 15 nm Al_2O_3 as a gate dielectric exhibit a minimum SS = 118.8 mV/dec. SS–I_D characteristics at different V_{DS} are similar, slightly better at high V_{DS} because of the larger impact of a Schottky barrier at lower V_{DS}. Because of the large band gap of β-Ga_2O_3, the band-to-band tunneling current at high V_{DS} is suppressed. Fig. 29(a) shows the I_D–V_{GS} characteristics in the linear scale of the same β-Ga_2O_3 FE-FET as in Fig. 28. V_T is extracted by linear extrapolation at V_{DS} = 0.1 V for both forward and reverse V_{GS} sweeps. V_T in the forward V_{GS} sweep ($V_{T, For}$) is extracted as 0.47 V, whereas V_T in the reverse V_{GS} sweep ($V_{T, Rev}$) is extracted as 0.38 V. Hence, the E-mode operation with V_T greater than zero for both forward and reverse V_{GS} sweeps is demonstrated. A negligible hysteresis is obtained for both on-state (high V_{GS}, as shown in Fig. 10(a)) and off-state (low V_{GS}, as shown in Fig. 28(a)), except that when V_{GS} is near the V_T region. At the V_T, low hysteresis is achieved to be 90 mV, calculated by using $|V_{T, Rev} - V_{T, For}|$, showing the great promise of using β-Ga_2O_3 for wide bandgap logic applications.

5. Conclusions

In conclusion, significant progresses have been achieved with remarkable power device performances even at this premature development stage, such as BV more than 3 kV of lateral Schottky Rectifiers, high current density 1.5/1 A/mm of D/E-modes FETs, BV of 1.8 kV for field-plated lateral MOSFET and f_T/f_{amx} of 5.1/17.1 GHz, respectively. In addition to device performance, sufficient low defect density less than 10^3 cm^{-2} of melt-grown native substrate and very smooth surface with RMS roughness less than 0.5 nm of epitaxial β-Ga_2O_3 thin film on its native substrate have all been demonstrated. However, some open questions about how to realize p-type β-Ga_2O_3 and how to resolve the low thermal conductivity issue are yet to be established. Once resolving those aforementioned issues, the bright future of β-Ga_2O_3 devices as power electronic products are definitely coming soon.

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